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THE CONTROL SYSTEM OF THE NEW SMALL WHEEL ELECTRONICS FOR THE ATLAS EXPERIMENT

P. Tzanis*,[1,2], on behalf of the ATLAS Collaboration
[1] National Technical University of Athens, Athens, Greece
[2] Brookhaven National Laboratory, Upton, NY, USA

Abstract

The present ATLAS Small Wheel Muon detector will be replaced with a New Small Wheel (NSW) detector in order to cope up with the future LHC runs of high luminosity. One crucial part of the integration procedure concerns the validation of the electronics for a system with more than 2.1 M electronic channels. The readout chain is based on optical link technology connecting the back-end to the front-end electronics via the FELIX, which is a newly developed system that will serve as the next generation readout driver for ATLAS. For the configuration, calibration and monitoring path the various electronics boards are supplied with the GBT-SCA ASIC and its purpose is to distribute control and monitoring signals to the electronics. Due to its complexity, NSW electronics requires the development of a sophisticated Control System. The use of such a system is necessary to allow the electronics to function consistently, safely and as a seamless interface to all sub-detectors and the technical infrastructure of the experiment. The central system handles the transition between the probe's possible operating states while ensuring continuous monitoring and archiving of the system's operating parameters.

NEW SMALL WHEEL

In order to efficiently handle the increased luminosity that will be provided by the High-Luminosity LHC (HL-LHC), the first station of the ATLAS [1] muon end-cap system (Small Wheel, SW) will need to be replaced. The New Small Wheel (NSW) [2] will have to operate in a high background radiation region (up to 22 kHz/cm²) while reconstructing muon tracks with high precision as well as providing information for the Level-1 trigger. The detector technologies to be used come from the family of gaseous detectors, the first is called small-strip Thin Gap Chambers (sTGCs), and the second comes from the category of micro-pattern gas detectors and is named Micromesh Gaseous Structure (Micromegas (MM)) [3] . The new experimental layout will consist of 16 detection layers in total and 8 layers per detection technology (8 layers sTGC and 8 layers Micromegas), as shown in Fig. 1. The sTGC detectors are designed to provide fast trigger and high precision muon tracking under the HL-LHC conditions. On the other hand, Micromegas detectors have a small conversion region (5 mm) and fine strip pitch (0.45 mm) resulting in excellent spatial resolution and are primarily used for precise tracking.

* polyneikis.tzanis@cern.ch

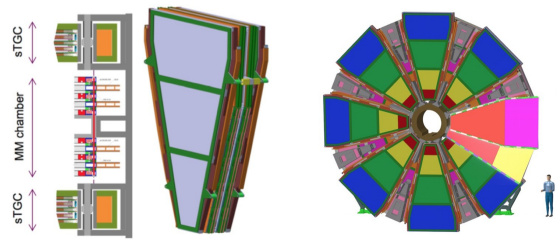

Figure 1: A graphic representation of the NSW sector (left) which consists of 8 layers of Micromegas in the inner part and sandwiched by 4+4 layers of sTGC detectors in the outer parts and view of the NSW (right) with 16 sectors in total. [4]

ELECTRONICS OVERVIEW

The NSW electronics for the trigger and Data Acquisition (TDAQ) path of both detectors is divided into two major categories, on-detector and off-detector electronics, as shown in Fig. 2. On the left-hand side, the front-end boards that

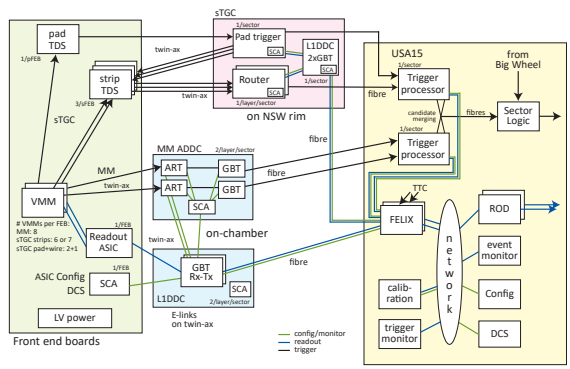

Figure 2: Overview of the NSW electronics scheme. The front-end detector boards are depicted on the left (for MM and sTGC), the data-driver cards (L1DDC, ADDC) in the middle while the back-end electronics can be seen on the right. [4]

are attached to the chambers bear VMMs, SCAs(Slow Control Adapter) and ROCs(Read Out Controller), while for the sTGCs they also host TDS chips. The ROC aggregates L1 data from many VMMs [5] and sends them to (Front End LInk eXchange (FELIX) [6] via the GBTx [7]. FELIX also sends trigger signals to the front-end electronics via the ATLAS TTC system. It also sends tracking data from the ROC to the swROD (here depicted to send the data fragments to the HLT), and communicates with the Detector Control System (DCS) [8] for slow control purposes. The Micromegas trigger data are collected from many VMMs by

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the ART ASIC, which sends them towards the Micromegas trigger processor, alongside geographical and timestamp information. The TDS chips on the other hand, handle the sTGC trigger primitives, and alongside the Pad Trigger and Router boards, are part of the more complex sTGC trigger chain, which has the associated trigger processor FPGA on the back-end as a final destination of its data-flow. Both FPGAs create muon candidates that are then transmitted to the SL. The NSW on-detector electronics (Front-End boards (MMFE8), Level-1 Data Driver Card (L1DDC), ART (Address in Real Time) Data Driver Card (ADDC)) will be placed inside the cavern (detector area with radiation and magnetic fields) and consists of custom-made boards mainly using radiation-tolerant Application Specific Integrated Circuits (ASICs). The communication between these boards will be established with the use of mini Serial Attached Small Computer System Interface (SCSI) cables. The off-detector electronics FELIX, trigger processor, sector logic and services running on commercial server computers like Read Out Drivers (ROD), Detector Control System (DCS), event monitoring, configuration, trigger monitor and calibration) will be placed outside the cavern in an area that is called USA15.

FELIX

The keystone of the ATLAS DAQ system will be the FELIX which is an FPGA-based system housed by a commercial server. FELIX will essentially be a bridge between the front-end electronics of all ATLAS detector subsystems, and their corresponding back-end components, which will mostly be software-based, as shown in Fig. 3. Situated in

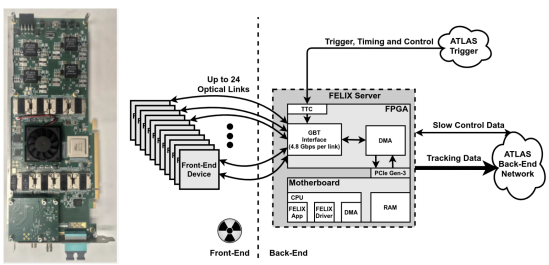

Figure 3: Left: The FELIX BNL712 FPGA board, which the NSW will use for its needs. It features a Xilinx® Kintex Ultrascale XCKU115 FPGA, a PCIe connector to interface with the CPU and the back-end network, and an optical coupler supporting up to 24 links. A dedicated mezzanine board receives the reference clock and the trigger information from the ATLAS TTC system. Right: FELIX and its relationship with other parts of the DAQ system.

the USA15, FELIX connects to the front-end electronics of the ATLAS cavern via optical links, or GBT links, each one of which is running at 4.8 Gb/s. For the NSW case, FELIX will interface with the front-end nodes over 24 optical links. These links carry the GBT frame, which is 84-bit wide. The Giga-Bit Transceiver (GBT) protocol is a transmission scheme that involves radiation-tolerant ASICs that are capable of handling the large amounts of data of high energy physics experiments.

GBT-SCA

The GBT-SCA ASIC (Giga-Bit Transceiver - Slow Control Adapter) [9] is an integrated circuit built in a commercial 130 nm CMOS technology and is the part of the GBT chipset which purpose is to distribute control and monitoring signals to the front-end electronics embedded in the detectors. It connects to a dedicated electrical port on the GBTx ASICs through an 80 Mbps dual redundant bidirectional data-link; namely the e-links. In order to meet the requirements of different front-end ASIC in various experiments, the SCA provides a number of user-configurable electrical interface ports, able to perform concurrent data transfer operations. The user interface ports are: 1 SPI master, 16 independent I2C masters, 1 JTAG master and 32 general-purpose IO signals with individual programmable direction and interrupt generation functionality. It also includes 31 analog inputs multiplexed to a 12 bit ADC featuring offset calibration and gain correction as well as four analog output ports controlled by four independent 8-bits DACs. An illustration of the different blocks are displayed on Fig. 4.

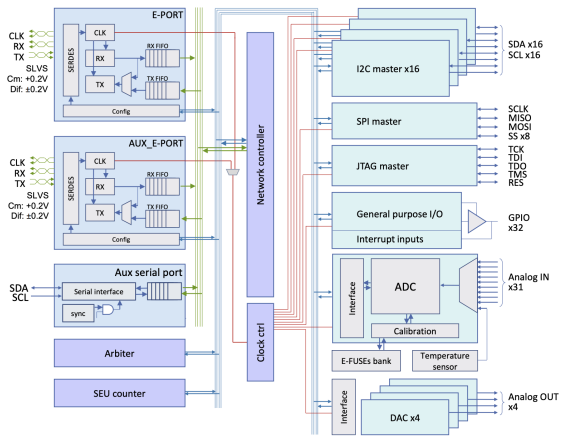

Figure 4: Overview of the GBT-SCA block diagram. [9]

SCA OPC-UA SERVER

For the NSW project alone, ≈ 6400 SCAs will be used to configure and monitor various ASICs that are part of the general DAQ scheme. All of these SCAs communicate with the back-end (i.e. FELIX) via the GBTx, which implements the GBT protocol in its logic, while FELIX implements the GBT-FPGA core in order to communicate with the aforementioned package. The SCA-to-GBTx interface is the E-link, a serial differential line running at 80 Mb/s over HDLC encoding. The protocol defined by the SCA's requirements is request/respond that is, for every packet received by the SCA, the back-end that originally transmitted the packet awaits for an associated reply by the SCA. In this SCA-GBTx-FELIX communication chain, the last two components can be viewed as data mediators, so there is one piece missing: the back-end logic that actually

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builds the packets-to-be-transmitted to the SCA, and handles the inbound traffic from the ASIC. This is a software suite, which is a dedicated Open Communications Platform Unified Automation (OPC-UA) server. Overview of the on/off-detector electronics and the DCS, Configuration and Calibration path via the SCA, the FELIX and the SCA OPC UA Server is illustrated in Fig. 5. A common readout path and a separate trigger path are developed for each detector technology. The communication chain starts in the control room with an OPC-UA client, which is the first step into our detector control system. Configuration and monitoring data is requested and sent from here to the OPC-UA server and next to the FELIX PCs, which lie in the underground service area. Then, through radiation-hard fibers, we reach the GBTx chips, which implement the optical links, to finally arrive to the SCA.

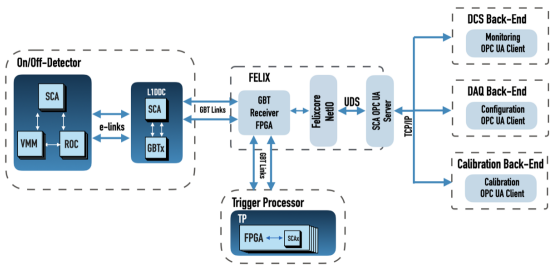

Figure 5: Representation of the on/off-detector electronics and the DCS, Configuration and Calibration path via the SCA, the FELIX and the SCA OPC UA Server [4]

ATLAS DETECTOR CONTROL SYSTEM

The ATLAS DCS has the task to permit coherent and safe operation of ATLAS and to serve as a homogeneous interface to all sub-detectors and the technical infrastructure of the experiment. The DCS must bring the detector into any desired operational state, continuously monitor and archive the operational parameters, signal any abnormal behavior. The DCS was designed and implemented within the frame of the Joint Controls Project (JCOP), a collaboration of the CERN controls group and DCS teams of the LHC experiments. Standards for DCS hardware and software were established together with implementation guidelines both, commonly for [10] and specifically for ATLAS. It combines common standards for the use of DCS hardware based on SCADA system Siemens, WinCC Open Architecture, also known as PVSS with its older name, where it serves as the basis for all DCS applications. Figure 6 depicts the architecture of DCS which can be divided into Front-End (FE) equipment and a system Back-End (BE).

FE includes equipment DCS, including customized electronic systems and related services such as high voltage power supplies and cooling circuits. The BE system uses the software WinCC, integrating front-end control systems into the framework components to facilitate the integration of standard hardware devices and the implementation of homogeneous control applications. The two ends of DCS

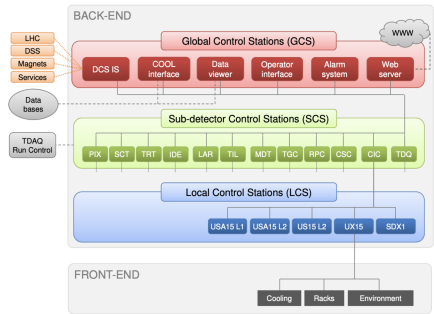

Figure 6: Graphical representation of the DCS architecture of the experiment ATLAS divided into 3 levels: GCS, SCS and LCS. [8]

communicate mainly through the industrial protocol bus CAN, while the communication standard OPC is used as a communication software protocol. The system BE is organized hierarchically on three levels, the Local Control Stations (Local Control Stations (LCS), the Sub-detector Control Stations (SCS)) and the Central Control Stations (Global Control Stations (GCS)). In total, BE consists of more than a hundred computer stations connected to a distributed system. Communication between subsystems of the system is handled by WinCC via a local area network. A distributed finite state machine, Finite State Machine (FSM), represents the complete hierarchy of the BE system as it integrates more than 10 million data elements into a single tree structure and ensures proper operation and efficient handling errors in each operating layer. The most important element of this system is the structure data point (DP), which plays the role of the global variable network. Each element of this structure has a unique name and configurability, and special DPs are used to read data from the hardware components updated by the interface OPC client-server communication.

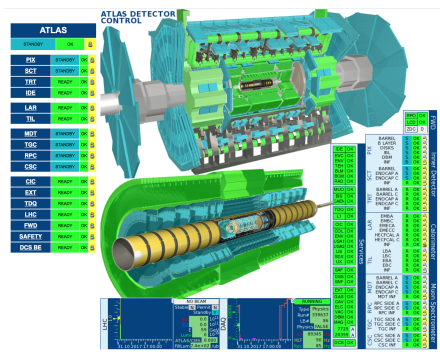

Figure 7: Operator interface (FSM Screen) showing the detector in STANDBY configuration during LHC ramp-up. The top hierarchy level object is shown together with its children objects (top left) and the associated main panel (bottom right). The UI allows the navigation to any FSM object and associated panel within the whole ATLAS DCS hierarchy. On the top right, a list of objects with non-OK Status allow shortcut navigation to problems. [8]

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Each node FSM has a unique name based on the subsystem name and its functionality following the conventions of ATLAS DCS and the state in which they are specified by a corresponding internal DP. The type of object FSM which defines the basic functionality of the node and its components, depends on the functional purpose and position of the element in the DCS architecture hierarchy. The main graphical user interface of ATLAS DCS with all subsystems integrated into a hierarchical structure FSM is illustrated in Fig. 7. The FSM is based on a strict hierarchical structure that constitutes parent-child relationships, where in tree construction commands are passed from parents to children, and situations from children to parents. This way, when some action is required on all children it is extremely efficient to command a higher node and correspondingly the status of the higher node summarizes the status of all nodes of any generation. All nodes are in a predefined state and only accept predefined commands as defined in the FSM type to which they belong. The DCS is operated from two primary, remotely accessible user interfaces – the FSM Screen for operation of the detector Finite State Machine hierarchy (see Fig. 7) and the Alarm Screen for alarm recognition and acknowledgment. Static status monitoring is provided by web pages on a dedicated web server allowing to quickly visualize all high level FSM user interface panels world-wide and without additional load of BE control stations.

NSW DETECTOR CONTROL SYSTEM

Due to its complexity and long-term operation, the NSW requires the development of a sophisticated Detector Control System (DCS). The use of such a system is necessary to allow the detector to function consistently and safely as well as to function as a seamless interface to all sub-detectors and the technical infrastructure of the experiment.

Architecture

The NSW DCS architecture and its integration with the ATLAS DCS have been finalized and projects will closely follow the existing look, feel and command structure of Muon DCS, to facilitate the shifter and expert operations. The current plan is to have 2 new sub-detectors, MMG (Micromegas) and STG (sTGC). The top node of both MMG and STG will propagate its state and receive commands from the ATLAS overall DCS. An overview of ATLAS MUO DCS structure with NSW DCS integration and brief structure of the sub-detector node structure is displayed in Fig. 8. The overview of the NSW structure and project/server allocation is displayed in Fig. 9.

ELECTRONICS CONTROL STATION

System Setup

The electronics system setup will consist of 28 FELIX servers, 12 for MMG and 16 for STG accordingly. The FELIX-SCA OPC UA Server granularity will be 1-to-1 meaning that we will have 1 SCA OPC UA Server per sub-detector sector. An example is illustrated on Fig. 10.

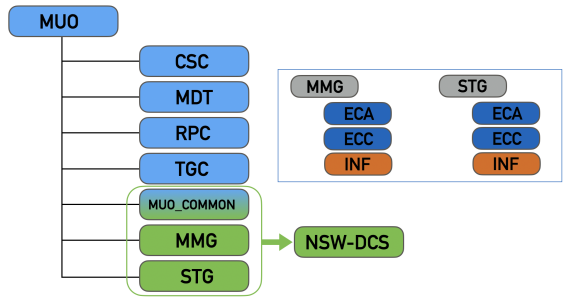

Figure 8: The overview of the ATLAS MUO DCS structure with NSW DCS integration and brief structure of the sub-detector node structure.

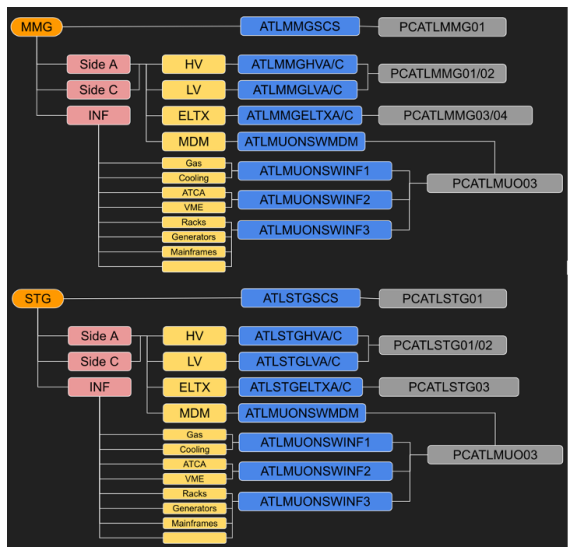

Figure 9: The overview of the NSW structure and project/server allocation.

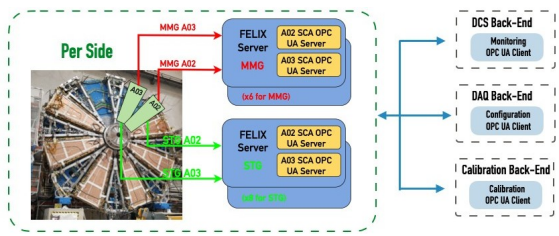

Figure 10: An illustration of the FELIX-SCA OPC UA Server granularity mapping.

For the system operation, automated sequence has to be settled up on the FELIX machine in order to perform the GBT e-link configuration, the FELIX API initialisation and the SCA OPC UA Server automatically in the FELIX machine boot.

Configuration

The NSW is a fully autonomous trigger and tracking detector system, adequately supported by an advanced electronics scheme and ready to handle the challenges of increased instantaneous luminosity at the High Luminosity LHC. It

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includes more than 60k front-end ASICs and a few tens of FPGAs, which need to be configured before every run of the experiment. This process needs to be efficient and quick, since it needs to happen a few times per day. The main ASIC to be configured is the VMM, the front-end signal pre-processing chip that can readout 64 channels. A few kbytes of configuration data include thresholds for each channel, but also global registers to define the gain, time-to-amplitude conversion and many others. For this procedure we need to use the SCA's SPI master to communicate with the 8 SCA's SPI slaves in the VMMs. Also, the SCA's GPIO interface is required, to act as an enable signal. Moreover, a similar scheme using the SCA's I2C interface is used for configuration of the TDS chip, which is used for timing and trigger.

Calibration

The calibration procedure consists of various timing and charge calibrations of the front-end electronics. Gain calibration is done by varying the signal input using the internal pulser of the chip. A specific configuration file needs to be loaded on the VMM chips, which is done with the SCA. Calibration of a time-to-amplitude converter is done by skewing the input clock, which is performed by re-configuring the specific on-board with different settings. Baseline and noise level is defined by reading out each channel output with the ADC when no collisions are occurring.

Monitoring

Due to its complexity and long-term operation, the ATLAS detector requires the development of an advanced DCS for the electronics monitoring using the SCA chip, which is installed on the 8000 front-end boards of the NSW. The use of such a system is necessary for the safe operation of the detector as well as to act as a homogeneous interface to all the sub-detectors and the technical infrastructure of the experiment. This system gives us the ability to monitor more than 100000 parameters which include all the power/temperature sensors, on-chip temperature and information, which are connected to the SCA on all the front-tend boards of the NSW. In order to achieve the electronics monitoring via the FELIX-SCA and the SCA OPC UA server chain some steps must be performed in advance. The first step is the creation of the SCA OPC UA Server XML file, which the various sensors connected to the SCA ADC channels are specified. Then, the second step is the initialisation of the FELIXcore and the SCA OPC UA Server, services which are running into the FELIX machine. The third step is the subscription to the SCA OPC UA Server via a WinCC-OA OPC UA Client. Then, another step is the creation of the SCA OPC UA Server XML items into DPEs inside the WinCC-OA. And finally, the monitor of the board parameters is accessible via the SCA electronics control station . The electronics control station has been developed, following the existing look, feel and command architecture of the other Muon subsystems, in order to facilitate the shifter/expert operations. It is mapped onto a hierarchy of Finite State Machine (FSM) elements using the toolkit. For each individual layer, a main panel has been developed, providing the user with useful information, reflecting the state and status of the detector, its vitals displayed in trendplots; while a secondary panel provides supplementary details. A general view of the graphical user interface of the top FSM nodes and their constituents is shown in the Fig. 11 and Fig. 12.

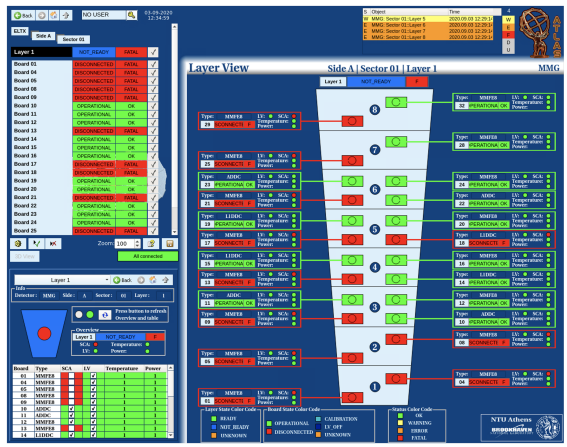

Figure 11: The interface of the Electronics control station and in particular the layer view of the sector which user can navigate and see in a glance the electronics status.

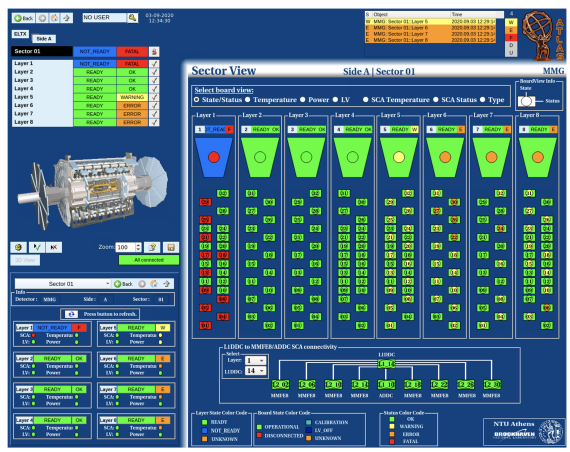

Figure 12: The sector view of the Electronics control station.

Each board's monitoring and conditions can be displayed on the panel. The state and status of the board depends on the status data point element of each board's temperature and power sensors and the communication validity of the SCA OPC UA server. The projects were validated through daily usage from shifters in the commissioning site at a first stage and then through the NSW control in ATLAS Control room.

DCS-DAQ Interaction

As already mentioned above, DCS, calibration and configuration share the common SCA OPC UA Server path for the SCA. Although, the front-end boards which are equipped with the VMM, are using the same SCA ADC input channel

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for both monitoring and calibration purposes. During the Physics run, the VMM monitor output is equivalent to the VMM temperature but during the Calibration run, the VMM monitor output will display the baseline measurement which is used for the board noice calibration measurements. Thus, during calibration run, VMM shows fake temperature values so a interface plugin between DCS-DAQ should be implemented in order to prevent the DCS to trigger several alarms and warnings. The solution found via the common SCA OPC UA Server and the FreeVariable status which is mainly a user defined OPC-UA item which can be controlled and monitored both by DCS and DAQ back-ends applications. Thus, during the Calibration run, the DCS will monitor the configuration status for this specific VMM of the FEB and the alarm will be disabled corresponding FEB's VMM, as shown in Fig. 13. In addition, more DCS-DAQ interaction tools are on-going in order to monitor the FELIX status, the GBTx alignment information and various FELIX infrastructure parameters.

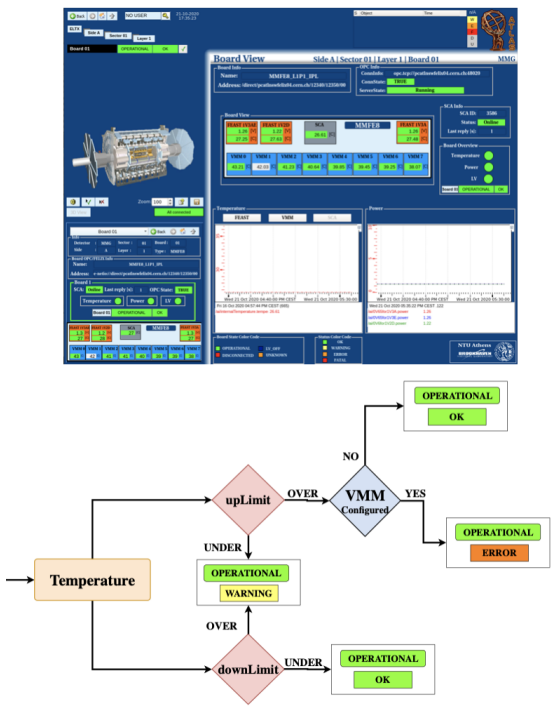

Figure 13: Top: Overview of the board panel of the electronics control station which shows the VMM temperature alarm disabled using the configuration status of the FEB's VMM via the SCA OPC UA Server. Bottom: A flow chart of the logic for the status and state definition based on the VMM temperature and the configuration status.

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