HEIDELBERG UNIVERSITY HOSPITAL

Heidelberg Ion-Beam Therapy Centre

Major Upgrade of the HIT Accelerator Control System Using PTP and TSN Technology

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OUTLINE

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- The motivation for a major upgrade
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The Heidelberg Ionbeam Therapy facility

Dedicated Accelerator complex for tumor treatment with:

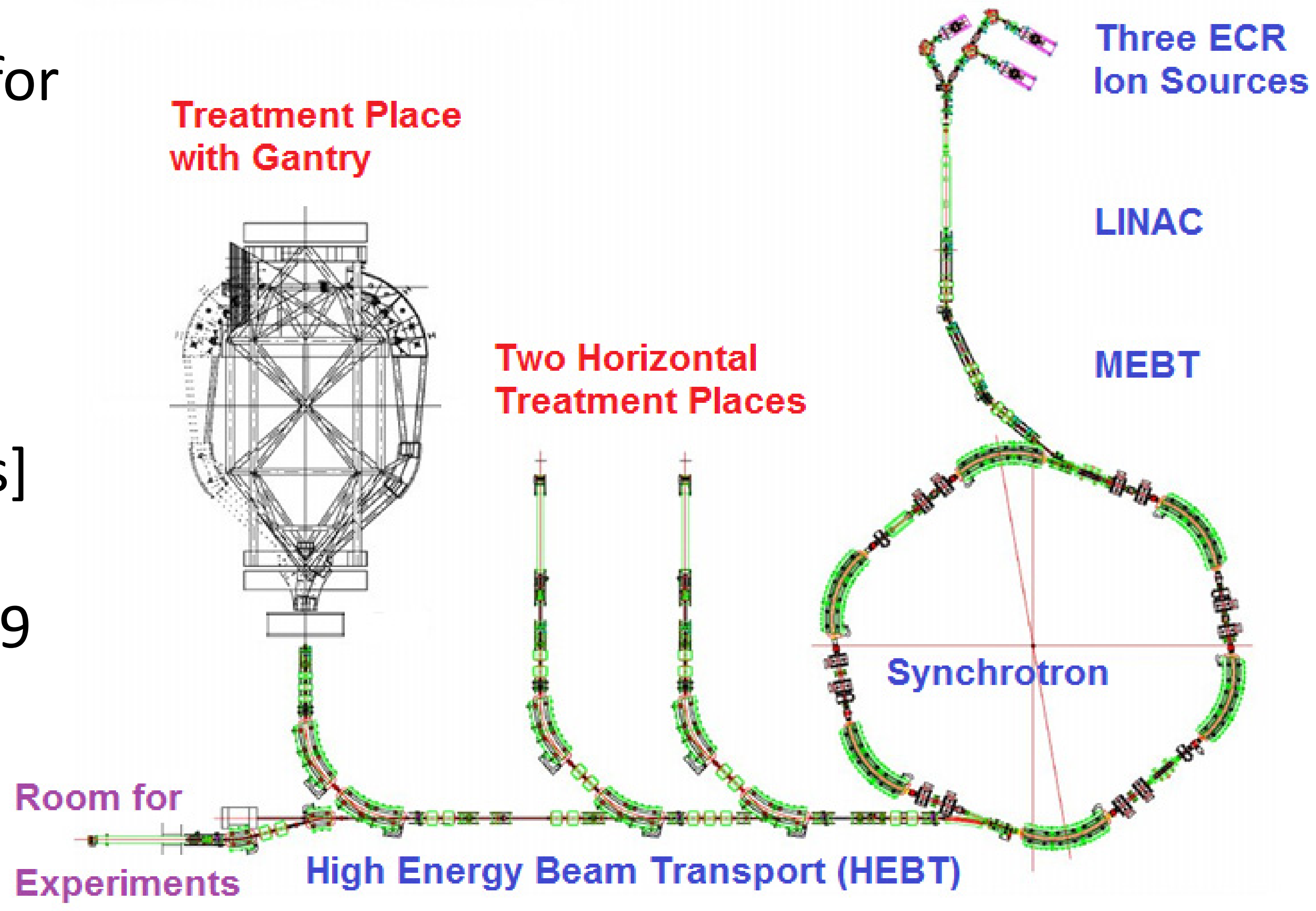
- p and He beams up to 230 MeV/u
- C beams up to 430 MeV/u

[higher energies for experiments]

Patient treatment started in 2009 (Gantry: 2012)

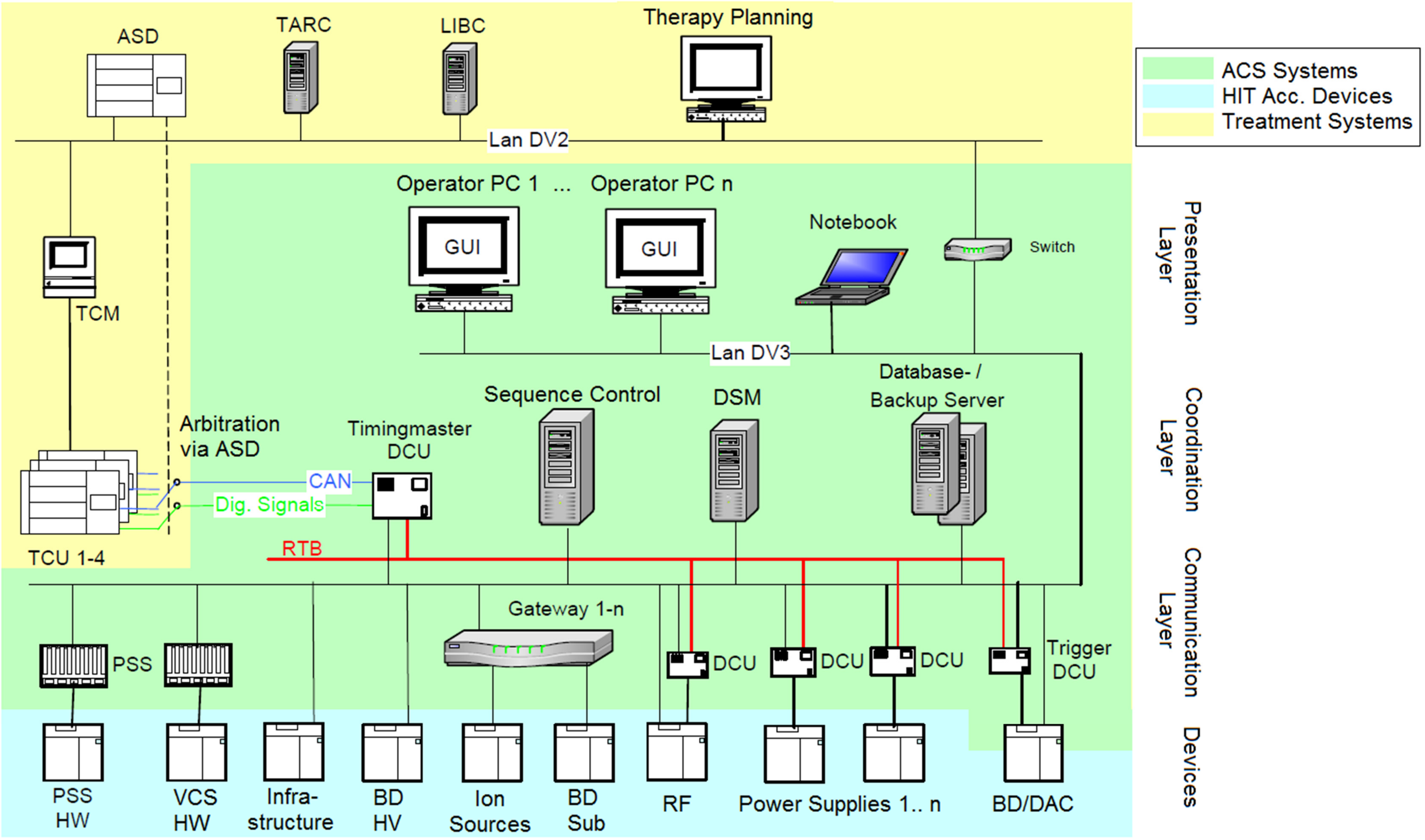
Currently ~ 700 patients/year

Total: ~ 5700 Patients treated



Current HIT ACS and its timing system (I)

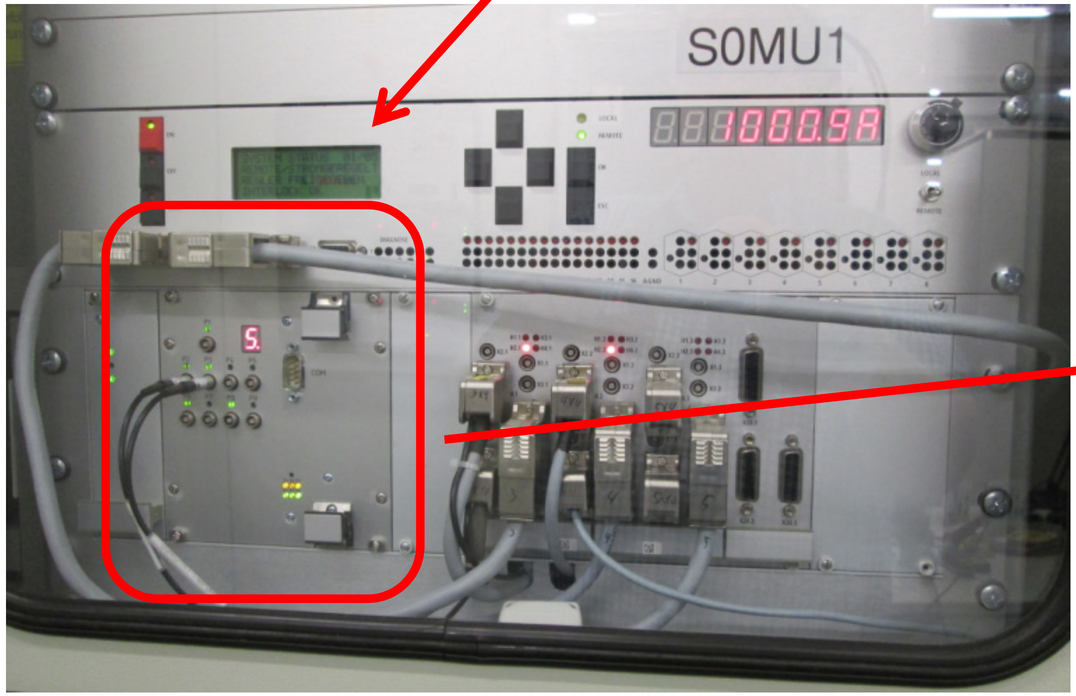
During treatment the therapy control system (TCS, yellow) sends commands via CAN bus to the ACS (green), which next accelerator settings should be carried out – safety is assured by redundancy , checksums, etc.

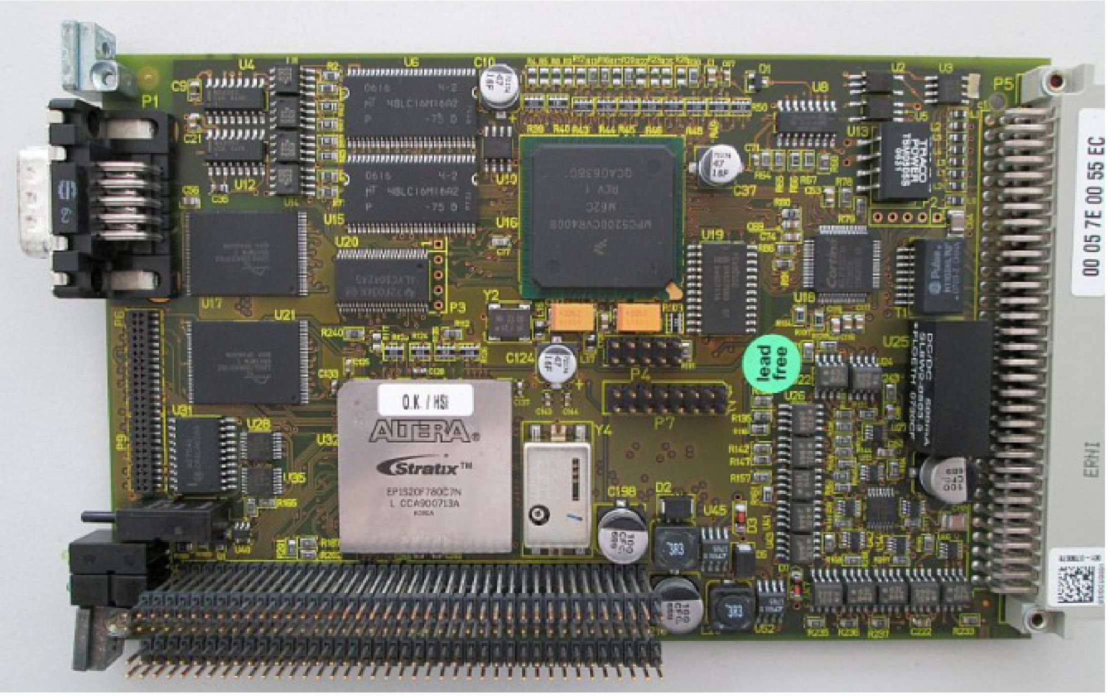


Current HIT ACS and its timing system (II)

Main Power Supply Room

Device Control Unit (DCU) – designed 2003:
MPC5200 processor, proprietary OS;
Altera Stratix FPGA for device type specific control firmware and timing access;
Timing via proprietary timing bus (RTB)





One DCU per power supply!

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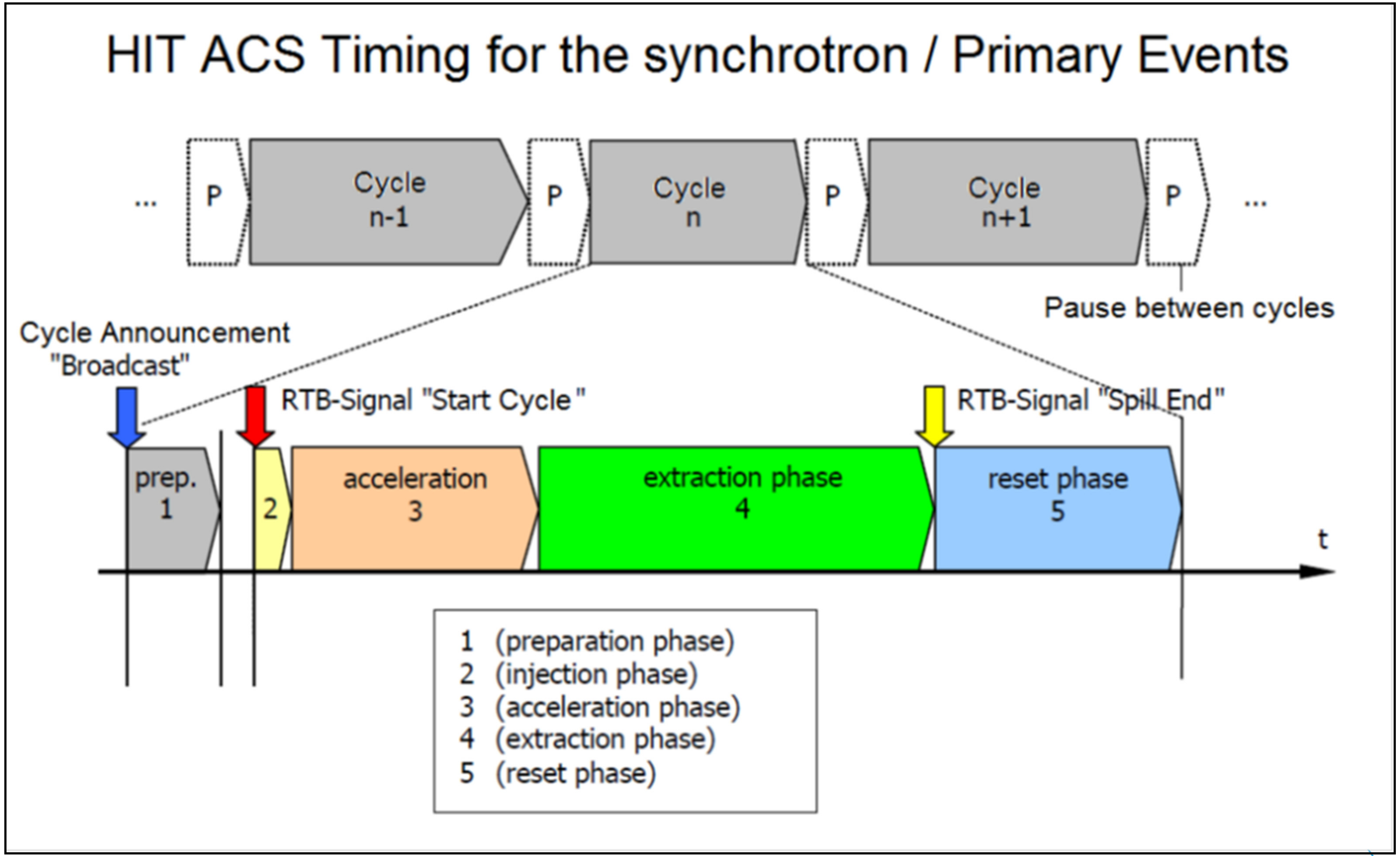
Current HIT ACS and its timing system (III)

RTB realized by Cat5 cable carrying primary events (HW signals):

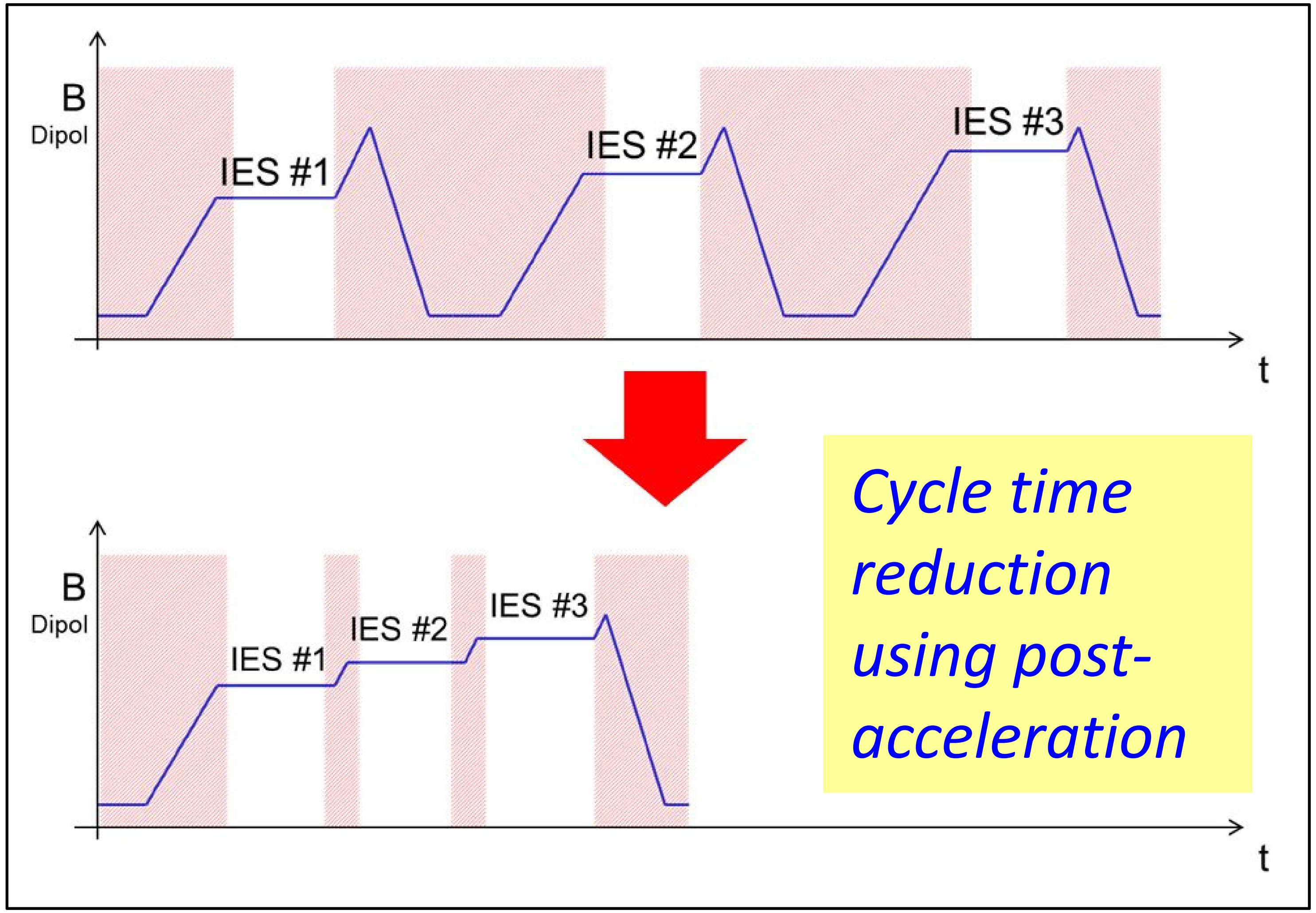
- Synchrotron Cycle Start
- Spill Pause (Gate)
- Spill End
- (Master Clock)

Specified timing precision: +/- 1 µs
Reached timing precision: +/- 10 ns
(by runtime adjustment of RTB between DCUs)



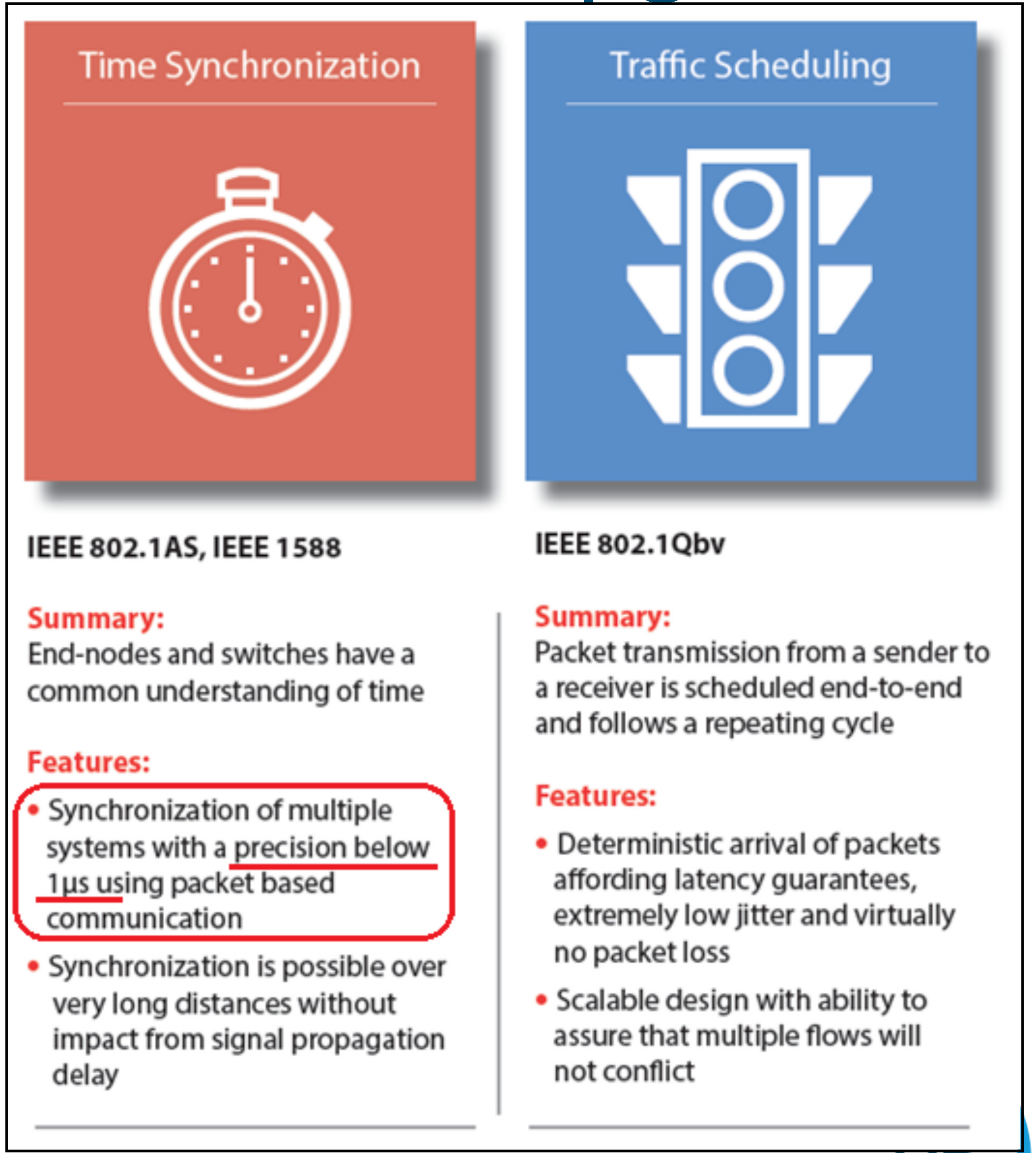
The motivation for a major upgrade

(1) More and more ACS components get obsolete, new DCU generation necessary
(2) New functionalities for higher efficiency of the facility needed – so-called "multiple energy operation" scheme → This will cause higher complexity of the ACS and more flexibility in the timing!
(3) Increase reliability → reduce cabling and connections ("one-wire-ACS"); use of deterministic Ethernet protocols; avoid proprietary solutions, use actual and "good" standards from industry!



PTP and TSN - A solution for the HIT ACS upgrade?

- From Standard Ethernet (IEEE 802.3) to *Time Sensitive Networking* (TSN): Introduction of real-time communication with hard, non-negotiable time boundaries for end-to-end transmission latencies;
  → "deterministic" Ethernet
- Synchronization of the clocks of all network-linked controllers by distribution from one central time source directly through the network
- Basis is the IEEE 1588 Precision Time Protocol (PTP), which utilizes Ethernet frames to distribute time synchronization information → IEEE802.1AS
- If all clocks of the ACS are synchronous within less than 500ns, the primary events (HW) can be replaced by Ethernet commands with time triggers (SW)



PTP and TSN - A solution for the HIT ACS upgrade?

Questions to solve:

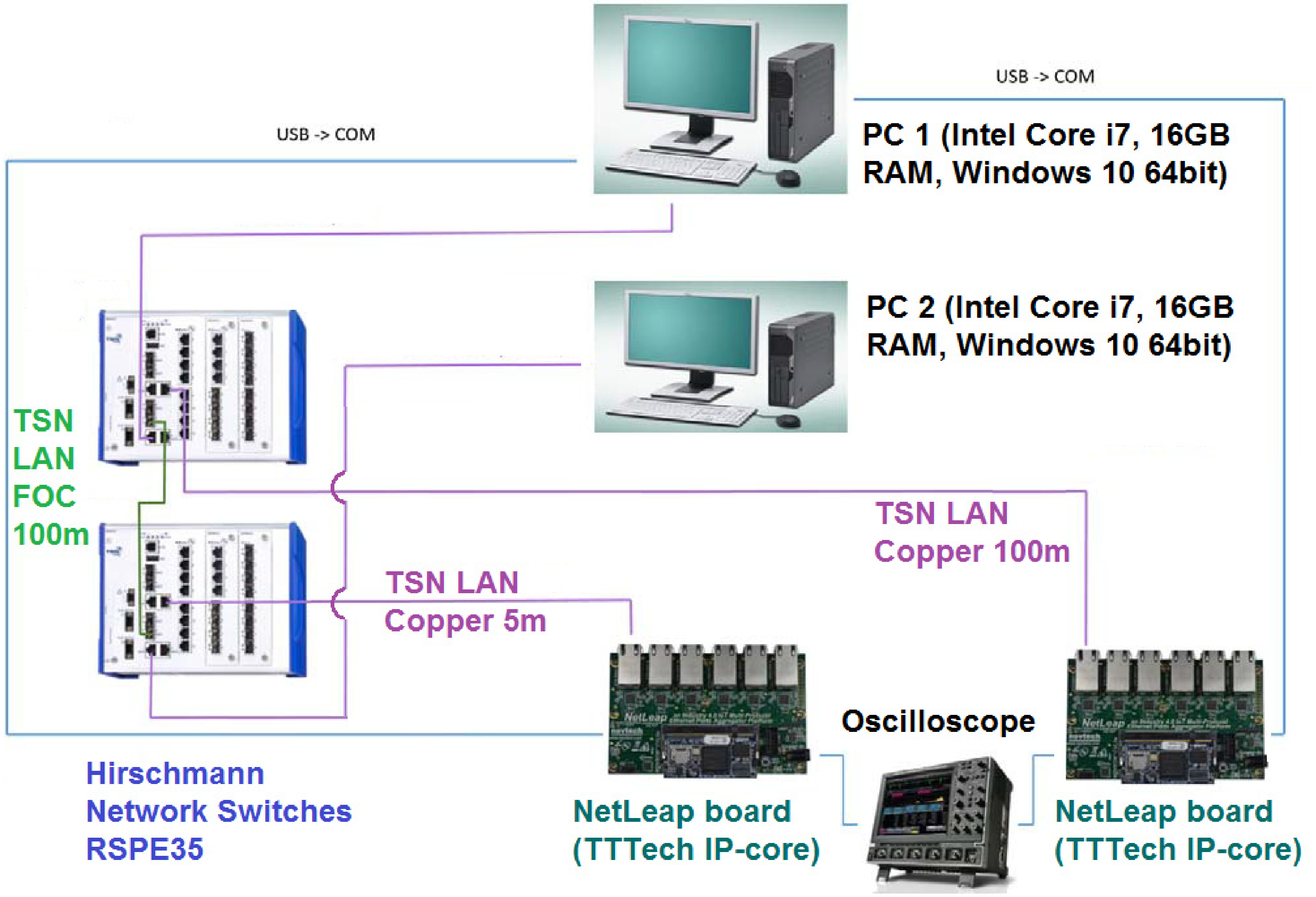
- Will this technique be available in near future? → ***Yes***, big boost by automotive market! Lively community:
- Are there components available to test the features and promised performance? ***Yes***, here a short list of
  - ➢ Network Switches: Hirschmann/Belden RSPE35, Cisco IE4000, …
  - ➢ Embedded Controllers: MitySOM, NovPek, NetLeap, …
  - ➢ Grandmaster clocks: Meinberg microSync, …

First timing measurement results from a test bench

- Test bench designed as realistic as possible – along the HIT ACS conditions!
- Therefore distances comparable to the HIT building are assumed, 100m from switch to switch using fiber optic cable (FOC) and 100m copper cable to connect embedded controllers (worst case).
- In the existing ACS 100 Mbit/s network, the load is ~5% with bursts up to 10% (normal “cyclic” operation), the TSN LAN is a 1 Gbit/s network, the load is estimated to only double in the next generation ACS.
- First test: Compare clock synchronization precision of two embedded controllers across the network with optional additional network load by two PCs. Grandmaster clock activated on one of the switches.

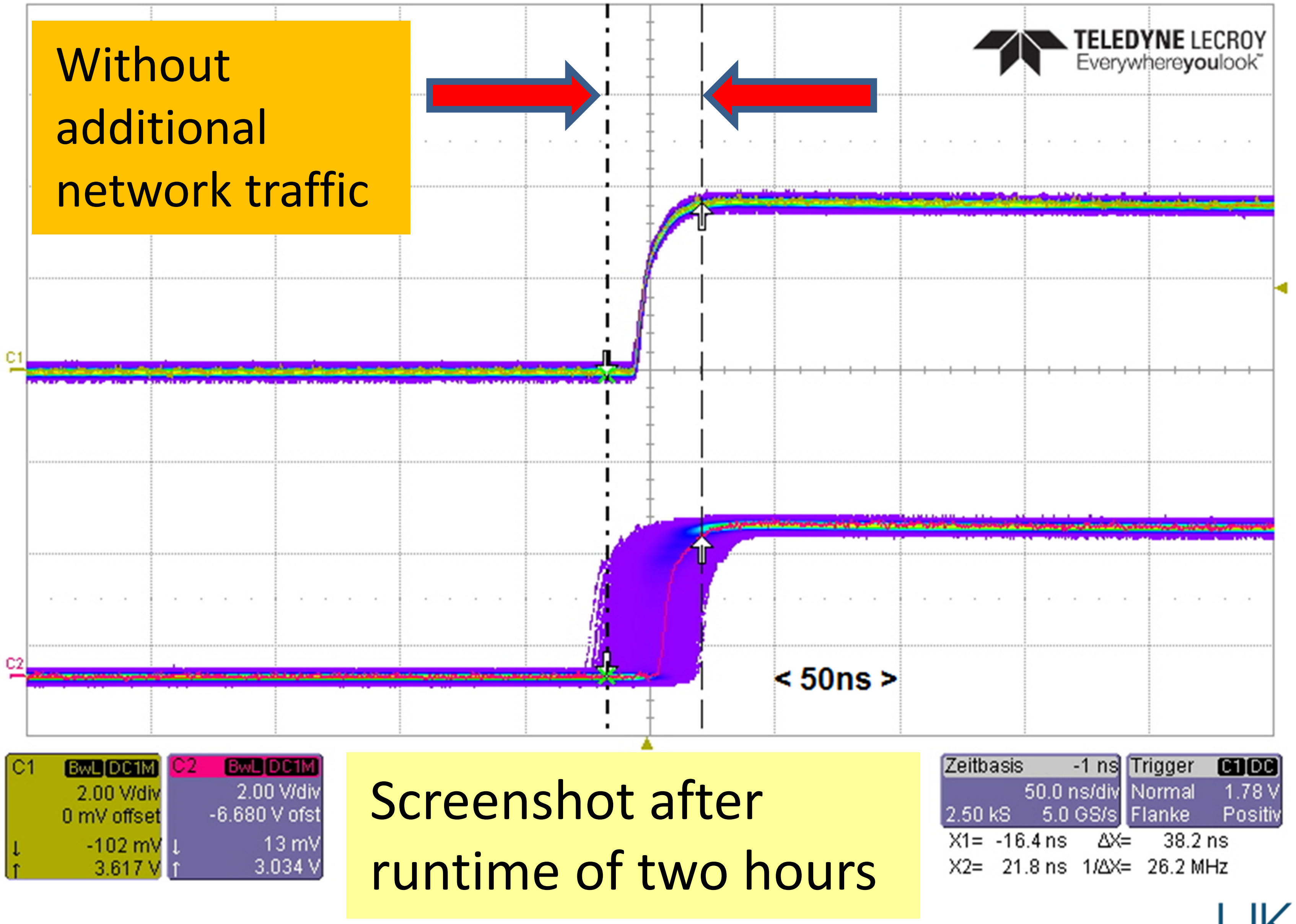
First timing measurement results from a test bench

- NetLeap Evaluation boards are equipped with NOVSOM®CVL Intel Cyclone V SoC, which contain a dual-core ARM Cortex-A9 processor system with FPGA logic on a single chip
- RT-Linux is used in the ARM cores, the TSN/PTP stack is implemented in the FPGA logic, these are commercially available from *TTTech* or *CAST*



First timing measurement results from a test bench

- For the exact measurement of the time jitter the signals „Pulse per second PPS“ of both boards were connected to an oscilloscope.
- Additional network traffic using ftp and Iperf does not change the result significantly
- Clocks of both controllers are running synchronously within less than +/- 25ns! A factor of 20 below the necessary precision!



Summary and Outlook

- HIT ACS timing constraints are satisfiable using TSN/PTP; IEEE802.1AS-REV (still *Draft 8.1*) will introduce improved time measurement accuracy in addition.
- Thus the "one-wire-ACS", based on components available in industry, seems possible – check with more embedded controllers in the network still due.
- Other TSN features like scheduling and traffic shaping (IEEE 802.1bv) as well as frame pre-emption technology (IEEE 802.1bu) will also help to make the ACS network traffic more secure and reliable.
- All components to be used are commercially available today or in near future and based on industry standards (HW, SW), only device interfaces remain proprietary.
- Existing FPGA firmware code can be transferred to Intel Cyclone SoCs.
- An implementation study of a TSN based HIT-ACS 2.0 is under way until Q1/2020 – the planned realization is scheduled from 2020–2022.