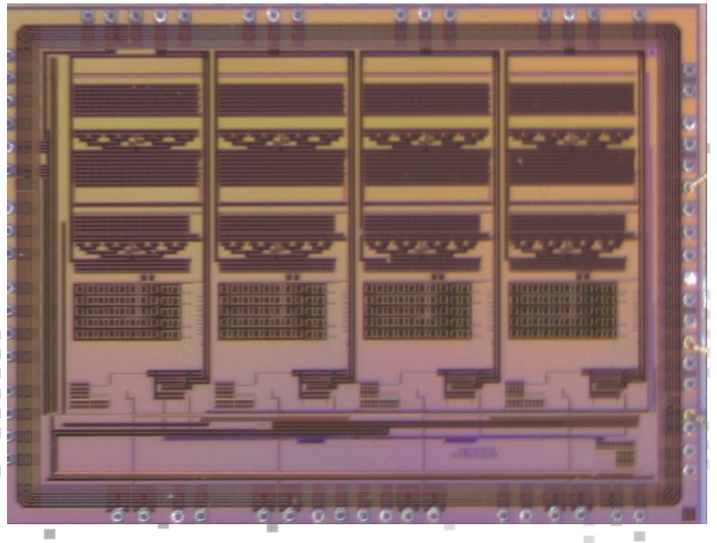

A 4-CHANNEL, 7ns DELAY TUNING RANGE, 400 fs STEP, 1.8ps RMS JITTER DELAY GENERATOR IMPLEMENTED IN A 180 nm CMOS TECHNOLOGY

F. Badets, G. Billiot, S. Bouquet, A. Spataro, A. Fustier, F. Lepin, B. Caillat, C . Magnier CEA-Leti
D.Monnier-Bourdin, B. Riondet, Greenfield Technology

OUTLINE

- Motivations
- Implementation
- Measurement results
- Conclusion

OUTLINE

- **Motivations**
- Implementation
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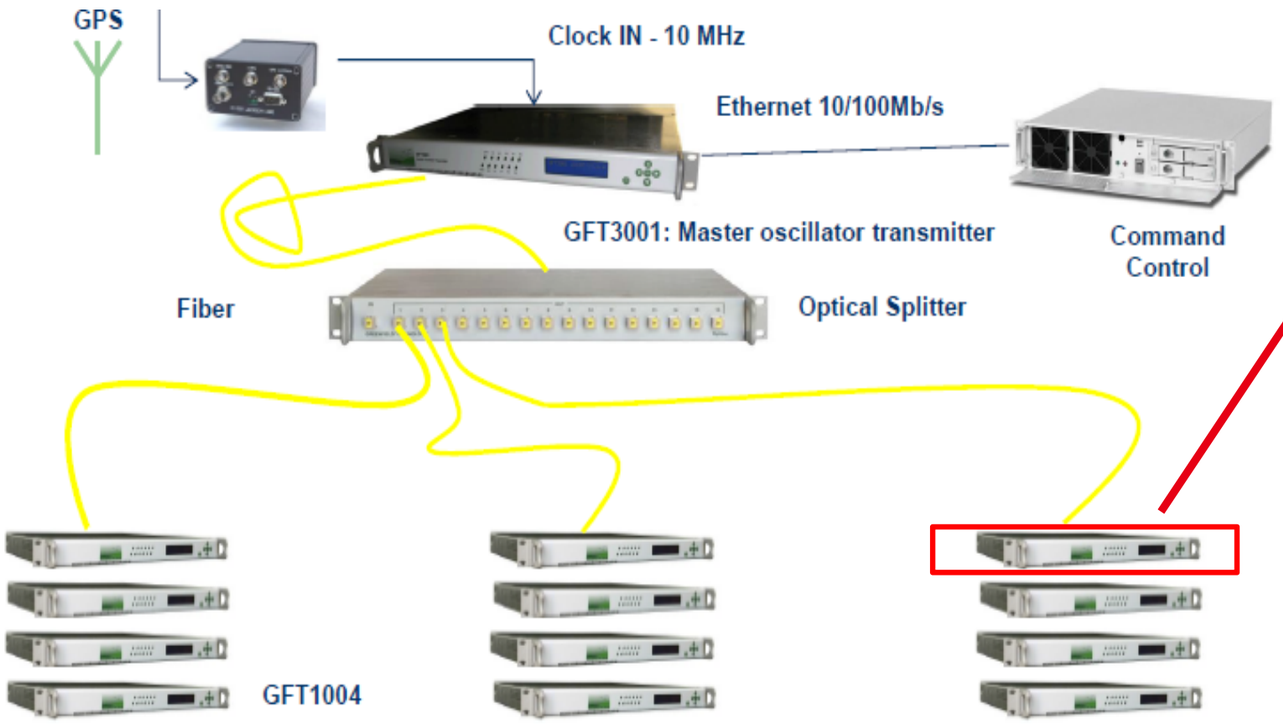
MOTIVATIONS



Greenfield Technolgy GT1000 timing system
for physics experiments
(100 to 2500 delay channels)

GFT1004 delay generator

Channels	4 (up to 10)
Resolution	1 ps
Jitter	10ps
Technology	Discrete components

GFT Next generation delay generator

Channels	>> 10
Resolution	< 1ps
Jitter	~ 1ps
New functions	Narrow pulses generation

Silicon integration of delay channels mandatory

EXISTING IC SOLUTIONS VERSUS ASIC DESIGN

Parameter	[3]	[4]	[5]	Unit
Delay Step	5	10	10	ps
Full Scale	5	5.6	10	ns
RMS jitter	1	-	3	ps
Pules repetition rate	1	1.5	1.2	GHz
Temperature drift	-	10	-	ps/°C
INL	30	40	20	ps

[3] Microchip (Micrel) SY89297U :

[4] OnSemiconductors B6L295:

[5] IDT 854s296i:

- **Few delay generator circuits**
  - Low jitter, good linearity
  - But limited time step and full scale

→ **Not compliant with physics experiment requirements**

- **ASIC design advantages**
  - Better fit of application needs
  - Allows performances optimization
  - Embedding dedicated functions

ASIC SPECIFICATIONS

Parameter	Value	Unit
Channels	4	
Delay Step	<1	ps
Full Scale	7	ns
RMS jitter	< 2	ps
Pules repetition rate	> 20	MHz
Master Clock Frequency	150 – 200	MHz
Temperature drift	<4	ps/°C
INL	<1	% FS

- **ASIC features**
  - 14-bit programmable delay shift
  - Independent activation/deactivation of each channel
  - LVDS / CML / LVEPCL compliant inputs
  - LVPECl clock input
  - On-chip resynchronization of input pulse
  - LVPECL output with trise and tfall < 1ns
  - 2 or 4 channels recombination for narrow pulse generation
  - Automatic calibration of delay full scale
  - Analog temperature sensor
  - SPI bus for R/W configuration registers

OUTLINE

- Motivations
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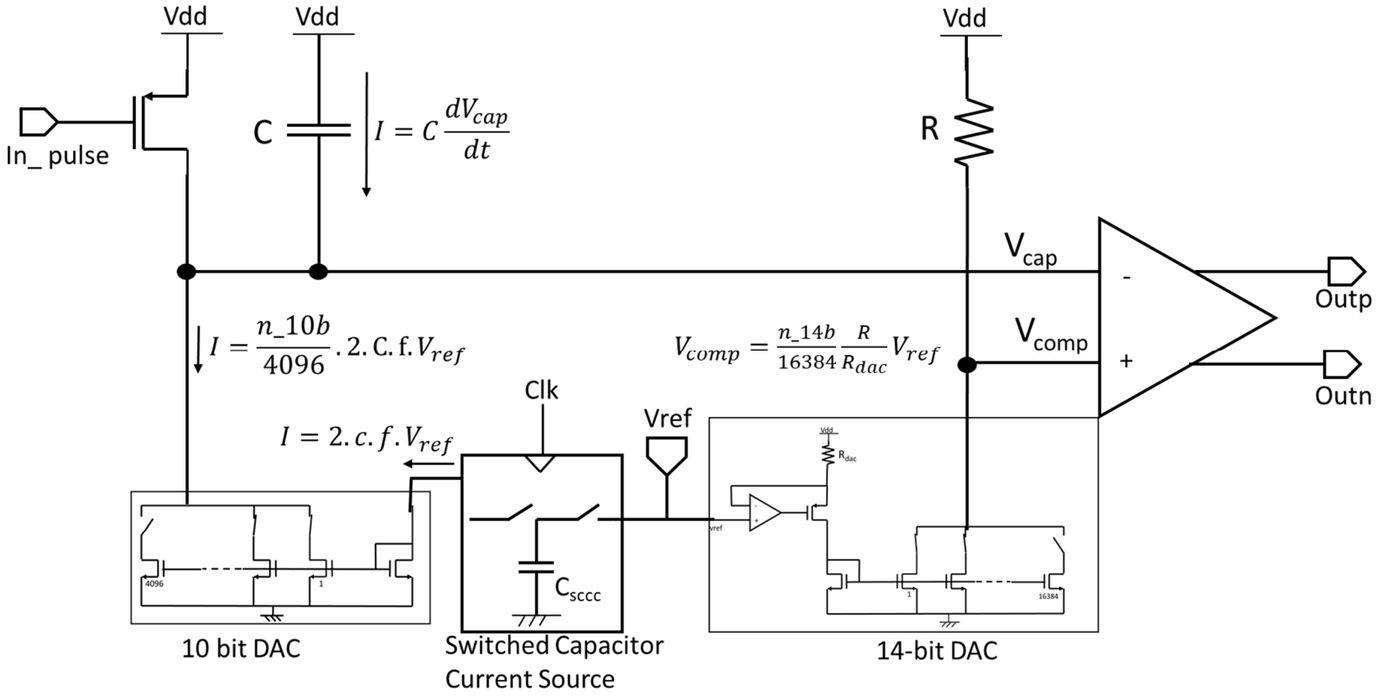
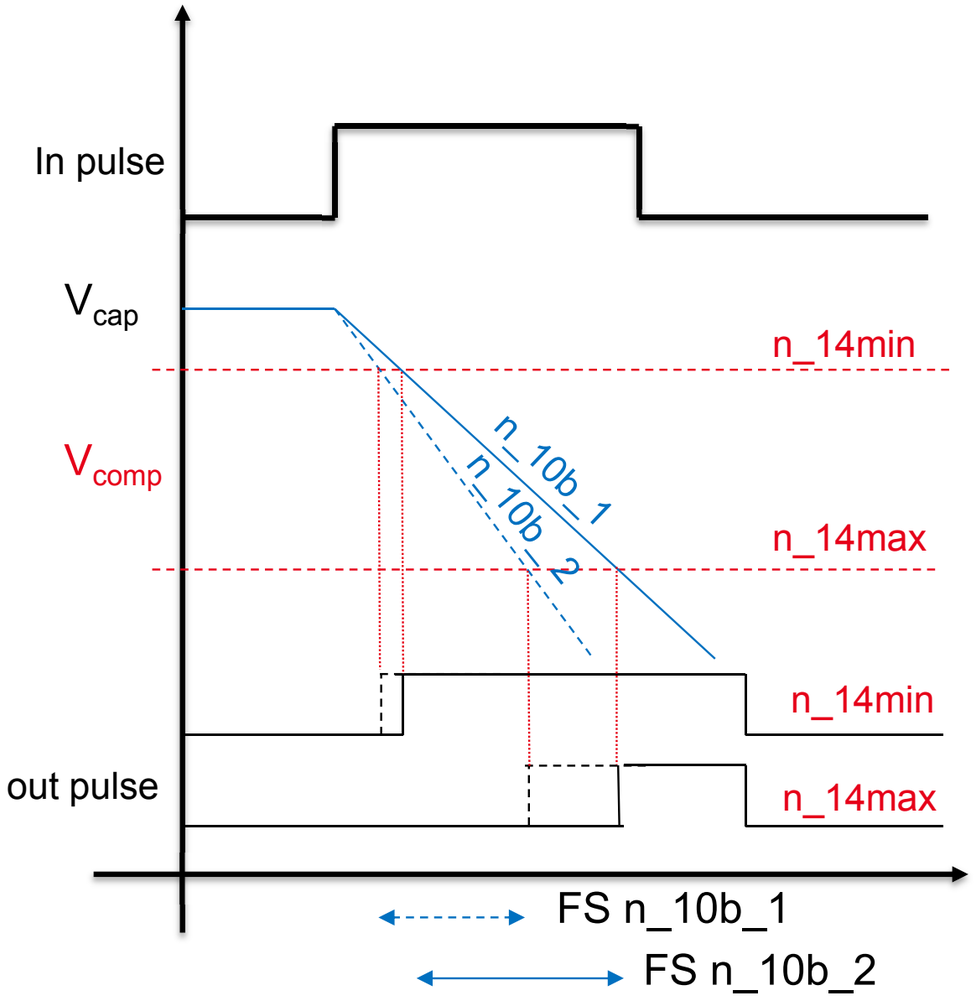
CORE DELAY GENERATOR



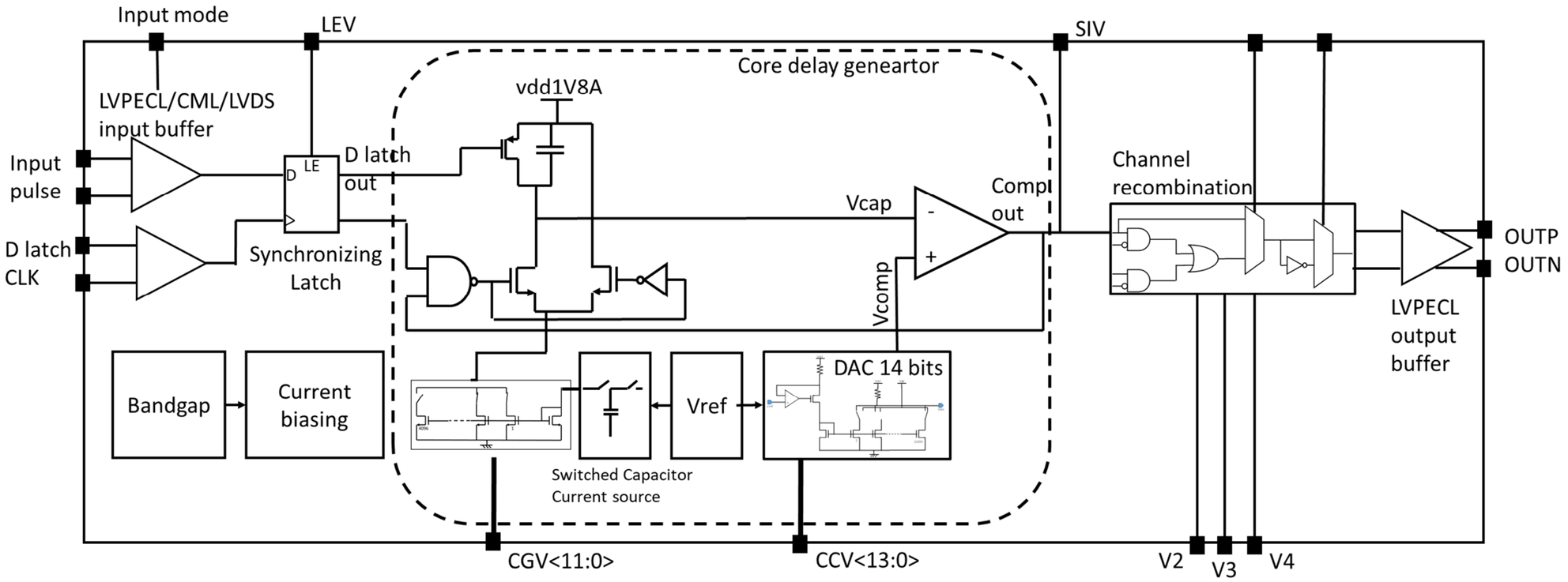


$$dt = \frac{1}{8}.\frac{n\_14b}{\_n\_10b}.\frac{R}{R_{dac}}.\frac{C}{C_{sccc}}.\frac{1}{f}$$

- **Delay depends on Resistor and Capacitor ratios**
  - Independent of temperature
  - Low varaitions versus process variations

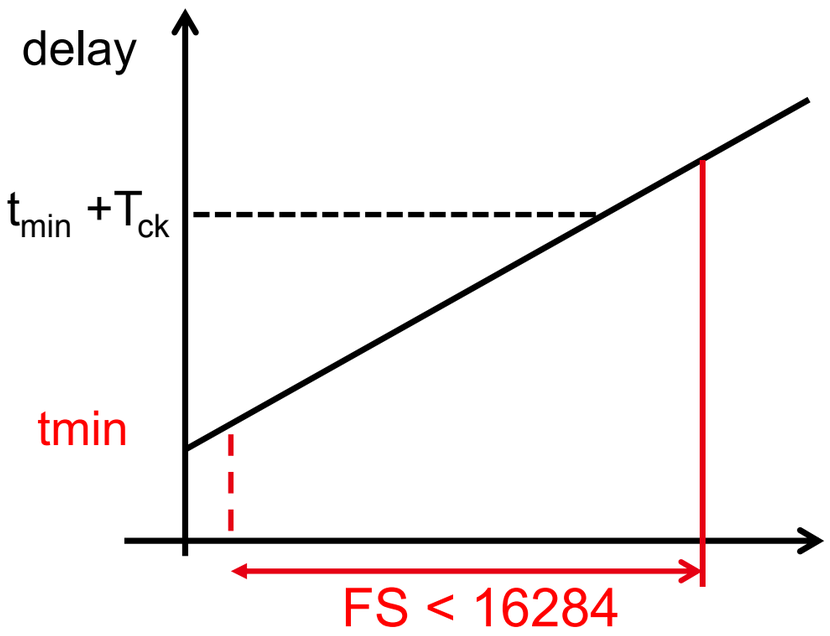
- **14-bit DAC controls delay shift**
- **10-bit DAC controls the slope**
  - Control of the full scale

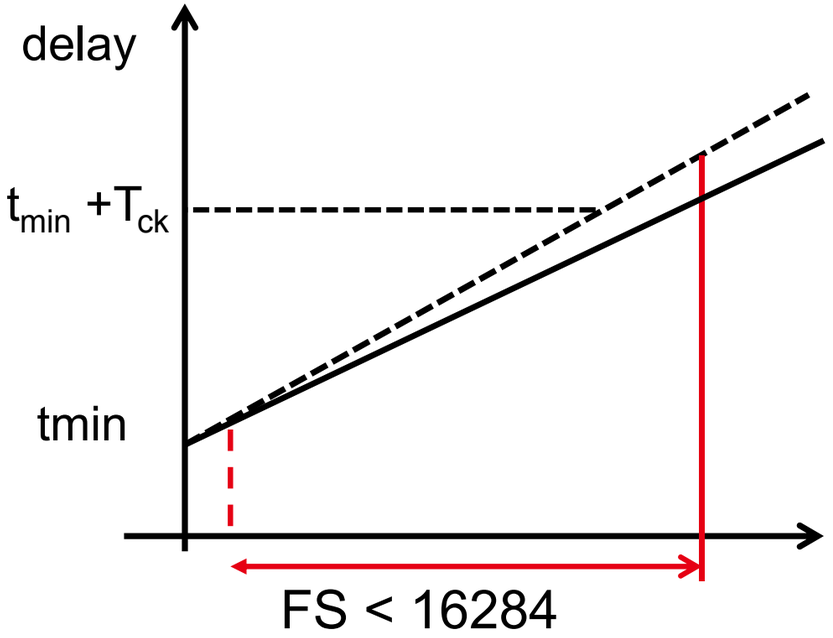
CHANNEL ARCHITECTURE



- D- latch :
  - Latch Enable : On-chip resynchronization
  - Latch Disable : differential buffer
- Channel recombination => narrow pulses generation
  - 2 channels : $Out_{ch1} = Out_{ch1} \& Out_{ch2}$; $Out_{ch3} = Out_{ch3} \& Out_{ch4}$
  - 4 channels : $Out_{ch1} = Out_{ch1} \& Out_{ch2} + Out_{ch3} \& Out_{ch4}$

AUTOMATIC CALIBRATION PRINCIPLE (1)





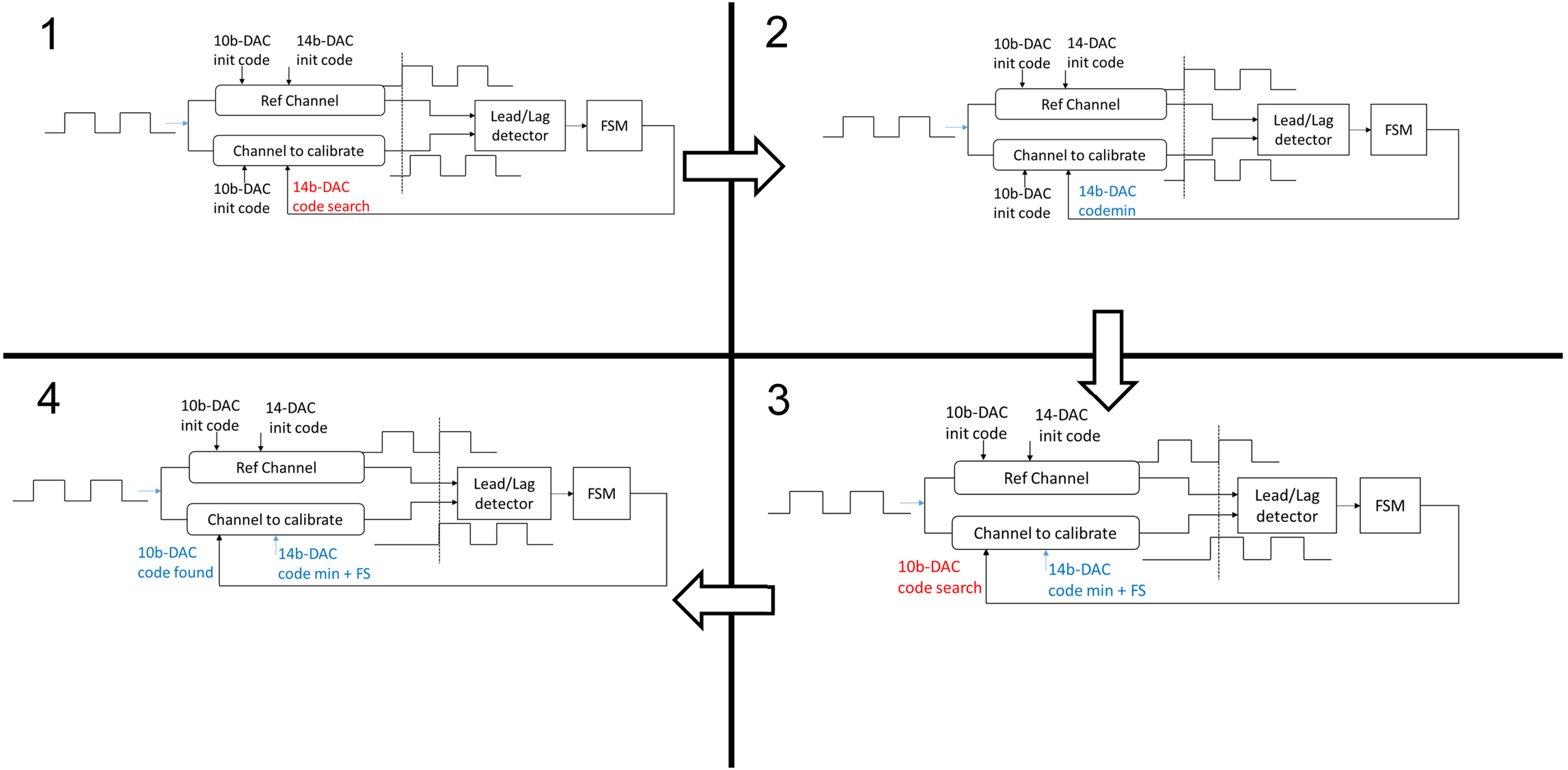
User sets:

- tmin (reference channel)
- FS code

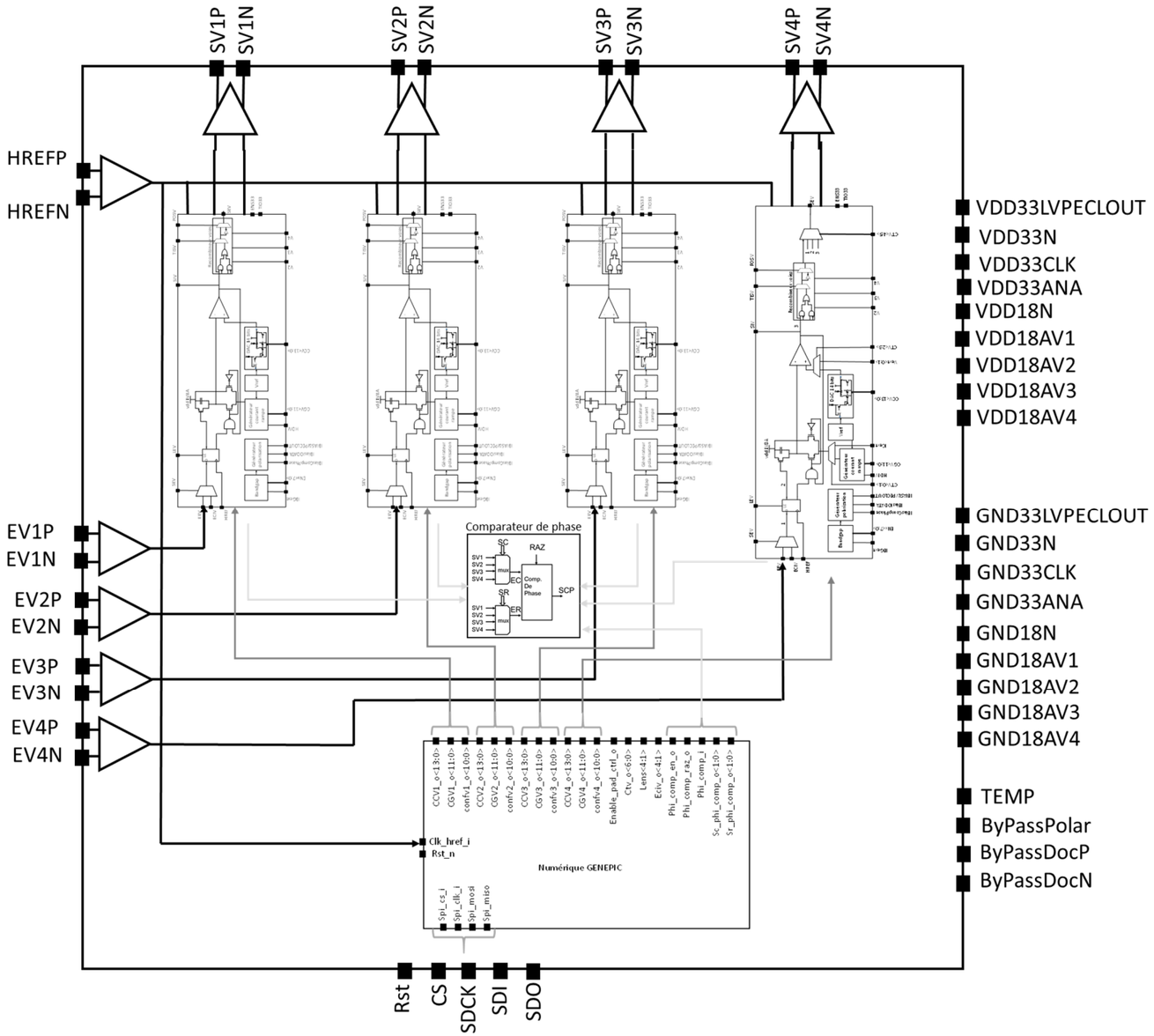
FSM adjusts:

- the code corresponding to min
- the slope of the channel delay range

AUTOMATIC CALIBRATION PRINCIPLE (2)



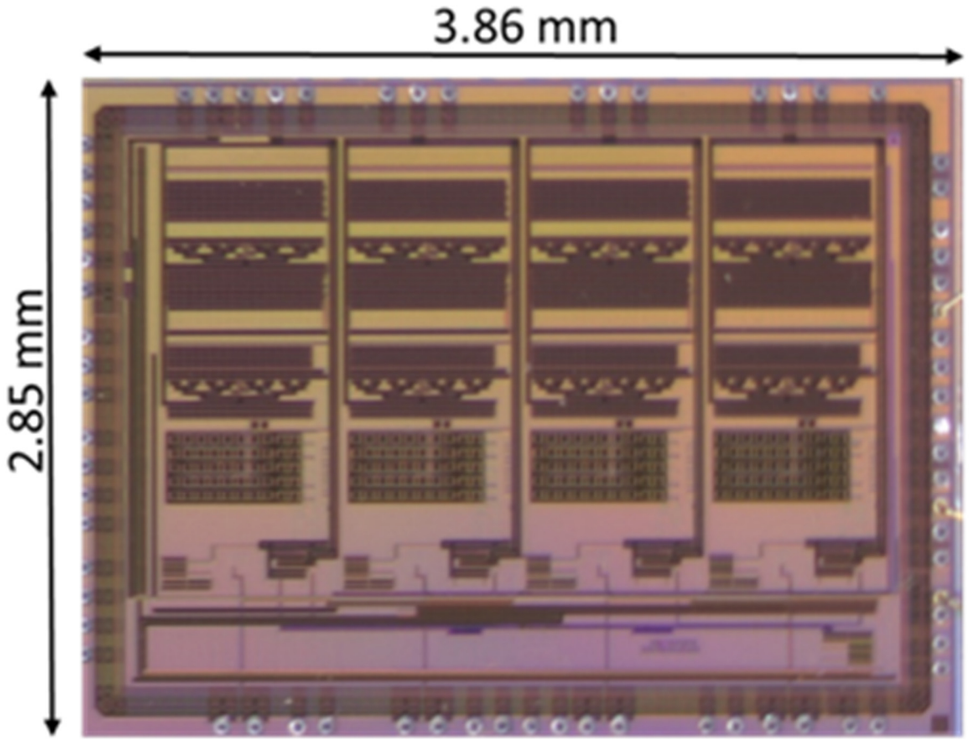
4-CHANNEL DELAY GENERATOR

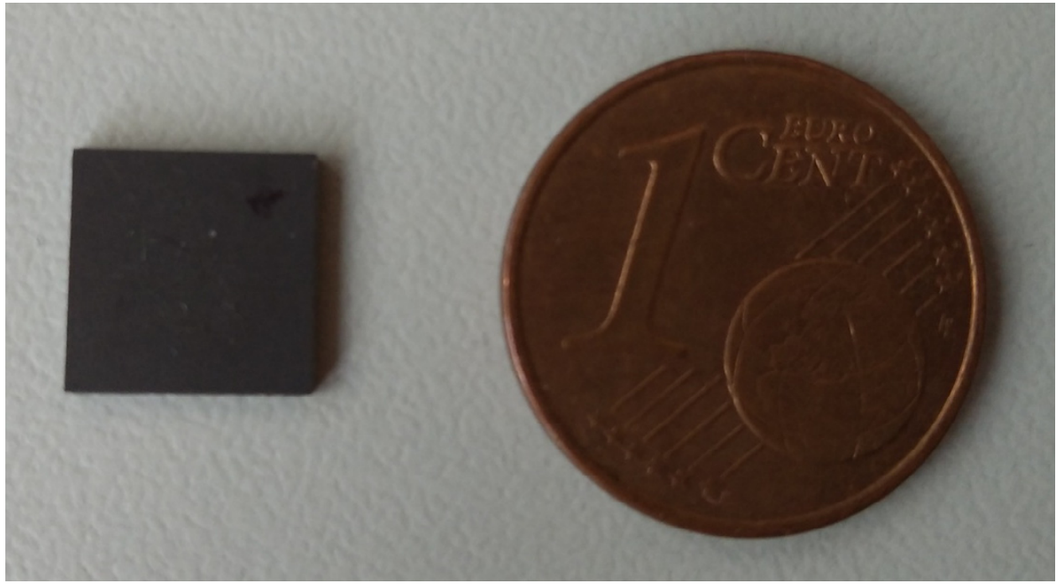


OUTLINE

- Motivations
- Implementation
- **Measurement results**
- Conclusion

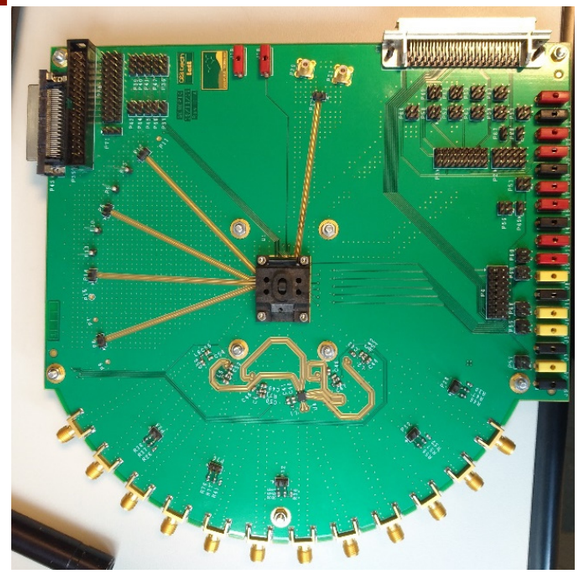
FABRICATED CHIP



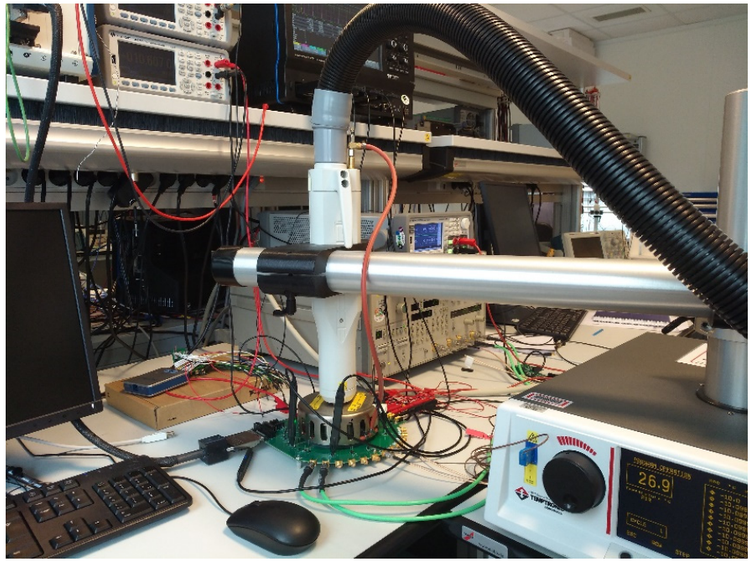


- Technology: CMOS 180 nm
- Area : 11 mm2
- Package : QFN 56 (8mm x 8mm)

TEST SETUP



- **Test board**
  - FR4 – 4 layers
  - 50 ohm lines
  - On board splitters for test automation
  - Dedicated socket

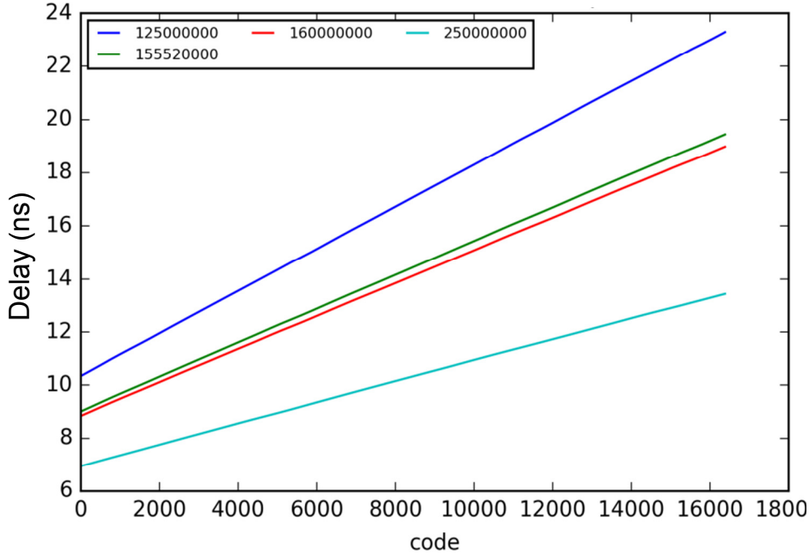


- **Test bench**
  - Thermostream ATS thermostat
  - Lecroy Waverunner 8404M 40 GS/s for accurate delay measurement
  - Anritsu MP1763C pattern generator => ultra low jitter input and clock generation
  - Keysight B2962A low noise power supply
  - Automatic test through Labview/Teststand

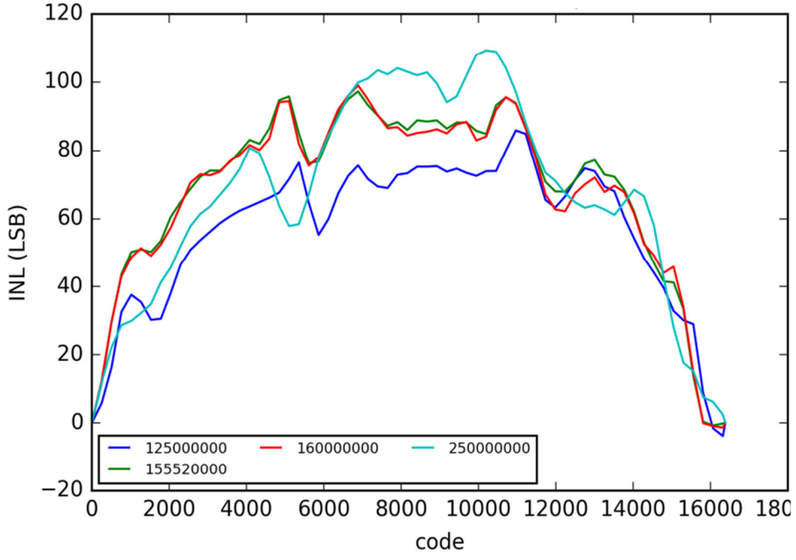
MEASUREMENT: NOMINAL CONDITIONS (30°C, 3.3V, 1.8V)

Before Calibration

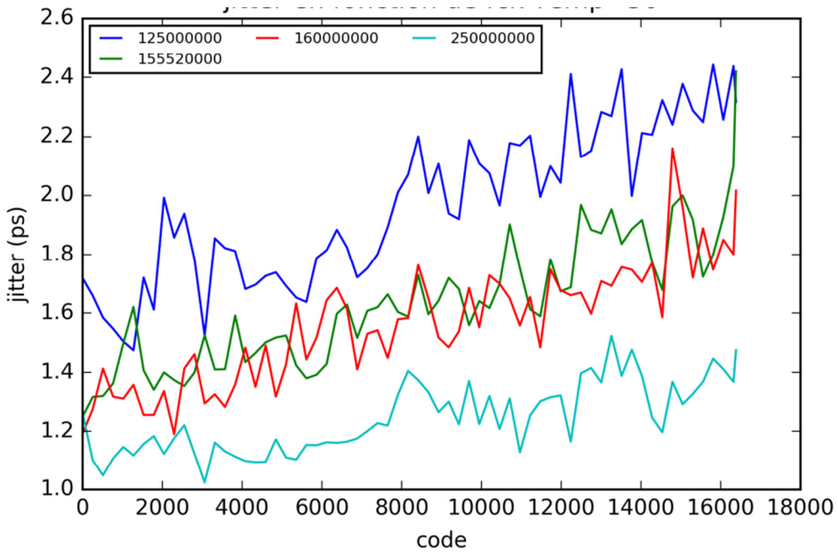
Delay



INL

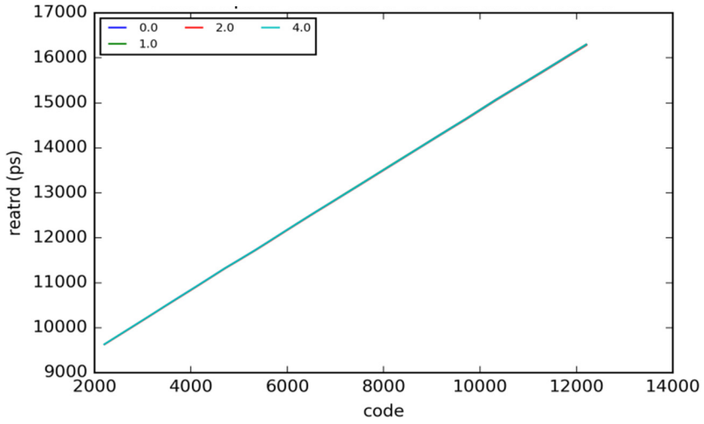


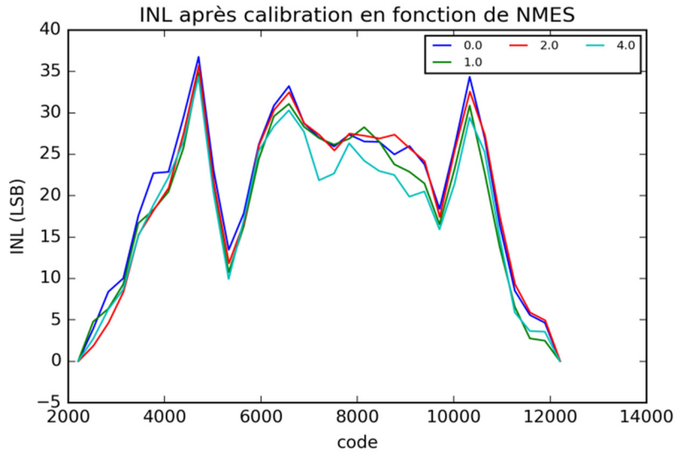
RMS Jitter



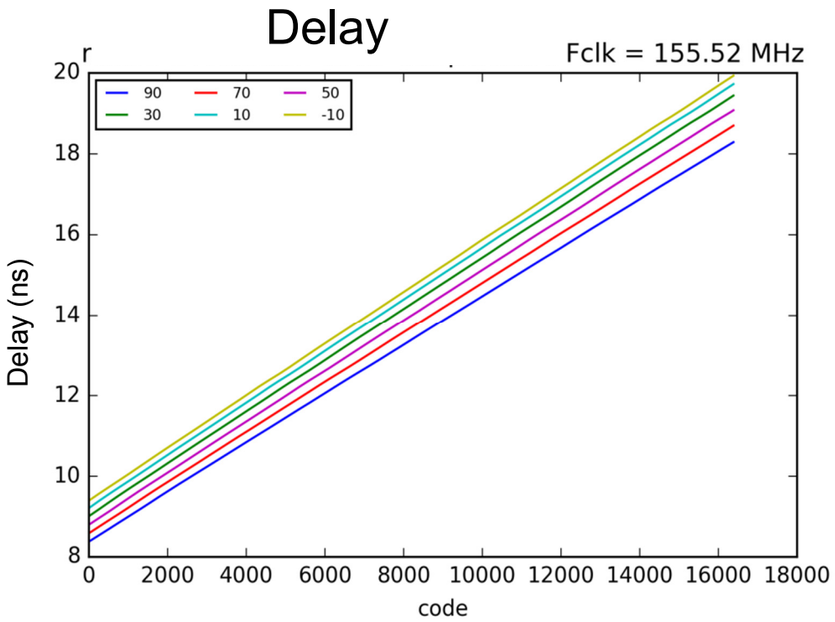
After Calibration

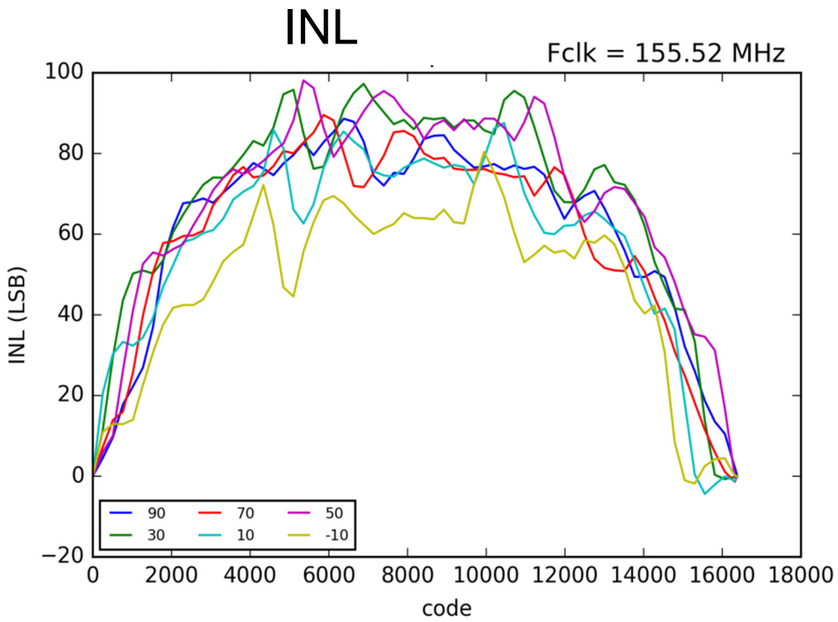
Delay

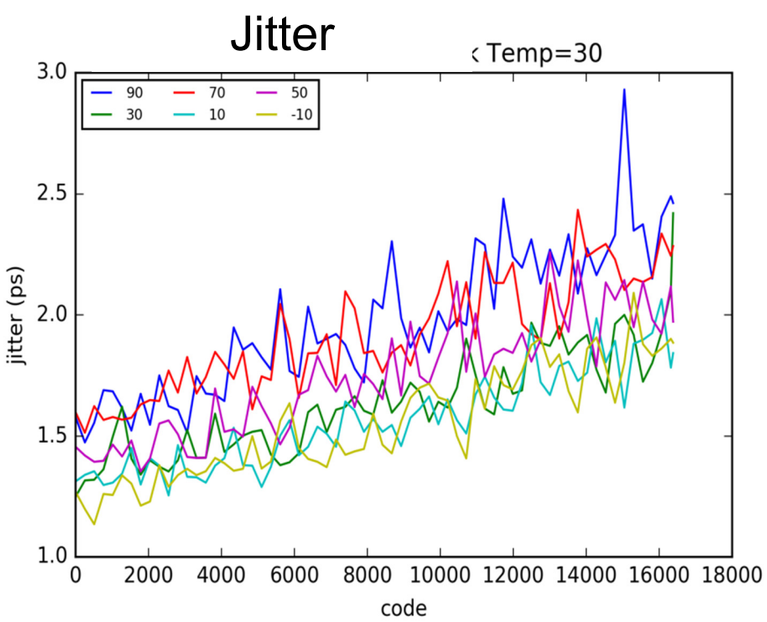




MEASUREMENT RESULTS: TEMPERATURE (-10°C / 90°C)

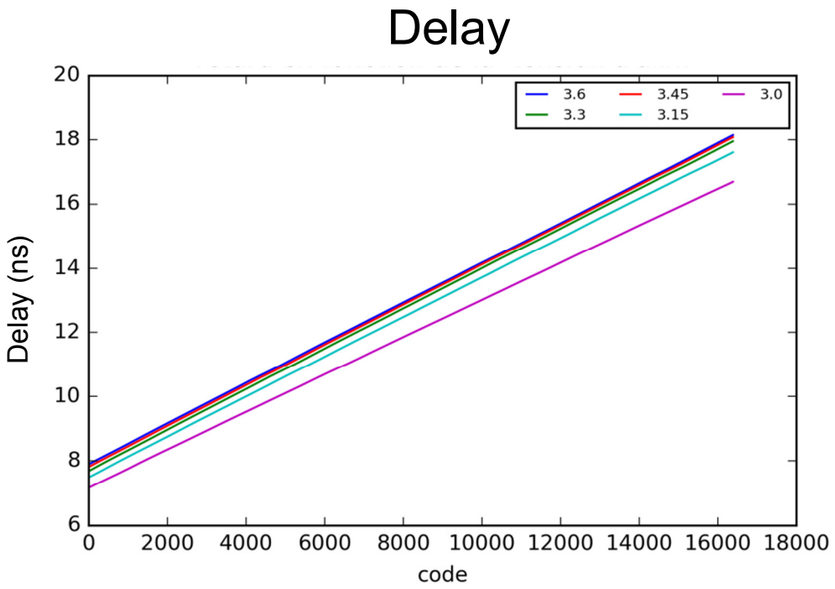


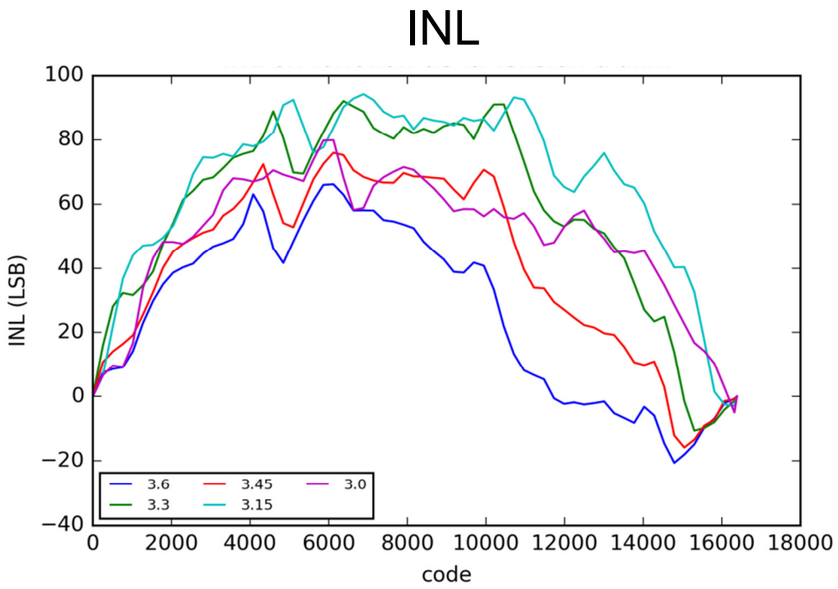


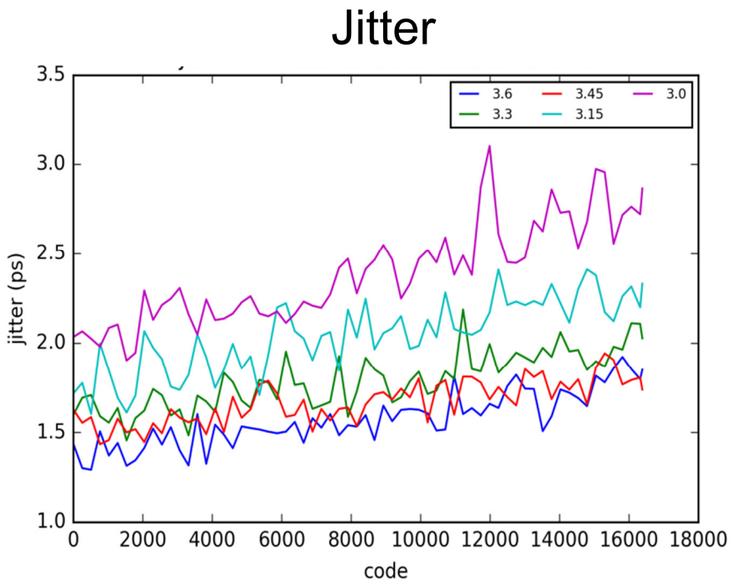


- **Temperature drift**
  - 8ps /°C test in socket
  - 2.5ps /°C when soldered on an application board

MEASUREMENT RESULTS: VOLTAGE SUPPLY (1.62 – 1.98 V, 3 – 3.6 V)







- **Degradation with lower supply voltage**

MEASUREMENT RESULTS SUMMARY

Parameter	Spec	simulation	measuremen	unit	comment
Power consumption 3V3		151	152	mW	
Power consumption 1V8		180	202.5	mW	
Puissance totale	500	331	355	mW	4 active channels
Fref Max	200	> 200	> 200	MHz	
LVPECL out Trise - Tfall	< 1	< 1	0.84	ns	
Input pulse min width			10	ns	> 2 * Tref
Input pulse repetition frequency	10	>20	>20	MHz	
Minimum output pulse width			2	ns	Recombination mode
Delay Full Sacle	Tref	> Tref	> Tref	ns	
Delay step	500	400	404	fs	après calibration, pour fclk = 150 MHz
INL	140	100	100	LSB	Before calibration
Jitter RMS	2	1.8	2.4 Worst case 1.8 typical	ps	Before Calibration
Insertion time	4n	5n	5.6n	s	Latch enable
Temperature Drift	4	1.5	8	ps/°C	over -10 / 90 °C
Diaphony			< 5	ps	
Temperature sensor slope		2	1.53	mV/°C	

OUTLINE

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CONCLUSION

- **4- Channel Delay Generator chip in low cost 180 nm CMOS technology**
  - 5 to 7 ns Full Scale
  - 1.8 ps typical RMS jitter
  - 500 fs typical time Step

  } Compliant with physics experiment

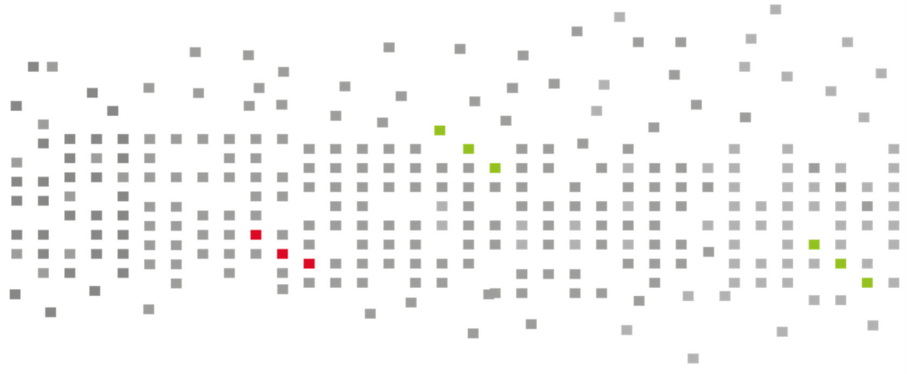
  - On chip synchronization
  - Recombination of channels => narrow pulse generation
  - Automatic calibration

  } New functions

  → Allows the design of low size delay generators whith new features

- **Next step: 2nd version scheduled in 2020**
  - Improved jitter and temperature drift
  - « On fly » loading of the 4 channels configuration registers with dedicated pin

Thank you for your attention



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