WEPHA096

Timing Signals Distribution for Synchrotron Radiation Experiments Using RF over White Rabbit

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Motivation

Some measurements in synchrotron radiation experiments requires high-precision timing signals synchronous with an accelerator.

- nuclear resonant scattering
- time-of-flight
- pump and probe time-resolved measurement using laser pulse

- **RF clock F_{RF}** (508.58 MHz @SPring-8)
- **fundamental revolution frequency F_{REV0}** (208.8 kHz@SPring-8)

I will conduct timing signal distribution for synchrotron radiation experiments at SPring-8 over a network by using RF over White Rabbit (RFoWR) technology.

Because…

- To use these signals at the experimental station, long RF cables and electronics (divider modules, delay modules, …) must be deployed.
- these timing signals are available for very limited beamlines because use of the dedicated fibers/cables restricts expandability of the signals.

Goals

- **renovate** the current timing signal distributions **using a network**,
- **offer increased usability** of the timing signals to the experimental users.

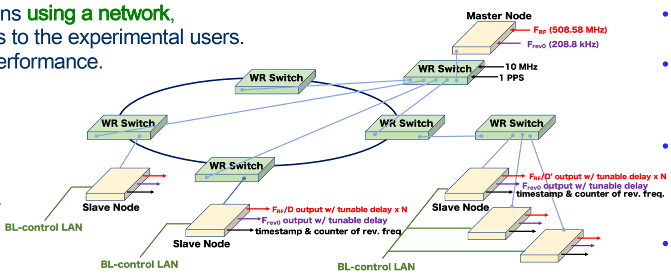
→ New system must provide equal or better performance.

- **F_{RF} distribution**

  Slave nodes should reproduce the sync. signals with F_{RF} and divided signals by 6, 12, 84 and 248, common divisors of harmonic number 2,436.

- **Keeping synchronization against slow changes in F_{RF}**

  should keep sync. against the slow adjustments of the F_{RF} in the range of ±500 Hz to compensate for the change in the SR circumference by tidal force.


Master Node
F_{RF} (508.58 MHz)
F_{rev0} (208.8 kHz)
WR Switch
10 MHz
1 PPS
WR Switch
WR Switch
WR Switch
WR Switch
WR Switch
Slave Node
Slave Node
Slave Node
F_{RF}/D output w/ tunable delay x N
F_{rev0} output w/ tunable delay
timestamp & counter of rev. freq
F_{RF}/D' output w/ tunable delay x N
F_{rev0} output w/ tunable delay
timestamp & counter of rev. freq.
BL-control LAN
BL-control LAN
BL-control LAN

Conceptual design of the timing distribution using RFoWR.

- **F_{REV0} distribution**
- **Phase adjustment**

  should provide a phase adjustable function of the output signals for the users with the resolution of < 50 ps.

- **Distribution of valuable information**

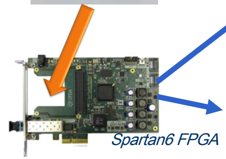
  can deliver timestamp and counter values related to the revolution frequency available as additional information attached to the experimental data.

- **Jitter of distributed signals**

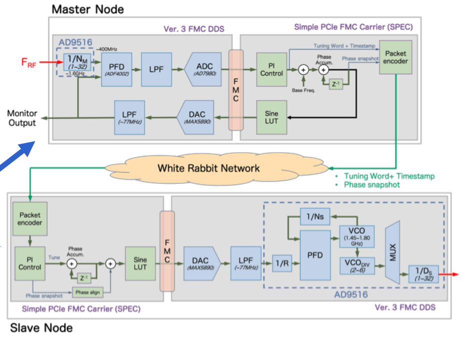
  required jitter is < 10 ps in the case of 84.76 MHz used for a laser oscillator (most severe case.

Building the Proof of Concept System (PoCS)

New ver. 3 FMC DDS



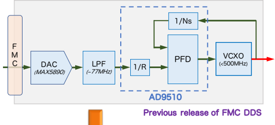
SPEC
(Simple PCI Express FMC Carrier)



Previous release of FMC DDS

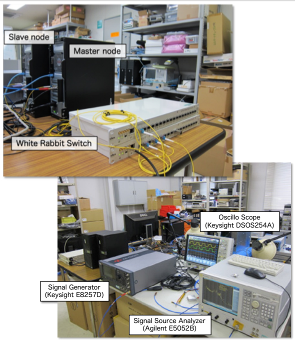
- could not provide enough output to reach 508.58 MHz,
- Did not meet our requirement because the measured jitter (10 Hz-20MHz) was ~16 ps *.

* T. Włostowski et al., "Trigger and RF Distribution Using White Rabbit", Proc. of 15th Int. Conf. of Accelerator and Large Experimental Control Systems ICALEPCS2015, Melbourne, Australia, 2015.



Purchased new ver.3 FMC DDS that had just been released.

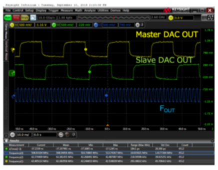
- Can be expected to output 508.58 MHz,
- Can be expected to provide better jitter performance than the previous version.


Slave node
Master node
White Rabbit Switch
Oscillo Scope (Keysight DSOS254A)
Signal Generator (Keysight E8257D)
Signal Source Analyzer (Agilent E5052B)

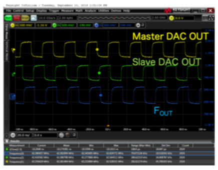
First Results Using the PoCS

1. F_{RF} & divided clock distribution

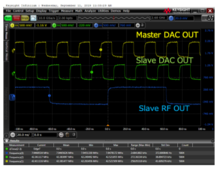
VCO_{DIV} = 3, D_S = 1
→ F_{OUT} = 508.58 MHz (= F_{RF})

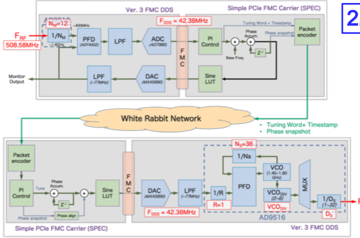


VCO_{DIV} = 3, D_S = 12
→ F_{OUT} = 42.38 MHz (= F_{RF}/12)



VCO_{DIV} = 6, D_S = 32
→ F_{OUT} = 7. 95MHz (= F_{RF}/64)

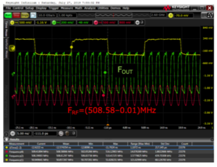




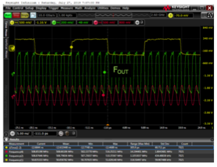
Parameters set

2. Keeping synchronization against slow changes in F_{RF}

1 kHz step
F_{RF}=508.58 MHz → 508.57 MHz
→ F_{OUT} keeps sync. with the F_{RF}



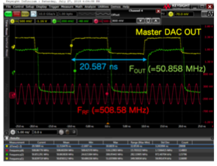
1 kHz step
F_{RF}=508.58 MHz → 508.59 MHz
→ F_{OUT} keeps sync. with the F_{RF}



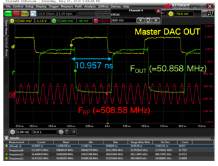
3. Resolution of phase adjustment

F_{OUT} = 50.858 MHz (VCO_{DIV} = 3, D_S = 10)

without phase offset



with phase offset = +1000 x 2^{32}



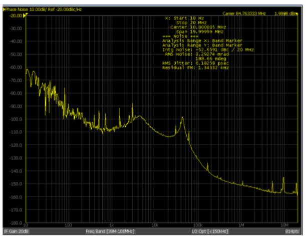
Difference = (20.587-10.957) ns
=9.63 ns

Resolution = 9.63 ns/1000x2^{32}
= 9.63 ps/2^{32}

4. Jitter of distributed signals

F_{OUT} = 84.76 MHz (VCO_{DIV} = 3, D_S = 6)

- Carrier : 42.38 MHz (508.58 MHz/12)
- F_{OUT} = 84.76 MHz (508.58 MHz/6)
- **Jitter : ~6 ps rms (10 Hz–20 MHz)**



Status and Perspective

Implementation of F_{REV0} distribution

- Reproduction of F_{REV0} in the slave node will be implemented by counting F_{RF}/DIV in the FPGA.
  - e.g., the FPGA counts 17.54 MHz (=F_{RF}/29), then it outputs a signal when the counter reaches 84 (=2,436/29).
- To align this output signal with F_{REV0}, a timestamp is recorded by the master node at the time the F_{REV0} signal input is utilized.

Implementation of a higher division rate than 64

- This function will be implemented in the same way as the F_{REV0} distribution.
  - e.g., when a signal obtained by F_{RF}/384 is desired, the slave node counts a 17.54 MHz (=F_{RF}/29) clock and generates a signal every time the counter reaches 12.
  - e.g., if a divided signal of F_{REV0}/21 is required, the slave node counts a 17.54 MHz (=F_{RF}/29) clock and outputs the signal every time the counter amounts to 84 × 21.

I would like to express my deepest gratitude to John Robert Gill@CERN.