TIMING SYSTEM UPGRADE FOR MEDICAL LINEAR ACCELERATOR PROJECT AT SLRI

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INTRODUCTION

SLRI has developed a prototype of the 6 MeV medical linear accelerator. A timing system is used to link various subsystems to provide synchronization for proper beam generation. All subsystems are connected to the Main Control System in a private network. In order to generate the required timing signals one needs to be able to adjust the resolution of the pulse width (in μsec) and delay time. Signal period can be adjusted to determine the frequency of the main clock. Analog output voltage level can also be determined as needed with enough number of channels as required by the subsystems. Configuration of all timing signals is also important. All of these requirements can be achieved by an easy-to-use GUI that is appropriately designed to communicate with users. Existing timing system has been used for testing the operation of the medical linear accelerator prototype for some time with satisfactory result. Recently, a new timing system has been designed to achieve better performance and to serve more requirements of the machine tests.

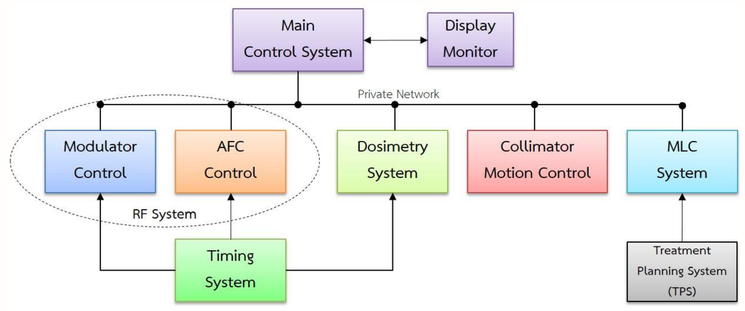

Figure 1: Network diagram of the machine prototype [1].

SYSTEM DESIGN

Hardware

- The main hardware platform for the new timing system is the Xilinx's Spartan 3 FPGA development board.
- System main clock of the FPGA main board runs at 50 MHz providing the resolution of 20 nsec.
- System main clock is multiplied by 2 in this new system so that the resolution is 10 nsec.
- The time-domain characteristics of individual timing signals can be set independently at the outputs of each timing module.

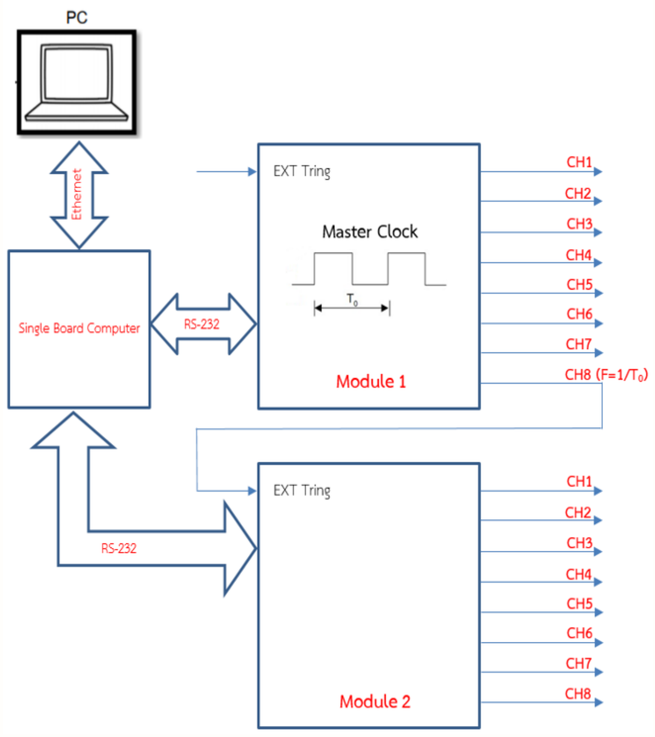

Figure 2: Timing System Diagram.

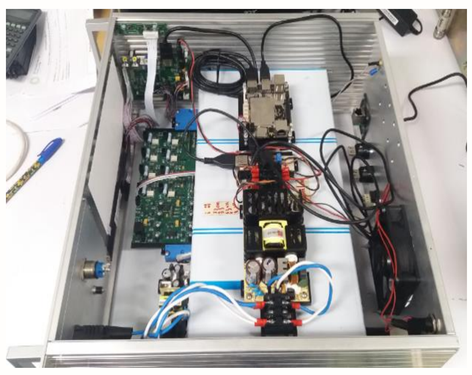

Figure 3: Installation of the hardware.

- One FPGA module has a maximum capacity of 8 timing outputs.
- The parameter adjustment on the FPGA depends on serial communication via RS-232 with the single board computer
- The remote personal computer which runs the GUI program communicates with the single board computer via Ethernet 10/100 Mbps.
- Synchronization between multiple FPGA modules can be done by connecting one output signal of one FPGA module as an external trigger to another FPGA module.
- 2 FPGA modules are connected in cascaded configuration. The last output (CH8) of FPGA module 1 is a trigger signal to FPGA module 2 for synchronization.
- The system effectively generates the total of 15 independent timing signals.
- Both FPGA modules can communicate independently with the single board computer via their own RS-232 ports.

Timing System Specification

1. Parameters of the signal from each channel can be determined independently from each other.
2. The output impedance of the desired channel can be chosen either 50 Ω or 1 kΩ.
3. Fundamental period (T_0) for determining the frequency of the main clock signal can be specified for the frequency from 0.0002 Hz to 10 MHz.
4. Delay time for shifting the desired timing signal can be independently chosen for each channel, which must be referred to the main clock signal, with a resolution of 10 nsec per step.
5. Pulse width of each desired channel has a resolution of 10 nsec per step.
6. For the channels with 50-Ω impedance output, the amplitude can be set between 2 and 20 volts.
7. For the channels with 1-kΩ impedance output, the amplitude can be set between 1 and 10 volts.
8. External trigger option can be enabled or disabled for individual FPGA modules (EXT Trig Channel).

Software

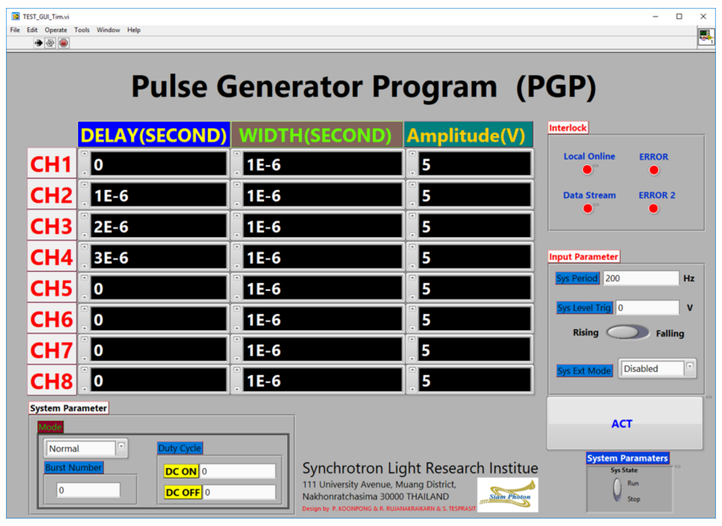

Figure 4: A new GUI.

- Main software design is developed using LabVIEW 2015.
- User determine pulse width, delay time, and amplitude of the timing signal for each channel. These parameters are transmitted via Ethernet communication to the single board computer.
- Standard Commands for Programmable Instruments (SCPI) is used as a basic international standard to generate commands for communication in order to create the timing signals for this system.
- The timing period T_0 is created within the FPGA module to be used as a reference for all channels. Delay time and pulse width are limited to be smaller than T_0.
- A VHDL function is designed and implemented in the FPGA modules to support a rate of 0.0002 Hz to 100 MHz at 10 nsec resolution. It also supports Burst Mode from 1 pulse to 9,999,999 pulses on the time-base basis.
- Outputs of the system can be chosen as a single pulse mode or burst mode, with additional information on duty cycle.
- External trigger is supported in the FPGA modules. The trigger input can handle the maximum frequency of 100 MHz. Rising-edge or falling-edge mode for the external trigger signal can be easily chosen with the maximum voltage of 15 Vdc.

CONCLUSION

The overall performance and time-domain characteristics of the timing signals are satisfactorily achieved. The concurrent operation of the multiple timing channels including the pulse width and delay time can be obtained similarly to the existing system. With this new design the timing resolution of 10 nsec for each step size is achieved as expected. The output voltage level of all timing channels can be easily customized. In addition, the synchronization option of two FPGA modules provides us flexibility to select and utilize more timing signals which will be required as the medical linear accelerator with multiple subsystems can be expanded, either for system test or commissioning purpose, in the future.

REFERENCES

[1] R. Rujanakraikarn and P. Koonpong, "FPGA-Based Motion Control System for Medical Linear Accelerator Development at SLRI", in Proc. 16th Int. Conf. on Accelerator and Large Experimental Control Systems (ICALEPCS'17), Barcelona, Spain, Oct. 2017, pp. 562-565. doi:10.18429/JACoW-ICALEPCS2017-TUPHA069
[2] P. Koonpong and R. Rujanakraikarn, "Timing System Using FPGA for Medical Linear Accelerator Prototype at SLRI", in Proc. 16th Int. Conf. on Accelerator and Large Experimental Control Systems (ICALEPCS'17), Barcelona, Spain, Oct. 2017, pp. 589-592. doi:10.18429/JACoW- ICALEPCS2017-TUPHA079
[3] http://www.xilinx.com
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