ISBN: 978-3-95450-209-7 ISSN: 2226-0358 doi:10.18429/JACoW-ICALEPCS2019-WEPHA071

TIMING SYSTEM INTEGRATION WITH MTCA AT ESS

J. J. Jamroz, J. Cereijo García, T. Korhonen, J. H. Lee, ESS, Lund, Sweden

Abstract

European Spallation Source (ESS) organization has selected cutting-edge technologies to satisfy performance and scalability expectations:

- Micro Telecommunications Computing Architecture (MTCA).
- Micro Research Finland (MRF) based timing system with delay compensation.
- Experimental Physics and Industrial Control System (EPICS).

To achieve optimal data acquisition quality, the control system is built on top of the timing system which gives the same absolute time reference to all EPICS process variables (PVs). The MTCA system gives configurable cableless access to manage connections among different electronic mezzanine cards, therefore reducing installation workload.

INTRODUCTION

ESS is a collaboration of 17 European nations and its objective is to be the world's most powerful spallation neutron source [1].

The neutrons are produced by a 5 MW proton beam (125 MW peak) hitting a solid, rotating tungsten target in 600 m distance from the ion source. The target weights 11 tonnes and rotates at 23 1/3 rpm containing 36 sectors.

The acceleration of the proton beam is ensured by a Radio-Frequency linear accelerator (RF linac) operating on 352.21 MHz (RF_L) up to 216 MeV and 704.42 MHz (RF_H) up to the nominal energy of 2 GeV. Main characteristics are 14 Hz repetition rate, 62.5 mA peak beam current, and 2.86 ms beam pulse length.

The linear accelerator consists of Normal Conducting Linac (NCL) and Superconducting Linac (SCL) with the following parameters:

- NCL: length = ~50 m, nominal energy = ~90 MeV.
- SCL: length = ~550 m, nominal energy = 2 GeV.

Superconductor cavities are cooled down to ~2 K using liquid helium. The design considers 180 klystrons with 1 MW peak power per each (40 kW average). The machine targeted operational availability is 95%.

TIMING NETWORK

Figure 1 presents the timing network. The installation is based on single mode OS2 duplex fibers (double sided arrows) due to the bandwidth–length product, monolithic network structure and compatibility to the IT infrastructure and easier maintenance. The RF Front End, TM, TD11, TD12 chassis are located within one cabinet making the tree trunk and connected to uninterruptible power source. The RF Front End electronics feeds TM with $RF_L/4$ (88 MHz) and Pulse per Second (PPS) synchronized to Global Positioning System (GPS). The TD21 up to TD2X chassis are distributed along with the linac inside the klystron gallery (service area) and supplying timing signals to other subsystems via TDMS. TDMS is an MTCA chassis with EVR which belongs to a specific subsystem. The EVR injects timing signals into the MTCA backplane to other AMC cards within the subsystem.

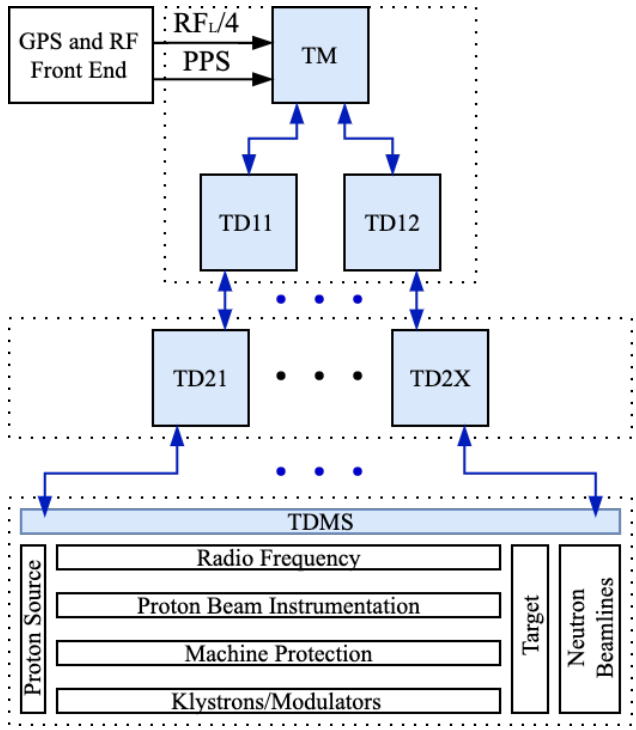

Figure 1: ESS timing network - tree topology. Timing Master (TM); Timing Distribution (TD); TDX_1X_2: X_1 - tree layer, X_2 - ID, TD2X contains X = 41 currently; Timing Distribution to Machine Subsystem (TDMS).

The MRF timing protocol assigns automatically each timing device to a topology ID. This feature has been used to develop a timing network builder [2] which plots actual network connections with states and power levels of transceivers. The builder is used to troubleshoot installation, to verify documentation and to perform maintenance checkups. In addition, the protocol supports a delay compensation of an optical signal. It makes the system resilient to aging and temperature impact on optical fiber (propagation delay) as the signal delay drifts are continuously compensated.

MTCA

MTCA is an open standard embedded computing specification created by PCI Industrial Computer Manufacturers Group [3]. Figure 2 presents the specification capabilities. MCH acts as a switch of different interfaces connected to AMCs within the system. Therefore, each AMC can utilize

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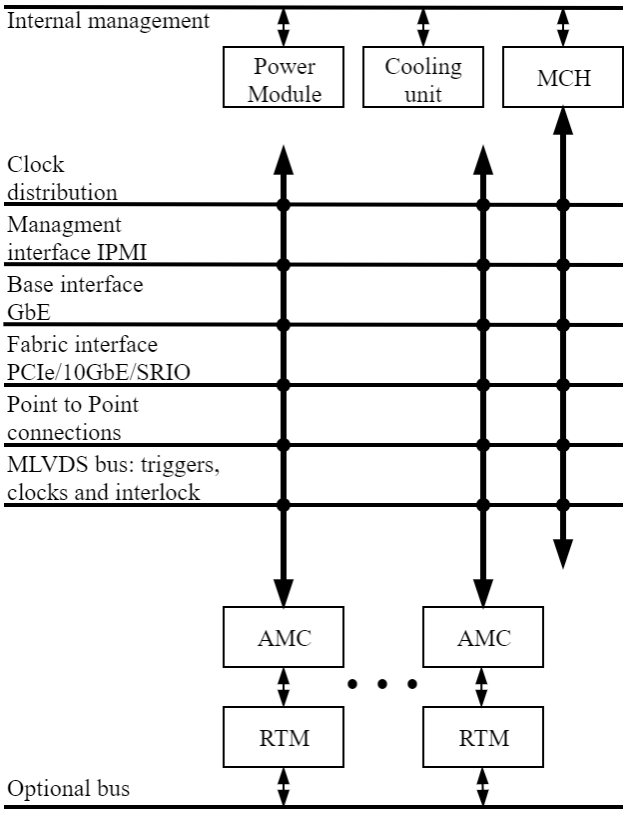

Figure 2: MTCA overview diagram. MTCA Carrier Hub (MCH), Advanced Mezzanine Card (AMC), Rear Transition Module (RTM).

GbE connection, a PCIe link (high speed communication or control capabilities), clocks and MLVDS trigger/interlock lines. The management interface is used for hardware health monitoring.

It is notable that within one MTCA crate, multiple industrial computers can be set up, whereas other standards allow only one master CPU. It gives hardware scalability to increase the capabilities of a certain distributed machine point without affecting an existing installation.

Host Hardware

Each MTCA system requires basic components in order to host AMCs. The following hardware was selected for that purpose:

- Chassis: 9 HE 12 AMCs 12 RTMs and 3 HE 6 AMCs 4 RTMs by Schroff.
- MCH: NAT-MCH-PHYS by N.A.T. Europe (NAT).
- Power Module (PM): NAT-MTCA-PM-FW 1000 W by Wiener and NAT-PM-AC600D 600 W by NAT.
- CPU AMC: AM90x and AMG6x by Concurrent Technologies.

Timing Hardware

The timing hardware is based on 2 different AMCs which were specially designed to meet the platform and performance requirements in collaboration with MRF [4]:

- Event Receiver (EVR): mTCA-EVR-300U.
- Event Master (EVM): mTCA-EVM-300. Event Generator (EVG) and Fan Out Concentrator capabilities within the same unit.

Timing Distribution Node

Three MTCA distribution nodes (TM, TD1, and TD2) are the main components of the timing network, shown in Fig. 1. Table 1 shows detailed information of each one.

Table 1: Timing distribution Nodes

Slot	TM	TD1	TD2-9U	TD2-3U
PM1	PM 1kW	PM 1kW	PM 1kW	PM 600W
PM2	PM 1kW	PM 1kW	Spare	N/A
MCH1	MCH	MCH	MCH	MCH
MCH2	Spare	Spare	Spare	N/A
AMC1	CPU	CPU	CPU	Spare
AMC2	EVG	EVM	EVM	CPU
AMC3	Spare	EVM	EVM	Spare
AMC4	EVM	EVM	EVM	EVM
AMC5	EVM	EVM	Spare	EVM
AMC6	EVM	EVM	Spare	EVM
AMC7	EVM	Spare	Spare	N/A
AMC8	Spare	EVM	Spare	N/A
AMC9	Spare	EVM	Spare	N/A
AMC10	Spare	EVM	Spare	N/A
AMC11	Spare	EVM	Spare	N/A
AMC12	EVM	EVM	Spare	N/A

The distribution is based on the same 9U chassis. TD2 (the highest quantity) is the exception as it is made of two different types:

- 9U chassis in places where it is recommended to have more spare AMC slots for future expansions.
- 3U chassis in other places in order to decrease costs.

TDMS is the front end of the timing network and it is made of one EVR inside an AMC2 slot of an MTCA chassis which belongs to a certain subsystem. Table 2 presents a typical TDMS implementation.

Table 2: Timing System Interface to an ESS Subsystem

Slot	TDMS
PM1,2	PM 1kW
MCH1,2	MCH
AMC1	CPU
AMC2	EVR - the timing subsystem interface
AMC3-12	AMC - subsystem specific
RTM3-12	RTM - subsystem specific

TIMING SYSTEM

The main role of the ESS timing system is to generate, acquire and distribute $RF_L/4$ based:

- Synchronous clock signals: $RF_L/4$.
- Trigger events as a derivative of timing events.

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- Data buffer with beam and machine parameters.
- Absolute time reference.
- Asynchronous machine events.

In addition, those features are utilized for troubleshooting of different distributed subsystems.

Timing Events

The timing events are used to generate trigger events (electrical or optical pulses) by EVR in accordance to trigger properties (delay, width, output type, etc.) in order to properly trigger a relevant subsystem. The timing events have been split into purpose blocks:

- [0x01 - 0x27] - repetitive RF synchronized events for the beam operation, in the EVG (master) sequencer: Ion Source Start & End (`ION_ST` & `ION_END`), Beam Pulse Start & End (`BPULSE_ST` & `BPULSE_END`), Start Of Cycle (`14HZ`), Beam Pulse Coming (`BPULSE_CM`), Send Data Buffer (`DATA`).
- [0x28 - 0x31] - special non-repetitive asynchronous events: Postmortem - global and local[1] (instrument) request (`PMORTEM` & `PMORTEMI`), Data On Demand - global and local (instrument) request (`DOD` & `DODI`), Calibration (`CAL`).
- [0x32 - 0x3B] - other master events (multiplexed counters, software events, etc.).
- [0x3C - 0x6F] and [0x72 - 0x78] - not allocated, spare codes.
- [0x70, 0x71, 0x79 - 0x7F] - predefined special events for MRF hardware functionality.
- [0x80 - 0x95] - local EVR input events, time digitizers (TDCs) used to timestamp experimental data.
- [0x96 - 0xC7] - local EVR sequencer events, local state machines used to generate a local sequence of events upon an arbitrary global event.
- [0xC8 - 0xFF] - not allocated, spare codes.

The total number of events is 256 (0xFF). The design assumes that upstream and downstream event codes serve the same purpose - flat design.

Beam Modes

Main modes of the ESS linac:

- Probe - initial check, beam threading.
- Fast Tuning - RF setting.
- Slow Tuning - invasive measurements, Low Level RF setting.
- Long Pulse - beam loss check, Lorentz detuning check.
- Neutron Production - regular operation.

Table 3 shows one-cycle trigger[2] sequence within the neutron production mode. The other modes operate on modifications of the regular settings. `MOD` and `CHOP` triggers are generated by other events in the cycle by adding adequate delays. The time gaps are planned to be used by processing time of EPICS high level applications in order to change the timing system parameters on time, so within the cycle.

Table 3: Neutron Production - One Linac Cycle

Trigger Event	Δt [ms]	Description
`14HZ`	0	Start Of Cycle
`ION`	~10	Ion Source Start
`MOD`	~12.88	Modulator Trigger
`BPULSE_CM`	~13	Beam Pulse Coming
`CHOP`	~13.3	NCL Chopper Trigger
`BPULSE_ST`	~13.32	Beam Pulse Start
`BPULSE_END`	~16.18	Beam Pulse End
-	-	Time Gap
`DATA`	~30	Send Data Buffer
-	-	Time Gap
	71.43	End Of Cycle

Data Buffer

The data buffer is a RAM region with the beam and machine parameters. The `DATA` event occurrence starts a process when the buffer content is injected into the timing network by TM. The process occurs typically at the end of the event sequence within one linac cycle as presented in Table 3. Table 4 presents the data buffer inner variables. The reserved data type serves two purposes: a holder for future extensions and byte offset alignment in order to allow integer (4 bytes) readouts of the inner buffer values.

Table 4: Timing Data Buffer - 32 Bytes

Offset	Byte	Data Type
0	1	Protocol number
1	1	Reserved
2	1	Protocol version
3	1	Reserved
4	8	Linac cycle counter/ID
12	1	Beam on/off
13	1	Beam destination (last point)
14	1	Beam mode
15	1	Reserved
16	4	Beam length: float [ms]
20	4	Beam energy: float [MeV]
24	4	Beam current: float [mA]
28	1	Raster pattern: 14 beam slots
29	1	Target segment (1-36)
30	1	Reserved
31	1	Reserved

Timing Distribution to Machine Subsystem

The TDMS EVR presented before in Fig. 1 delivers timing clocks and triggers electrically over the backplane to other AMC cards within a certain subsystem. Table 5 presents physical connections and signals between the EVR and other AMCs within a chassis.

[1] The local is within a chassis and the global covers the machine.

[2] If the timing event abbreviation is used as a trigger abbreviation, it points that the trigger is generated by the event with a subsystem specific configuration.

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Table 5: MTCA MLVDS Backplane Signal Distribution

Line	Function	I/O	Trigger	Frequency	Description
TCLKA	RF CLK	OUT	N/A	88MHz@RF	$RF_L/4$ - AMC clock
TCLKB	RF CLK	OUT	N/A	-	A spare clock
RX17	Trigger	OUT	14HZ	14Hz@RF	Start Of Cycle
TX17	Trigger	OUT	BPULSE_CM	<=14Hz@RF	Beam Pulse Coming
RX18	Trigger	OUT	BPULSE	<=14Hz@RF	Beam Pulse Length defined by BPULSE_ST&END
TX18	Trigger	OUT	PPS	1Hz@GPS	Pulse per Second
RX19	Trigger	OUT	PMORTEM	Asynchronous	A local postmortem acquisition
TX19	Trigger	IN	PMORTEMI	Asynchronous	An AMC requests a global postmortem acquisition
RX20	Trigger	OUT	DOD	Asynchronous	A local data acquisition
TX20	Trigger	IN	DODI	Asynchronous	An AMC requests a global data acquisition

TCLKA delivers 88 MHz ($RF_L/4$), that synchronizes other AMC internal clocks, acquisition and functions in order to perform RF based deterministic operations by a subsystem.

14HZ trigger always occurs together with the linac cycle, delivering a linac cycle fiducial mark. BPULSE_CM and BPULSE existence depends upon the operation mode. It is notable that BPULSE trigger is as long as the proton beam length, therefore it delivers a piece of complex timing information about the beam start, end and length. The BPULSE trigger is constructed by two other events: BPULSE_ST & BPULSE_END. PPS delivers a second reference synchronized to GPS in order to reset timestamp arrays.

The asynchronous triggers are dedicated for postmortem and on-demand data acquisition. PMORTEM is caused by a fault occurrence somewhere in the ESS machine and requests to freeze postmortem data buffers within the subsystem (chassis) for future analysis. PMORTEMI is generated locally by AMC and requests a global postmortem acquisition. In order to achieve that, the timing system delivers the PMORTEM event to other subsystems. DOD can happen periodically (every couple of minutes) by a software routine in order to collect acquisition data. In addition, it can be requested arbitrary by an operator. On the other hand, DODI trigger is generated automatically by a subsystem. The DODI activator has to be predefined for that purpose, e.g. beam current value over a certain interest point.

EPICS INTEGRATION

The EPICS [5] Input/Output Controller (IOC) executes on a CPU card in an MTCA crate and connects to the technical network through MCH. It communicates with the EVM or EVR over PCIe on the backplane.

The EPICS integration of the ESS timing system is based on the community edition of the IOC for the MRF timing system, mrfioc2 [6]. The IOC has been adapted for usage at ESS [7] by modifying the code structure to allow compilation and distribution through the ESS EPICS Environment, E3 [8]. The E3 environment allows an EPICS integrator at ESS to add support for the timing system in two parts: the devlib2 library [9] for communicating with the EVR/EVM and the mrfioc2 module.

Figure 3 presents a block diagram of the timing hardware integration into EPICS. The e3-mrfioc2 [10] application is

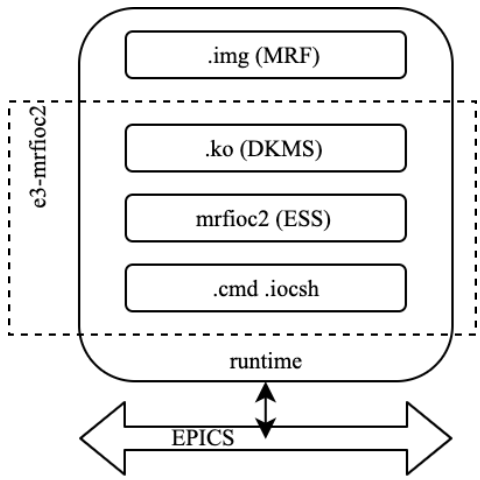

Figure 3: EVM/EVG and EVR IOC software stack.

source code based, platform independent (Debian, CentOS, etc.) and handles the following core parts:

- The 64 bit kernel object (.ko) compilation and deployment within Dynamic Kernel Module Support (DKMS).
- The ESS fork of mrfioc2 which complies with ESS requirements.

The e3-mrfioc2 module within E3 manages the timing software stack with source release tags, versioning, compilation, rollbacks, installation in order to run the EVM or EVR IOC. The FPGA image files (.img) are delivered by MRF. IOC shell files (.cmd, .iocsh) apply a proper configuration to the timing hardware within a certain use case.

Figure 4 depicts a control room where an operator supervises the system with GUI-based interfaces (OPIs) - dotted-line blocks. A supercycle means a predefined sequence of 14 Hz machine cycles, e.g. 1 Hz supercycle has 1 cycle with a beam and 13 cycles without any beam respectively. The cycles are preconfigured with the Control OPI. The Supercycle application is the Control OPI backend which prepares

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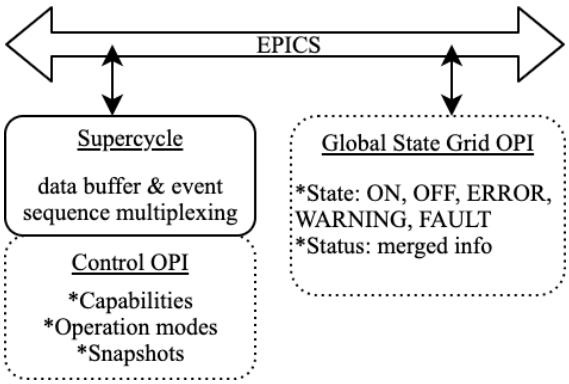

Figure 4: Timing applications.

EVG event sequences and the data buffer within one machine cycle. It means that the next cycle is prepared before the end of the current one.

TM, TD1, TD2 and TDMS IOCs are monitored by the Global State Grid which gives a look at an actual state of a node in the timing network.

The FPGA image development of the MTCA timing hardware continues and new features are continuously updated into ESS mrfioc2 by ESS ICS HWI group together with e3-mrfioc2. The updates are shared with the EPICS community.

SUMMARY

The ESS deployment of the timing system is based on two AMCs. It increases troubleshoot capabilities within the system and decreases installation complexity. All the features are successfully running and the integration with MTCA has passed tests successfully, therefore it confirms that the system meets the expectations.

In addition, the significant contribution to MTCA hardware and software development has been released to the scientific community.

OUTLOOK

A neutron science group requested a fast absolute TDC to generate experimental data coming from neutron choppers and devices distributed along a beamline. A theoretical performance expectation is around 5000 tst/s (timestamp/s).

Figure 5 presents a test setup in order to achieve the goal with EVR. The actual TDC max speed reaches to around 400 tst/s (IN0 + IN1 trigger timestamps) without losing any data and it is one order of magnitude too slow. At present, mrfioc2 FIFO depth is 1 for each event code and mostly used up to 120 tst/s by the EPICS community.

An advanced implementation would be to improve the software queue to allow deeper buffering of some event codes. This would increase the time needed to readout and process the result. For instance, a 512 element FIFO theoretically would need to be read only once per second. This implementation would remove a need for any other TDC system at ESS and speed up a future neutron experiment development by utilizing the existing hardware and software further on.

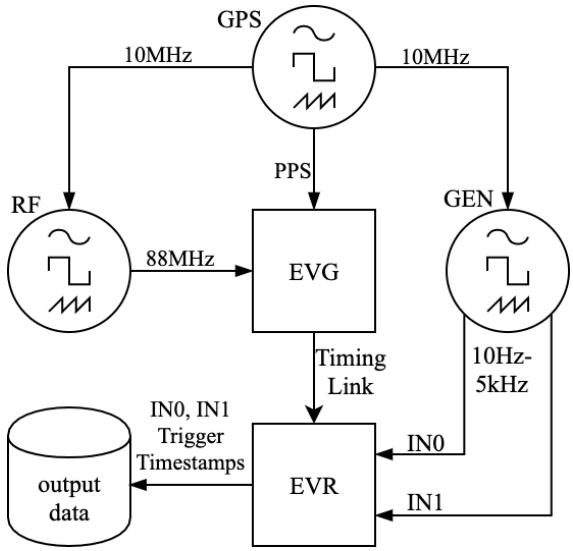

Figure 5: The absolute TDC evaluation setup with EVR.

ACKNOWLEDGEMENTS

I wish to acknowledge the help provided by Karl Vestin with project management and support, Faye Chicken with a project asset inventory and management, Peter van Velze with installation support, Jukka Pietarinen with EVM/EVR FPGA image development and support, Michael Davidsaver with development of mrfioc2.

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