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MAJOR UPGRADE OF THE HIT ACCELERATOR CONTROL SYSTEM USING PTP AND TSN TECHNOLOGY

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Abstract

Two important reasons led to the first developments for a new ACS for the HIT ion therapy accelerator complex: a) the first implementation of the ACS was done in 2003-2005. It was implemented as a proprietary solution, which works very well and reliable for more than 10 years. However, more and more components e.g. parts of the device control units (DCUs, [1]) are no longer in stock. Thus a new realization using standard SoCs or similar is necessary; b) new functionalities like multiple energy operation [2] should enhance the duty factor of the accelerator facility resulting in significantly higher patient irradiation efficiency. In cooperation with our commercial partner Eckelmann [3] we are investigating the newly available deterministic Ethernet technologies like "Time-Sensitive Networking" with several IEEE 802.1xx sub standards [4]. Early TSN implementations in embedded controller boards and switches were obtained in a test installation in autumn of 2018. The test bench was set up to study the feasibility of e.g. the required timing precision using PTP, respectively IEEE 802.1AS-Rev. The aim is to realize a "one-wire-ACS" based on Ethernet only for deterministic data transfer and message based triggers for synchronized ACS functions. Results from our TSN test bench experiences will be reported.

THE HEIDELBERG IONBEAM THERAPY FACILITY

The HIT accelerator complex is based on a linac-synchrotron system accelerating ions to energies up to 430 MeV/u corresponding to ion penetration depths of approx. 30 cm in human tissue.

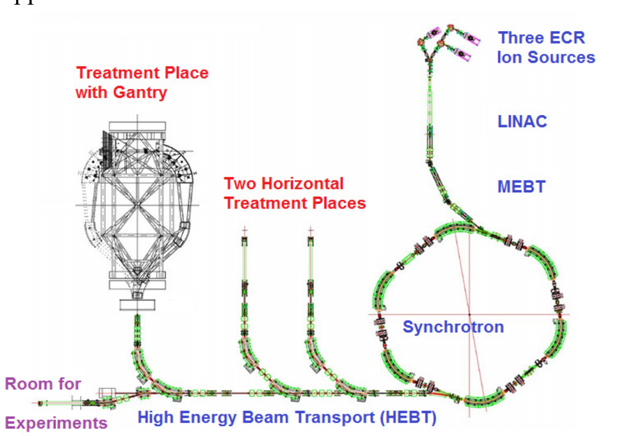

Figure 1: Schematic view of the HIT accelerator complex.

The facility – constructed from 2003-2008 – is equipped with two fixed horizontal beam lines, a rotating beam line (heavy ion gantry), all for patient treatment, and an experimental area (Fig. 1). The synchrotron is a cyclic operating device with phases of beam injection, acceleration to the desired particle energy, corresponding to the desired penetration depth (iso energy slice), beam extraction, and preparation for the following cycle. Ions are slowly extracted by the transverse knock-out extraction method with extraction times which last up to 5 s [5]. HIT uses the intensity controlled raster scanning method of pencil beams as dose delivery system [6].

Cancer therapy with carbon ion and proton beams has been carried out at HIT since 2009 (gantry part since 2012). Currently around 700 patients are irradiated per year; approximately 5700 patients have been treated in total since the beginning.

CURRENT HIT ACS AND ITS TIMING SYSTEM

The HIT ACS has the following top-down structure:

- *Presentation Layer* with GUIs on Operator PCs under Win10,
- *Coordination Layer* with different servers (OracleDB, Sequence Control, SataSupply Model) under WinServer2019 and the timing master, which feeds the real-time bus (RTB) and communicates with the Therapy Control System (TCS),
- *Communication Layer* with network, RTB and linked DCUs
- *Devices* and Subsystems for slow controls.

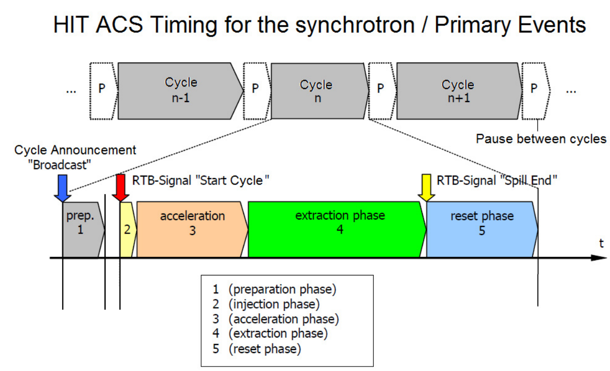

Figure 2: HIT ACS timing for the synchrotron part [7].

During treatment the TCS sends commands with the next ion beam request via CAN bus to the ACS, which contain the next accelerator settings (ion species, energy, intensity, focus) to be carried out – safety in this communication and the subsequent cycle execution is assured by several mechanisms like redundancy, checksums, etc.

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During treatment the ACS is completely under remote control. The machine and its settings can also be fully controlled by the operator.

The timing system was developed together with the device control units designed in 2003. They contain a MPC5200 processor with a proprietary OS and an Altera Stratix FPGA for the device type specific control firmware, written in VHDL. The DCUs are all linked to a proprietary timing bus (RTB), which is realized using Cat5 cable carrying primary events / triggers as HW signals. For the synchrotron cycles the following primary events are used (see Fig. 2) to start the different machine phases: Synchrotron Cycle Start, Spill Pause (Gate), Spill End and a Master Clock on the fourth twisted pair. The specified timing precision was ±1 µs, but by runtime adjustment of the RTB signals between the DCUs a precision of ±10 ns was achieved. A new test showed that the most time critical accelerator phase, the multi-turn injection into the synchrotron, needs a device-to-device timing precision of about ±500 ns.

THE MOTIVATION FOR A MAJOR UPGRADE

Sixteen years after the ACS development started and with about ten years of operation (with 8200 hours per year) a major upgrade seems to be eligible:

(1) More and more ACS components get obsolete, a new DCU generation will be necessary.

(2) New functionalities for higher efficiency of the facility are needed – the so-called "multiple energy operation" scheme may reduce the irradiation time by a factor of two, see Fig. 3. On the other side this will cause a higher complexity of the ACS and more flexibility is necessary within the timing of a synchrotron cycle.

(3) To increase the ACS reliability furthermore, e.g. a reduction of the cabling and connections would be desirable, leading to a "one-wire-ACS" based on Ethernet only for deterministic data transfer and message based triggers for synchronized ACS functions.

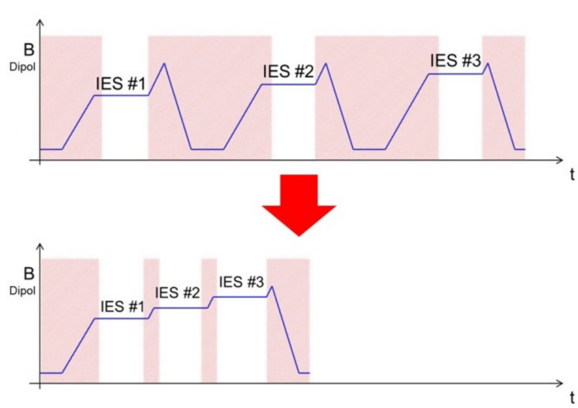

Figure 3: Using a "multiple energy operation" scheme will reduce the irradiation time per patient up to a factor 2 (IES: iso-energy layer).

PTP AND TSN – A SOLUTION FOR THE HIT ACS UPGRADE?

In industry a lot of different real-time buses are in use today, but more or less all of them are vendor-specific, even if they use the Ethernet HW platform. Therefore a new standard will lead from standard Ethernet (IEEE 802.3) to "Time Sensitive Networking" (TSN) introducing real-time communication with hard, non-negotiable time boundaries for end-to-end transmission latencies, or shortly: "deterministic" Ethernet. This aims for time synchronization within networks with high precision (IEEE 802.1AS). The clock synchronization of all network-linked controllers is achieved by distribution from one central time source directly through the network. Basis of this technique is the IEEE 1588 Precision Time Protocol (PTP), which utilizes Ethernet frames to distribute time synchronization information. In the case of the HIT ACS the primary events (HW) can be replaced by Ethernet commands with time triggers (SW), if all clocks of the ACS are synchronous within less than ±500ns.

The questions to solve are:

- Will this technique be available today or in near future? Yes, there is a big boost by the automotive market. And there is a very lively community around TSN, see e.g. [8] for a yearly industry conference on this topic.
- Are there enough components available to test the features and promised performance? Yes, here is a short list of such devices under investigation at HIT/EAG: a) Network Switches: Hirschmann/Belden RSPE35, Cisco IE4000, etc.; b) Embedded Controllers: MitySOM, NovPek, NetLeap, etc.; c) Grandmaster clocks: Meinberg microSync and others.

Seeing these results of a comprehensive market survey HIT set up a test bench together with its partner company at the end of 2018. The aim was to check the capabilities of TSN for the next generation ACS.

FIRST TIMING MEASUREMENT RESULTS FROM A PTP/TSN TEST BENCH

Along the HIT ACS conditions of today a small test bench was designed. Distances comparable to the HIT building were assumed, e.g. a length of 100 meters from one switch to a second one using fibre optic cable (FOC) and also up to 100 meters of copper cable to connect embedded controllers as the worst case, see Fig. 4.

In the existing ACS 100 Mbit/s network, the load is less or equal to 5% with bursts up to 10% (normal "cyclic" operation), the TSN LAN is a 1 Gbit/s network, the load is estimated to only double in the next generation ACS. The first test case to be investigated: Compare clock synchronization precision of two embedded controllers across the network with optional additional network load by two PCs. As we need no absolute time the grandmaster clock was activated on one of the switches.

NetLeap Evaluation boards were used which are equipped with NOVSOM®CVL Intel Cyclone V SoCs;

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these chips contain a dual-core ARM Cortex-A9 processor system with additional FPGA logic on a single chip. RT-Linux is used in the ARM cores; the TSN/PTP stack, commercially available from companies like TTTech or CAST, is implemented in the FPGA logic. For the exact measurement of the time jitter between two controllers the signals "Pulse per second PPS" of both boards were connected to an oscilloscope. In addition, tools like ftp and Iperf were used on two attached PCs to increase the network traffic.

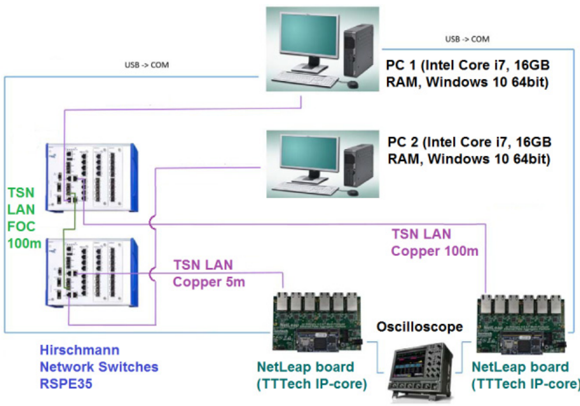

Figure 4: TSN test bench for the next generation HIT ACS using Hirschmann/Belden RSPE35 switches and NetLeap boards with TSN IP stacks.

The results are very encouraging; the clocks of both controllers are running synchronously within less than ±25 ns, as can be seen in Fig. 5, the jitter stays between the two dashed marker lines.

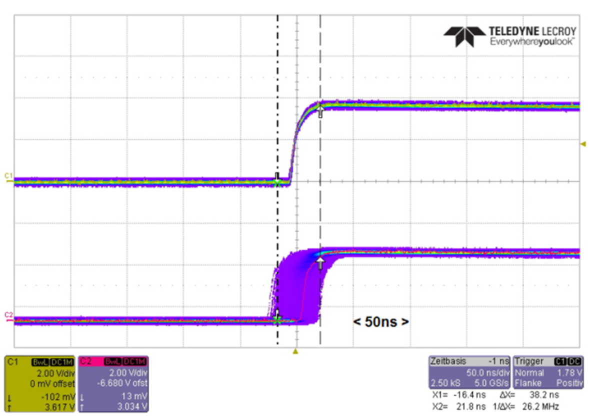

Figure 5: Oscilloscope screenshot after two hours runtime, set-up described in the text.

Additional network traffic does not change the result essentially; the marker lines are only insignificantly passed. Thus the necessary precision is undercut by a factor of twenty!

SUMMARY AND OUTLOOK

The HIT ACS timing constraints are satisfiable using TSN/PTP; an implementation of the enhanced TSN standard IEEE802.1AS-REV (still Draft 8.1, should be finalized by end of 2019) will introduce improved time measurement accuracy in addition. Thus the "one-wire-ACS" seems possible – a check with more embedded controllers in the network is still due. Other TSN features like scheduling and traffic shaping (IEEE 802.1bv) as well as frame pre-emption technology (IEEE 802.1bu) will also help to make the ACS network traffic more secure and reliable. All components to be used are commercially available today or in the near future; they are based on industry standards concerning HW and SW, only the device interfaces will still remain proprietary. Fortunately, the existing FPGA firmware code for the different accelerator devices in VHDL can be transferred from ALTERA Stratix to Intel Cyclone SoCs with only few modifications.

An implementation study of a TSN based HIT-ACS 2.0 is under way and will be ready in Q1/2020 – the planned realization is scheduled in the years 2020-2022.

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