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A 4-CHANNEL, 7 ns-DELAY TUNING RANGE, 400 fs-STEP, 1.8 ps RMS JITTER, DELAY GENERATOR IMPLEMENTED IN A 180 nm CMOS TECHNOLOGY

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Abstract

This paper discloses the silicon integration, in a 180 nm CMOS technology, of a 4-channel delay generator dedicated to timing with resolution lower than a picosecond. This integrated circuit aims at miniaturizing delay generators while fulfilling the needs of modern physics experiments.

The delay generation principle relies on the linear charge of a capacitor triggered by the input pulse. The output pulse generation occurs when the capacitor voltage exceeds a programmable threshold voltage. A calibration circuit is embedded on-chip to automatically match the delay tuning range to the period of the master clock, ranging from 5ns to 7ns. The delay value is set with the help of a 14-bit DAC which leads to a 400fs delay step. Among other features, the chip embeds a combination mode of either 2 or 4 channels to output narrow width pulses. The chip is fully compliant with LVDS, LVPECL and CML differential pulses at its input and produces LVPECL pulses output.

The chip has been fully characterized over temperature (0 to 60°C) and supply voltage (+/- 10%). The chip is compliant with pulse repetition frequencies up to 20 MHz. The measured INL is 100 LSBs and the RMS jitter is 1.8 ps. The power consumption has been measured to 350 mW for 4 active channels.

INTRODUCTION

Synchronization of large physics experiments requires accurate timing systems having resolution down to a few picoseconds. They are usually made of several multi-channel delay generators that provide different sampling rates for multi-shot or single short triggering for each instrument distributed in a large area [1][2]. Experiments using large number of instruments require large number of delay channels and thus several multi-channel delay generators. Therefore, miniaturization of delay channels is highly desirable in order to provide either low volume delay generator modules or delay generators embedding a high number of delay channels.

A few Integrated Circuits providers offer delay generator products [3] [4] [5]. Nevertheless, as it could be seen in Table 1, these solutions failed to fulfil the needs of physics experiments in terms of time step which is limited to 5ps in the best case. This paper discloses the implementation of a 4-channel delay generator in a 180 nm CMOS technology and packaged in a small 56-pin QFN package. Its small form factor as well as its overall performances in terms of delay step (< 500 fs), full scale (7ns) and jitter (1.8ps) pave the way to the design of delay generators having very large numbers of delay channels and compliant with physics experiment requirements.

Table 1: Existing Delay Generators Integrated Circuits

Parameter	[3]	[4]	[5]	Unit
Delay Step	5	10	10	ps
Full Scale	5	5.6	10	ns
RMS jitter	1	-	3	ps
Pules repetition rate	1	1.5	1.2	GHz
Temperature drift	-	10	-	ps/°C
INL	30	40	20	ps

The paper is organized as follows: a first section introduces the targeted specification. A second section details the overall architecture of the proposed delay generator and the implementation of its building blocks and functions. The third section presents the measurements results. Some conclusions end the paper.

Table 2: Delay Generator Specifications

Parameter	Value	Unit
Channels	4	
Delay Step	<1	ps
Full Scale	7	ns
RMS jitter	< 2	ps
Pulse repetition rate	< 20	MHz
Master Clock Frequency	150 – 200	MHz
Temperature drift	<4	ps/°C
INL	<1	% FS

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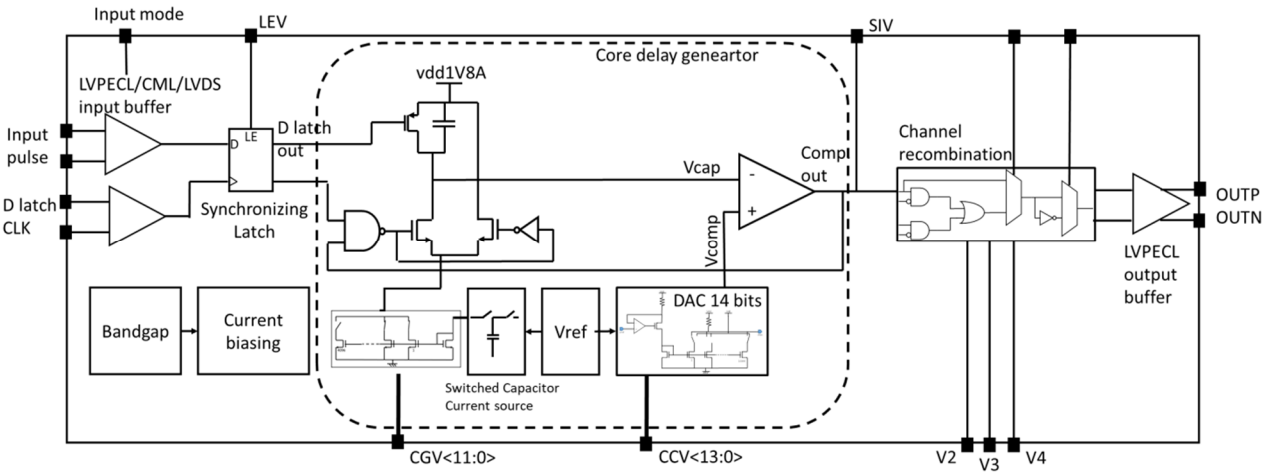

Figure 1: Architecture of a channel of the delay generator.

CHIP SPECIFICATIONS

The proposed circuit aims at providing a fine delay generation with a full scale corresponding to the period of a high frequency master clock which could be used itself as the counting clock of a coarse delay generator.

Table 2 lists the targeted specifications of the delay generator chip. They have been set to be compliant with modern physics experiments requiring a time step lower than a 1 ps and a limited jitter. They have been set to be fully compliant with Greenfield Delay Generators specifications.

DELAY GENERATOR ARCHITECTURE

Channel Architecture

Figure 1 depicts the overall channel architecture. It is composed of a differential input buffer which could be configured to be compliant with LVPECL, CML and LVDS input.

An on-chip D latch has been integrated for on-chip resynchronization purposes. The D-Latch output triggers the programmable delay generator.

Then the pulse enters a multiplexer that permits to output either directly the programmable delay output or a recombination of 2 or 4 channels output.

Last, the multiplexer output is sent out of chip through a LVPECL output buffer.

Figure 2 depicts the chronogram of the delay channel from the pulse input to the comparator output.

Input Buffer – Clock Buffer

Both input and clock buffers have been implemented as Current Mode Logic (CML) gates which are based on differential amplifiers with resistive loads. Their differential topology ensures their immunity to common mode noise as power supply boise and variations. In addition, low resistive load values have been chosen to increase the bandwidth that helps in reducing both the value and the temperature drift of their propagation time at the expense of power consumption.

The pulse input Buffer could be configured to comply with pulses having different input common modes ranging from 0.9 to 2.9V and different amplitudes. The pulse input buffer is compliant with LVPECL, CML and LVDS pulse formats.

D-CML

A differential CML D latch has been implemented for on-chip pulse synchronization purpose.

In a first mode, the D-latch is enabled and is used to resynchronize the input pulse on the rising edges of the high frequency master clock.

In a second mode, the D-latch could be deactivated. It is then configured as a CML buffer to allow out of chip pulse resynchronization.

Programmable Delay Generator

As depicted in Fig. 1, the core delay generator is based on the linear charging of a capacitor with the help a constant current source [6]. A comparator is used to generate the delayed pulse once the capacitor voltage drops below a comparison voltage. The delay tuning is obtained by controlling this comparison voltage through the use of a 14-bit DAC.

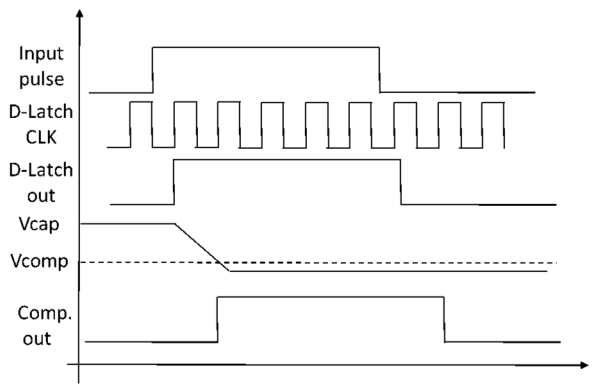

Figure 2: Timing diagram.

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The linearity of the architecture relies strongly on the 14-DAC linearity as well as on the linearity of the capacitor charging.

For the sake of linearity, the 14 bit DAC has been implemented as a segmented current steering DAC. A thermometric architecture has been chosen for the 10 MSBs while a binary structure has been chosen for the 4 LSBs ensuring a good trade-off between linearity and implementation complexity. The elementary current sources have been implemented using cascode structures to improve both linearity and power supply rejection.

The charging current source has been implemented using a switched capacitor current source scheme [7]. Indeed, a switched capacitor could be used to emulate a resistor whose value is given by (1):

$$R = \frac{1}{C_{sccc} * f} \quad (2)$$

where C_{sccs} is the capacitor used as the switched element and f is the switching frequency. The switched capacitor current source generates a current whose value is given by (3) [7]:

$$I = 2.C_{sccc}.f.V_{ref} \quad (3)$$

Where V_{ref} is the value of a reference voltage.

The switched capacitor current source is used as the reference current of a 10-bit DAC which current output is used to charge the delay generator integrating capacitor. The 10-bit DAC allows the control of the slope of the voltage ramp across the integrating capacitor. The control of the slope is advantageously used to calibrate the full scale of the delay as explained latter.

As depicted in Fig.1, the switched capacitor current source and the 14-bit DAC that sets the comparison voltage share the same V_{ref} generator. In this condition the delay generated by the core delay generator could be expressed by (4):

$$\tau_{gen} = \frac{n}{2}.\frac{R}{R_{refdac}}.\frac{C}{C_{sccc}}.\frac{1}{f} \quad (4)$$

Where n is the 14-bit DAC code, R is the load resistance converting the 14-bit current steering DAC into the comparator voltage, R_{refdac} the resistor converting the V_{ref} into the 14-bit DAC current reference, and C the delay generator integrating capacitor. It is worth noting that the delay depends only on the master clock frequency, and on ratios of capacitance and resistance. Using the same kind of resistors and the same kind of capacitor leads to a temperature independent architecture. Moreover, it ensures good robustness over manufacturing process and matching variations.

The delay comparator has been implemented as a multistage differential amplifier in order to get high gain while no sacrificing bandwidth for the sake of lowering the comparator aperture time and thus its jitter contribution.

Channel Multiplexer

A differential CML multiplexer has been implemented that helps in combining the delay generator output with the outputs of the other channels. In a first mode, the multiplexer outputs the core delay generator. In a second mode, the multiplexer recombines the core delay generator with either one other channel or the three others.

In the 2-channel combination mode, the performed operation at channel 1 and 3 outputs are:

$$Out_{ch1} = Out_{Ch1} \,\&Out_{Ch2} \quad (5)$$

$$Out_{ch3} = Out_{Ch3} \,\&Out_{Ch4} \quad (6)$$

In the 4-channel combination mode the performed operation at channel 1 output is:

$$Out_{ch1} = Out_{Ch1} \,\&Out_{Ch2} + Out_{Ch3} \,\&Out_{Ch4} \quad (6)$$

Both combination modes could be used advantageously to produce very narrow pulses.

Biasing

The biasing of the different blocks involves a bandgap reference that ensures low dependency to temperature and voltage supply variations. The bandgap voltage is converted into a current with the help of a resistor. The current is then mirrored and applied to all CML gates of the pulse path. The resistor is of the same type as used in the CML gates in the pulse path to ensure a constant voltage amplitude at CML gates outputs over voltage and supply voltage variations.

Calibration

The chip embeds a Finite State Machine (FSM) allowing the automatic calibration of the full scale of the delay range. Indeed, a calibration is needed to ensure that all channels are matched in term of insertion delay and full scale that should match the period of the high frequency clock [8].

The calibration begins by the choice of a reference channel and the channel to be calibrated. First, the user chooses the code that corresponds to the minimum delay and apply it onto the reference channel. Then the calibration FSM searches for the code to be applied on the channel to be calibrated to get the same delay. For that purpose, a pulse is generated and applied on both channels. A phase detector (lead/lag detector) is used to measure the delay difference between the reference channel and the channel to be calibrated.

In the second step, the user chooses the full scale in term of DAC code that should correspond to the period of the high frequency clock. The code obtained in step one is added to the chosen full scale. Then a pulse is applied to both channels. The phase frequency detector measures the delay difference between the reference channel and the channel to be calibrated. The FSM then adjusts the slope of the integrator to match the delay between the two channels by playing on the code applied on the 10-bit DAC of the switched capacitor current source.

Once the three channels calibrated, one is choose as the new reference channel for the full scale calibration of the former reference channel.

Programmability

All the configuration words of the chip could be written and read in on-chip registers with the help of a standard SPI interface.

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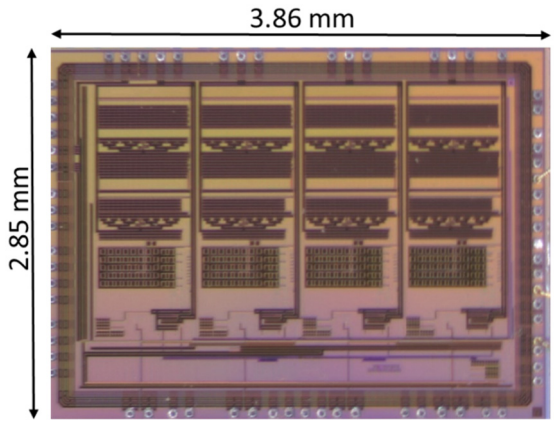

Figure 3: Chip microphotograph.

MEASUREMENT RESULTS

Test Setup

The 4-channel delay generator has been implemented in a 180 nm CMOS technology and packaged in a 56-QFN package. As depicted in Fig. 3, the overall area is about 11 mm2.

A 4-layers test board has been designed for test purpose. It embeds a dedicated socket that permits the easy replacement of the Device Under Test (DUT). For the sake of test automation, multiplexers have been implemented on board to direct the input pulse to the particular channel to be tested.

Figure 4 depicts the setup of the test bench. Anritsu MP1763C pattern generator has been used to generate both the LVPECL high frequency clock and the differential CML input pulse, both with very low jitter. The LVPECL output signal is monitored using a 40 GS/s Lecroy Waverunner 8404M oscilloscope that allows jitter measurement down to 1 ps. The chip is supplied with the help of low noise power supply. A Thermostream ATS thermostat has been used for temperature stabilization purpose.

Measurement Results

A 3.3 Volt power supply is necessary to bias the input, output and clock IOs. All the other blocks are biased with the help of 1.8 Volt power supply. When all the 4 channels are biased, the measured power consumption is 350 mW.

Figure 5 depicts the delay, INL and jitter versus the 14-bit input code. They are measured under nominal conditions (30°C, 1.8V, 3.3V) for one of the 4 channels, and for master clock frequencies ranging from 125 MHz to 250 MHz, which is larger than the 150 to 200 MHz specified range. It could be seen that the delay full scale over the 14-bit code always exceeds the master clock period as expected. The measured delay step ranges from 400 fs for a 250 MHz master clock to 730 fs for a 125 MHz master clock frequency.

Measured worst case for the INL is about 100 LSBs which represent almost 40 ps for a 250 MHz master clock frequency and represents less than 0.7% of the full scale,

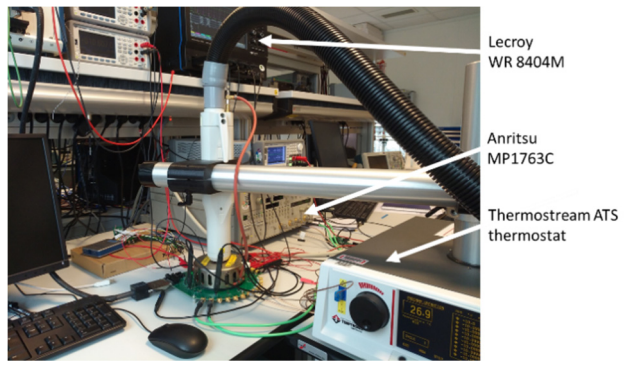

Figure 4: Test bench setup.

which is well into specification.

As expected, the jitter improves when the frequency of the master clock increases, as a higher master clock frequency induces a faster ramp voltage across the integrating capacitor of the core delay generator. One could easily see that the jitter degrades when increasing the code of the 14-bit DAC. This could be easily explained as a higher code implies a longer integration time that results in more noise to be integrated onto the integrating capacitor. Worst case jitter is 2.4 ps for the largest code at 125 MHz. However, it remains below 2ps for the targeted frequency range (150 to 200 MHz) of the master clock.

Figure 6 depicts the delay, INL and jitter measurement over temperature ranging from -10 to 90 °C. The delay measurement shows a drift of the delay with temperature of about 8 ps/°C. Nevertheless, a 2.5ps/°C temperature drift has been measured once the chip is soldered on a test board for a reduced temperature range.

The jitter degrades with higher temperature as it could be expected. Nevertheless, it remains below 2 ps for the specified 0, 60° C range.

CONCLUSION

In this paper a fully integrated 4-channel 400 fs time step delay generator compliant with modern physics experiments has been presented. It includes several new functionalities as on-chip input pulse resynchronization, channel recombination circuits and automatic full scale calibration. Measurement over temperature (0- 60°C) and supply voltage have confirmed a time step of 400 fs, a jitter of 1.8 ps and a controllable full scale range from 6 to 12 ns corresponding to master clock frequency ranging from 250 MHz to 125 MHz respectively. The measured power consumption is about 350 mW when all the 4 channels are activated.

The delay generator has been packaged in small 56-QFN package It paves the way to the design of very low volume fine steps delay generators or the design of delay generators with very number of delay channels.

A second version is currently under design with availability scheduled in 2020. This second version targets improved temperature drift and jitter performances. It will embed a buffered register bank, allowing the simultaneous writing of all the configuration registers through the use of a dedicated “load registers” pin.

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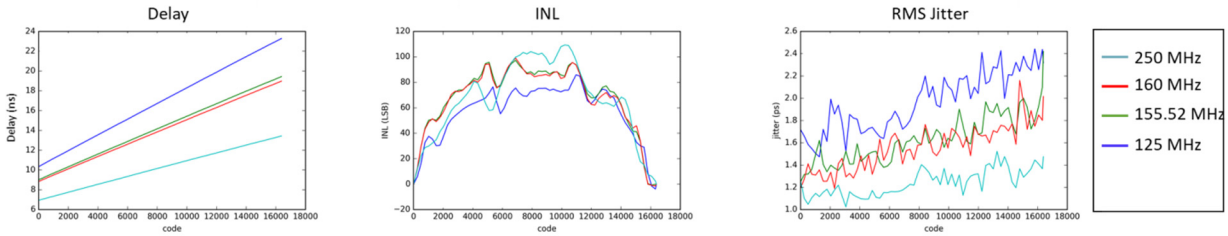

Figure 5: Delay, INL and RMS jitter measurement for different reference frequency.

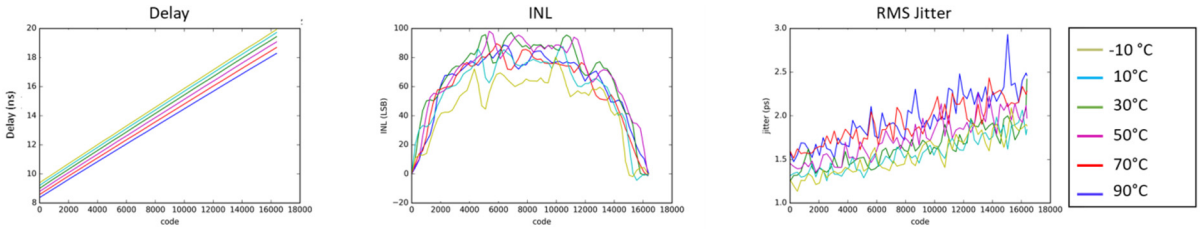

Figure 6: Delay, INL and RMS jitter versus temperature.

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