

16th International Conference on Accelerator and Large Experimental Physics Control Systems

Porting VME-Based Optical-Link Remote I/O Module to a PLC Platform

- an Approach to Maximize Cross-Platform Portability Using SoC

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Outline

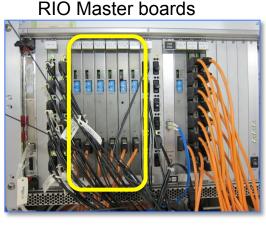
- Background
 - Optical-linked remote I/O system
 - Platform consideration
- Development of module
 - Design policy
 - Hardware implementation
 - Software implementation
 - Implementation of FPGA logic
- Summary



- VME
 - employed at SPring-8 as FE computers.
- Optical-linked Remote I/O systems
 - utilized to cover widely distributed accelerator equipment.
 - consist of VME-based master boards and several kinds of slave boards.
 - two types of optical-linked remote I/O system
 - RIO system
 - *OPT-VME system*



- RIO system
 - developed by Mitsubishi Electric Co.
 - used since 1997, already **discontinued**.
 - employ over 1,400 slave boards in SPring-8.
 - mainly for SR magnet power supplies control.
 - many of them can be replaced with *OPT-VME system*.
 - developed the compatible slave boards.



RIO Slave boards





- OPT-VME system
 - developed by SPring-8 at 2001.
 - two types of **VME-based** master boards.
 - OPT-VME
 - OPT-CC

OPT-VME: 4ch single-slot VME board



OPT-CC: 12ch dual-slot VME board





- OPT-VME system
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 - two types of **VME-based** master boards.
 - OPT-VME
 - OPT-CC
 - employ over 400 slave boards in SPring-8.
 - 10 types of slave boards are available.

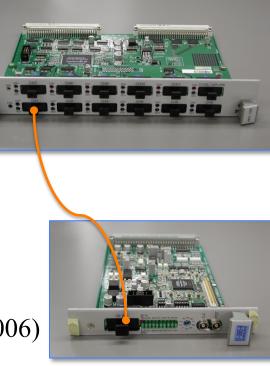
a kind of slave board



Used for steering magnet PSs control at the booster ring.

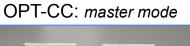


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 - two types of **VME-based** master boards.
 - OPT-VME
 - OPT-CC
 - employ over 400 slave boards in SPring-8.
 - 10 types of slave boards are available.
 - original communication protocol (OPT-Protocol 2006)
 - Only support point-to-point connection.

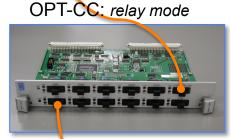




- OPT-VME system
 - ОРТ-СС
 - also available in the relay-mode.
 - max. 132 slave boards can be controlled from a master.





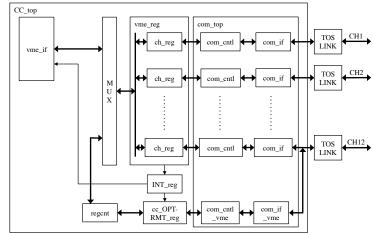


slave board





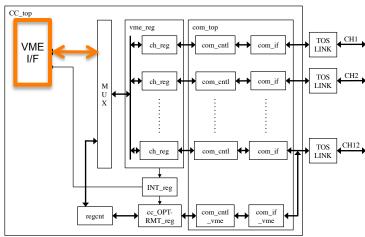
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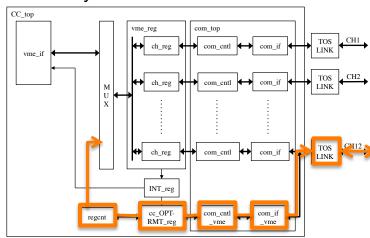
In a master mode





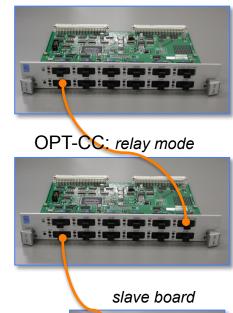
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 - communication procedure with the remote slave board is **implemented in the device driver** for the master board.



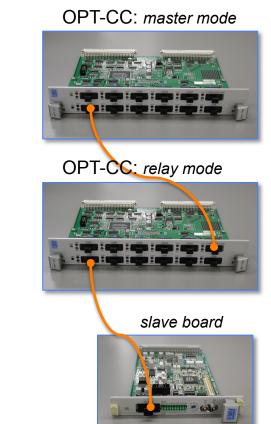
OPT-CC: master mode





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The device driver is responsible for the high-level communication procedures including the remote slave control.





Platform Consideration

• VME

- Passed over 30 years, become out-of-date.
- Two major issues;
 - Lack of bandwidth.
 - Discontinued the de-fact standard bus-bridge chip Tsi148.

 \rightarrow This has been a big problem for VME users.

• considering the next-generation alternative platform.



Platform Consideration

• MTCA.4

- Decided to introduce MTCA.4 as a high-end platform.
- Analog-based old SR LLRF system controlled by VME is planed to be replaced with MTCA.4-based digital LLRF system.





Platform Consideration

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- Linux PLC (Programmable Logic Controller)
 - one of the candidate to **cover a low-end side**.
 - e.g. e-RT3 (FA-M3) by Yokogawa Electric Co.
 - already applied as front-end computers in both SPring-8 and SACLA.



- Developed the new master module of the OPT-VME system based on the e-RT3 platform.
 - To effectively utilize the resources of large amount of *OPT-VME* slave board (~400).
 - RIO slave boards (~1,400) are also integrated by replacing OPT-VME based compatible slave boards.
 - Considering alternative platform portability such as a PCI Express (MTCA.4)



Development of the new master module

• OPT-PLC

 e-RT3-based new master module for the OPT-VME system.

SoC	Xilinx Zynq 7015 : XC7Z015-1CLG485C
Memory	1GB DDR3-SDRAM 128MB QSPI Flash
LAN	1 port (RJ-45 Connector)
MicroSD	1 port (Micro-SD socket)
UART	1 port (Micro-USB connector)
High-Speed Serial I/F	4 pairs x 6.25GBps in a 70pins stacking connector (Molex 53625-0774)
JTAG	1 port
Power	+5V±5%





OPT-PLC module

- Design Policies
 - 1. Equip with as many optical channels as possible.
 - 2. Separate an I/O unit from a logic control unit.
 - 3. Control the module using the e-RT3 general-purpose device driver.
 - 4. Control the module from a sequence CPU in addition to a Linux CPU.



OPT-PLC module

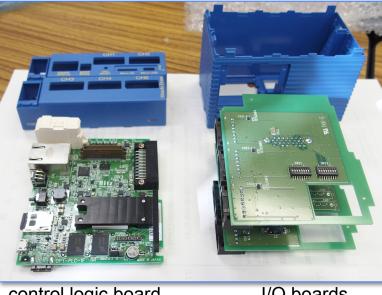
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Hardware Implementation

- Consists of three PCBs.
 - Separate two I/O boards from the control logic board.
 - Connected using 70 pins stacking connector each other.
 - *PCB* is a little small to mount the FMC.
- Equipped with 5 optical channels.



control logic board

I/O boards



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→ Implementation of Software & FPGA logic



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→ Implementation of Software & FPGA logic
Keyword : SoC



e-RT3 General-Purpose Device Driver

- supplied and supported by Yokogawa Electric Co.
- primitive device driver to handle memory access and interrupt.



e-RT3 General-Purpose Device Driver

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Background

ICALEPCS2017

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master board.

The device driver is responsible for the high-level communication procedures including the remote slave control.



OPT-CC: master mode



slave board



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CALEPCS2017

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OPT-CC: relay mode

How do we implement this high-level communication procedures?

board is implemented in the device driver for the

master board.

The device driver is responsible for the high-level communication procedures including the remote slave control.

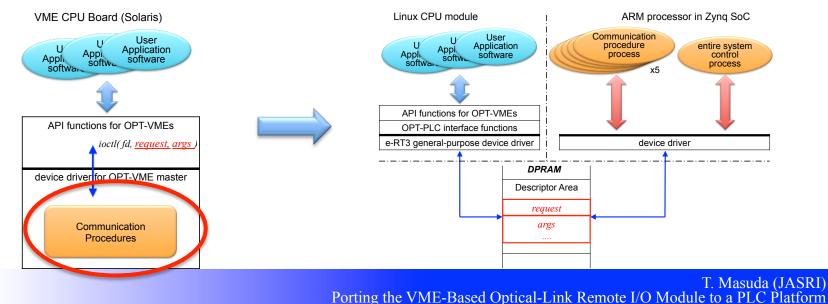
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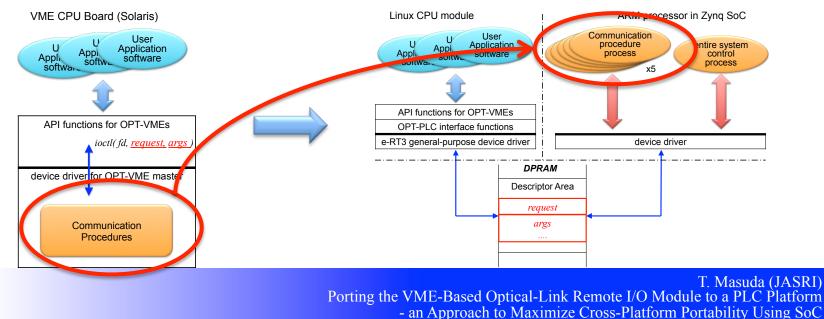
- Adopt SoC (Xilinx Zynq 7000)
- Implement the high-level communication procedures as application software running on ARM Linux in SoC.



- an Approach to Maximize Cross-Platform Portability Using SoC

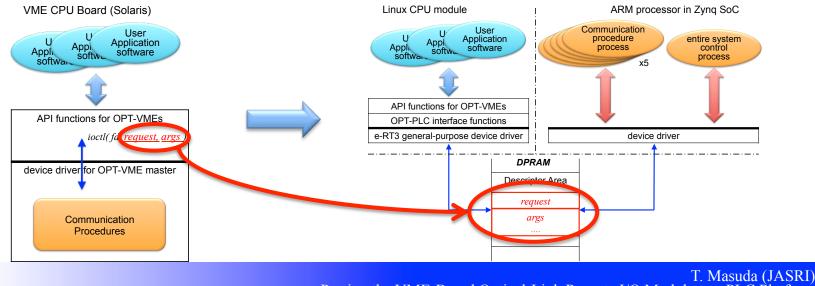


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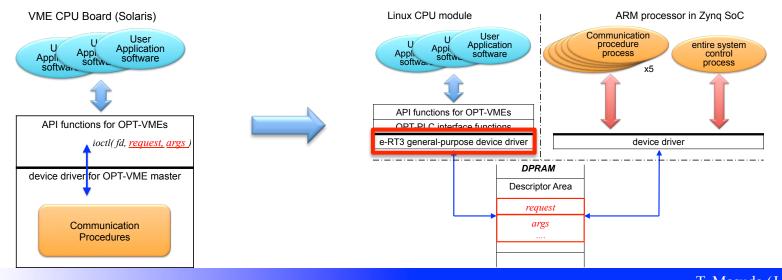
ICALEPCS2017

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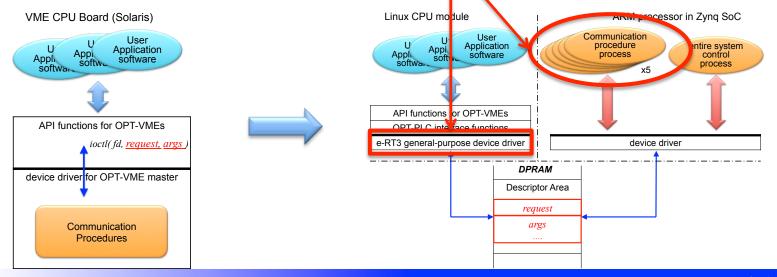


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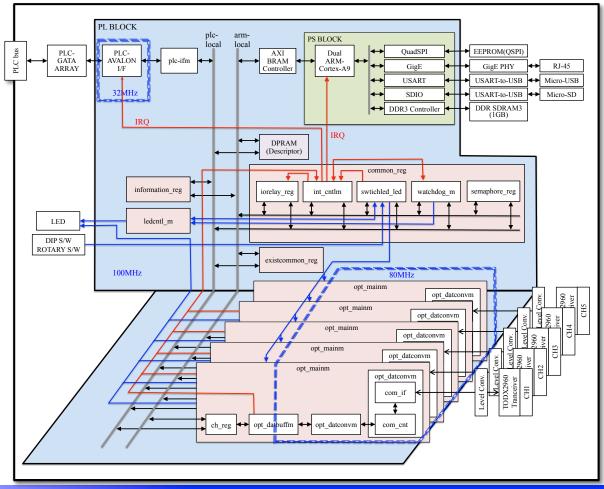


- Adopt SoC (Xilin) As a result the device driver of platform side is simplified, the module portability to other platform is enhanced. Implement the high-never communication procedures as application software running on ARM Linux in SoC.



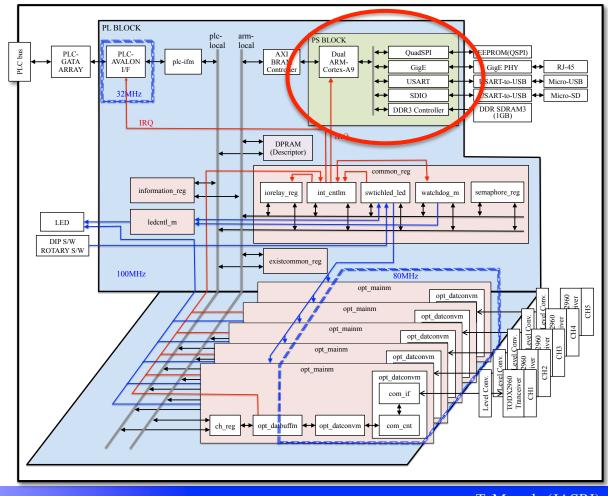


Implementation of FPGA Logic

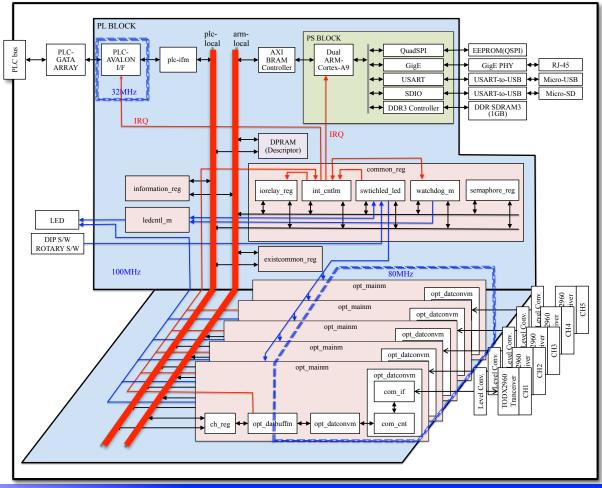




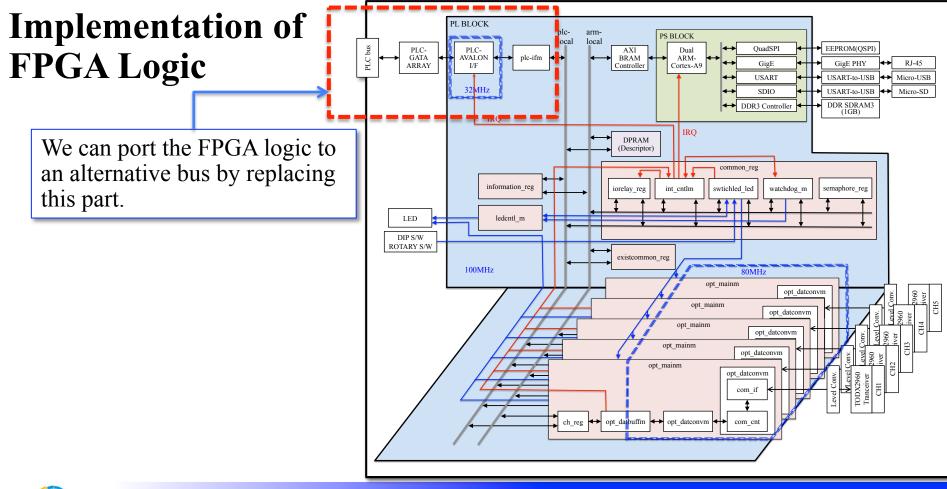
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Implementation of FPGA Logic









Summary

- We have successfully ported the VME-based optical-link remote I/O module to the e-RT3 platform.
- The developed module OPT-PLC is equipped with Zynq 7000 SoC to build the communication procedures as the application S/W on the ARM Linux.
 - the interface with the PLC bus is simplified and the e-RT3 general-purpose device driver is available.
- We can port the developed FPGA logic to an alternative bus e.g. the PCI express by replacing the PLC bus interface block in the PL part.
- The interface simplification enhances portability.





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Thank you for your attention.

