



User Experience in MicroTCA

Workshop Summary

Thomas Walter
DESY

Overview

■ Sessions

- **MicroTCA – Introduction to the Standard**
Kay Rehlich (DESY)
- **MicroTCA in Real Life**
Thomas Holzapfel (Powerbridge/ N.A.T.)
- **Implementation of MicroTCA for Beam Diagnostics and Synchronization**
Matthias Felber (DESY)
- **Scalability of MicroTCA.4 Systems**
Thomas Holzapfel (Powerbridge)

■ Attendance: ~ 50



Key Takeaways

- 1 Community active & growing
- 2 Scalability: starter kits added to portfolio
- 3 MicroTCA standard continues to evolve
- 4 Tool sets
- 5 MicroTCA beyond Physics
- 6 Applications portfolio keeps growing
- 7 European XFEL: MicroTCA works!



1 Community active & growing



6th MicroTCA Workshop for Industry and Research
6th - 7th December 2017
DESY, Hamburg

microTCA
TECHNOLOGY LAB
A HELMHOLTZ INNOVATION LAB

Email: thomas.walter@desy.de

Mobile: +49 175 5080 473

<http://mtcaws.desy.de/>

1 Community active & growing



2 Scalability: starter kits added to portfolio

- open, mature, robust Standard
- extremely scaleable
- ecosystem is intact
- big variety of different processor boards
 - X86, Freescale, ARM
 - GPGPU, FPGA, DSP
- big variety of I/O-functions available
 - dedicated AMC modules
 - carrier cards (IP, PMC, XMC, FMC)
- variety of chassis
 - From small to big
- highspeed interfaces
 - Up to PCIe x8, Gen.3
 - Ethernet 1,10,40GbE
 - SRIO Gen.2
 - 2018 upcoming SRIO Gen.3 and PCIe Gen.4

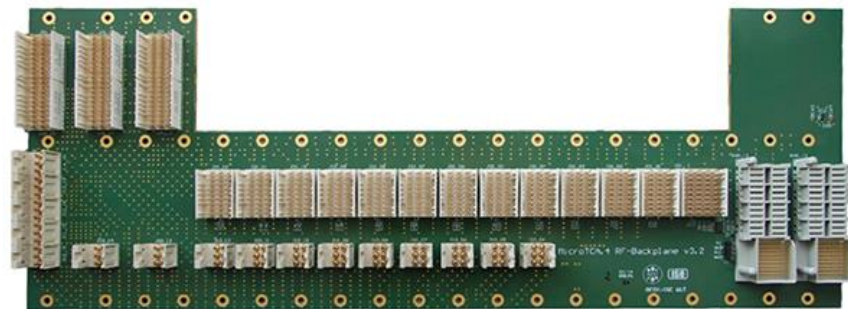


Source: Scalability of MicroTCA.4 Systems - Thomas Holzapfel (Powerbridge)

3 MicroTCA standard continues to evolve

- MicroTCA 4.1: new hardware extensions
 - additional rear backplane
 - supports both precision analog and digital functions
 - ancillary Rear Power Modules
 - used in XFEL
- New Backplanes: 40G (and beyond)

Source: <https://www.picmg.org/openstandards/development/>



Source: N.A.T. GmbH



4 Tool Sets

Version 2.20 De (Revision #1207)

Licensed option

- FRU Editor
- Backplane View
- HPM Update
- MCH Scanner
- System Dump
- Event Log

NATview 2.25

Application Fru Sensor Tools Help

Auto Update: 1 seconds

Resources of system 192.168.137.185

- [003] N.A.T. GmbH - Germany NAT
- [005] N.A.T. GmbH - Germany NAM
- [006] N.A.T. GmbH - Germany NAM
- [007] N.A.T. GmbH - Germany NAM
- [203] Temp CPU
- [202] Temp CPU max
- [201] Temp PCB
- [200] Temp PCB max
- [199] 1.0V
- [198] 1.2V
- [197] 1.5V
- [196] 1.8V
- [195] 2.5V
- [194] Current
- [193] HotSwap
- [192] HS 007 AMC3
- [008] N.A.T. GmbH - Germany NAM
- [009] N.A.T. GmbH - Germany NAM
- [010] N.A.T. GmbH - Germany NAM
- [011] N.A.T. GmbH - Germany NAM
- [012] N.A.T. GmbH - Germany NAM

Sensor # 203 / LUN 0: Temp CPU = 40.0 degree Celsius (n/a -- n/a)

Temperature (deg C)

40,00

	MIN	MAX
non-critical	8.0	75.0
critical	4.0	80.0
non-recoverable	2.0	110.0

Edit thresholds Cancel

Update

Source: MicroTCA in Real Life Thomas Holzapfel (Powerbridge/ N.A.T.)

5 MicroTCA beyond Physics

Markets

Our diverse membership allows PICMG to develop compelling specifications in multiple markets. PICMG technologies are widely used in a broad swath of industries including industrial automation, military/aerospace, transportation, communications, test/measurement, physics/research, energy, medical, and more!

	COM Express	AdvancedTCA	CompactPCI	CompactPCI Serial	HPM	MicroTCA / AMC	SHB
Industrial Automation	X		X	X			X
Gaming	X						
Telecommunications	X	X			X	X	
Aerospace	X		X	X	X	X	
Defense	X	X	X	X	X	X	X
Railway	X		X	X	X	X	
Energy	X		X	X	X	X	X
Medical	X		X	X	X	X	
Test / Measurement	X	X	X	X	X	X	
Physics		X			X	X	X
Drones / UAV	X		X	X	X	X	

Source: Scalability of MicroTCA.4 Systems - Thomas Holzapfel (Powerbridge)



6 Applications portfolio keeps growing

- Optical Synchronization System
- Diagnostic Systems & MTCA
 - Bunch Arrival Time Monitor
 - Bunch Compression Monitor
 - Electro-Optic Diagnostic
 - Beam Position Monitors
 - Charge Measurements
 - Beam Loss and Beam Halo Monitors
 - Wire Scanners



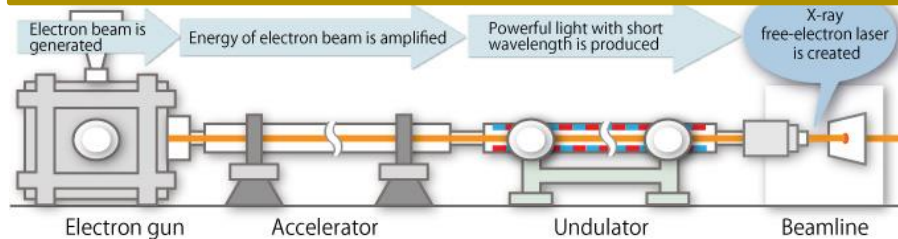
Source: Implementation of MicroTCA for Beam Diagnostics and Synchronization - Matthias Felber (DESY)

7 European XFEL: MicroTCA works!



The European X-ray Free Electron Laser

17.5 GeV light source user facility
TESLA superconducting 1.3 GHz RF cavities
1.4 msec RF pulses at 10 Hz
e- beam 1.35 mA nom. - 4.5 mA max
Dec. 18th 2015: first beam in injector
2015-2016: main tunnel installation
Q1 of 2017: main linac commissioning
May 4th 2017 : first lasing
End of 2017: first user operation



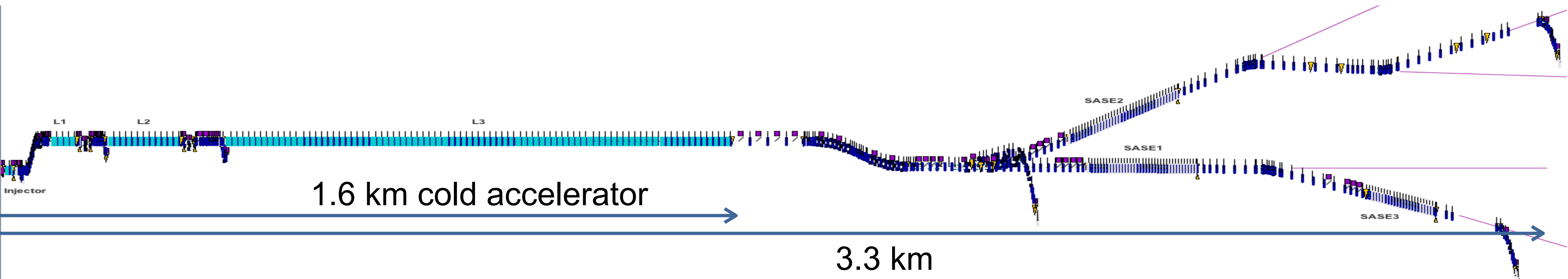
MicroTCA @ European XFEL

The Standard and its Usage

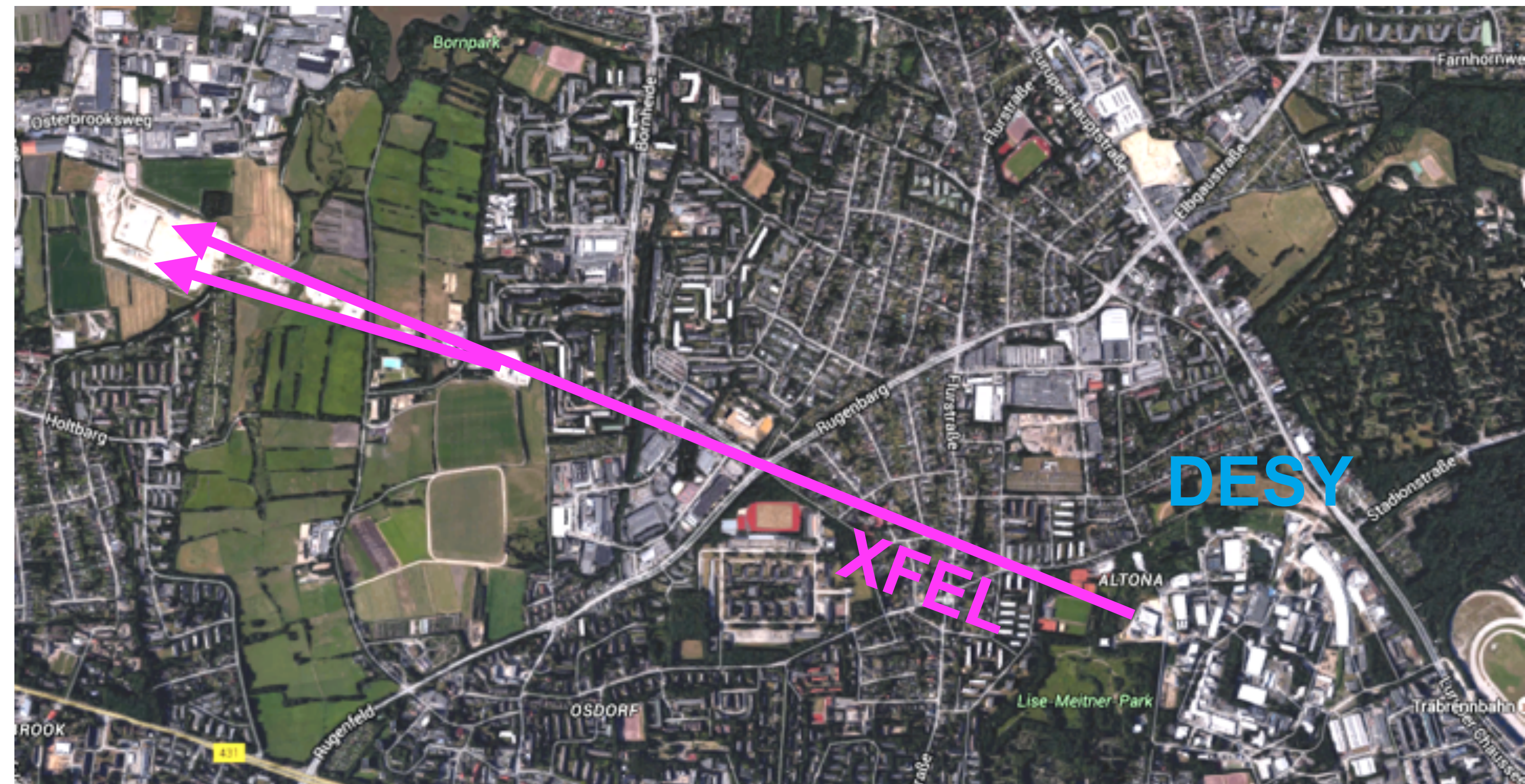
Kay Rehlich

DESY, MicroTCA Technology Lab

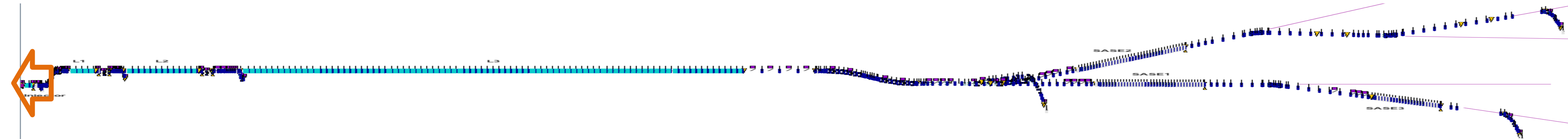
Outline



European XFEL
MicroTCA Systems
The MicroTCA Standard
Control System DOOCS

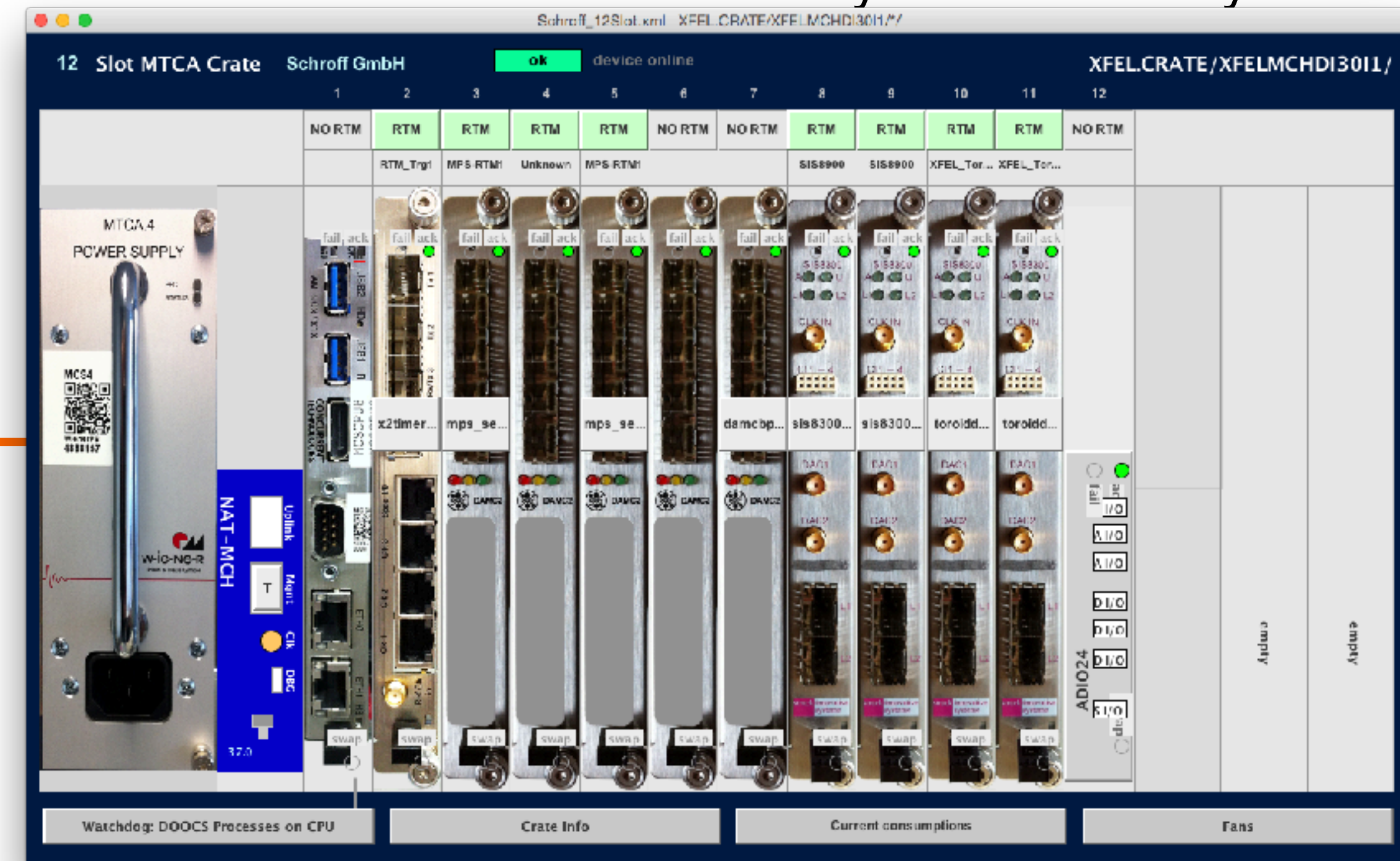


First MicroTCA Crate in the Injector

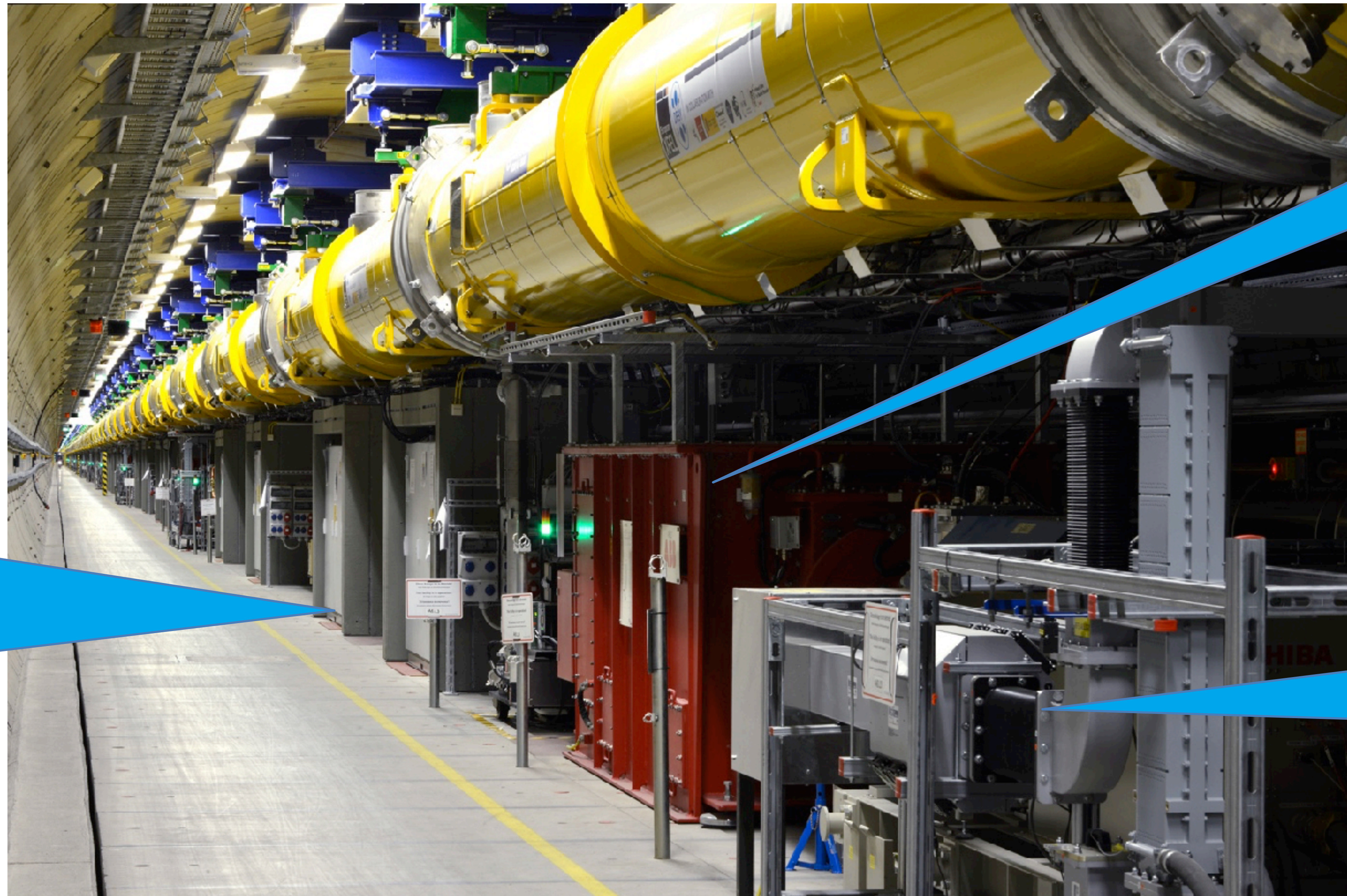
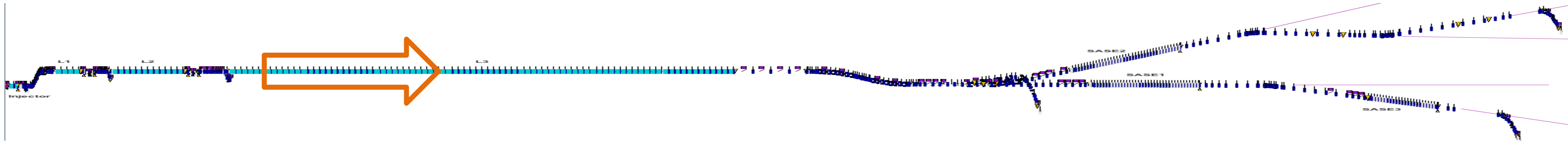


The Gun

One MicroTCA Crate as seen by the Control System



The Cold Linac



Racks for:

- Vacuum
- Cryo
- Magnets
- RF
- LLRF
- Coupler
- Diagnostics

Pulse
Transformer for
Klystron

10 MW Klystron
with
2 Wave Guides,
1.3 GHz

One RF Station = 4 Modules = 32 Cavities = 5 MicroTCA $\approx$ 50m



Coupler Interlock
Slave

LowLevel RF
Slave

Coupler Interlock
Master



Diagnostics
Vacuum, Magnets

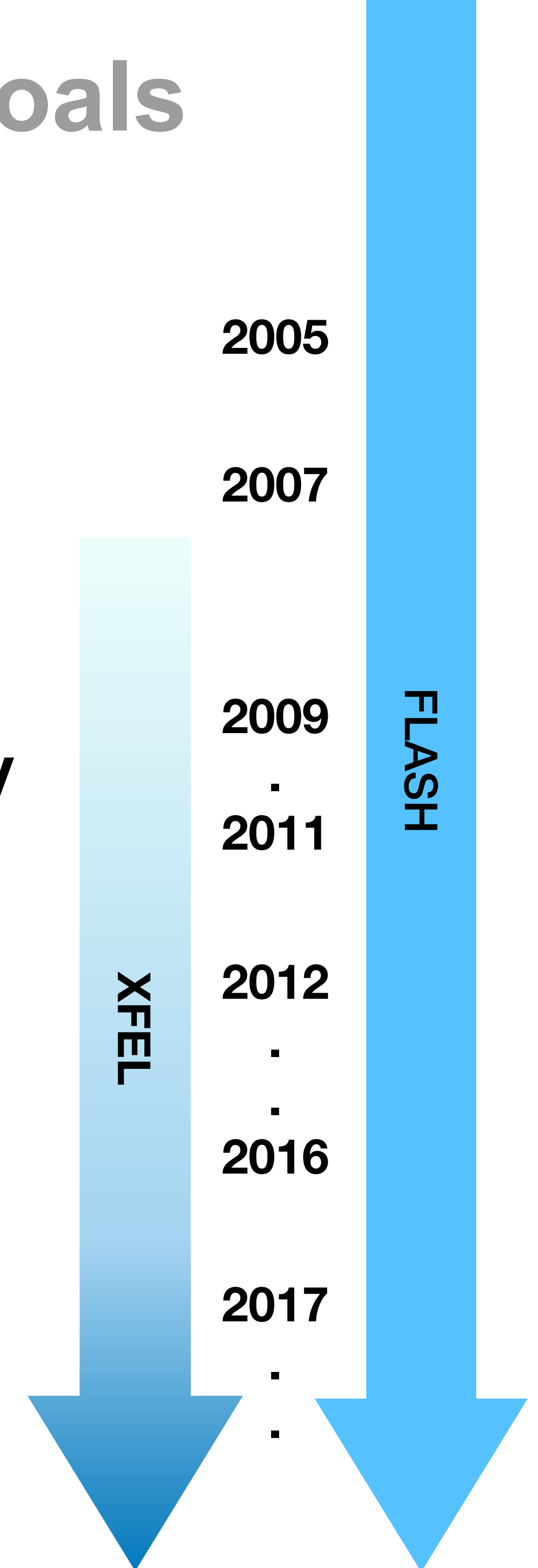
LowLevel RF
Master

XFEL Key Dates

- FLASH First lasing at 109 nm : 2000
 - Injector operation started: Dec. 2015
 - Main tunnel closed: 13. 1. 2017
 - First Beam in dump 2.5 GeV: 25. 2. 2017
 - 12 GeV in main dump: 8. 4. 2017
 - Beam permission SASE 1: 26. 4. 2017
 - Beam in SASE 1 dump (~1 km): 27. 4. 2017
 - First Light: 2. 5. 2017
 - User runs since: Sept. 2017
- 6 weeks:
2 km beam line,
700 cavities
- 

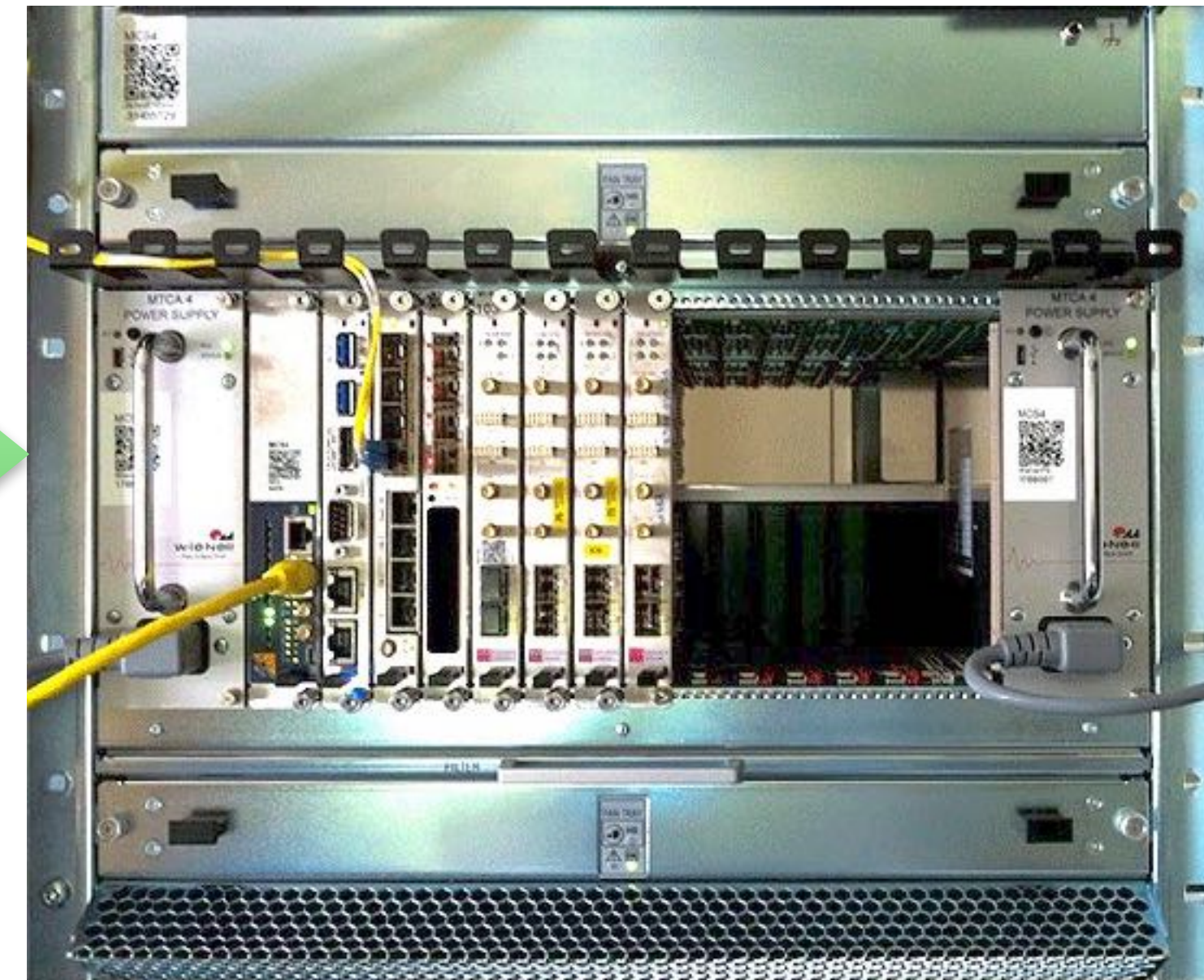
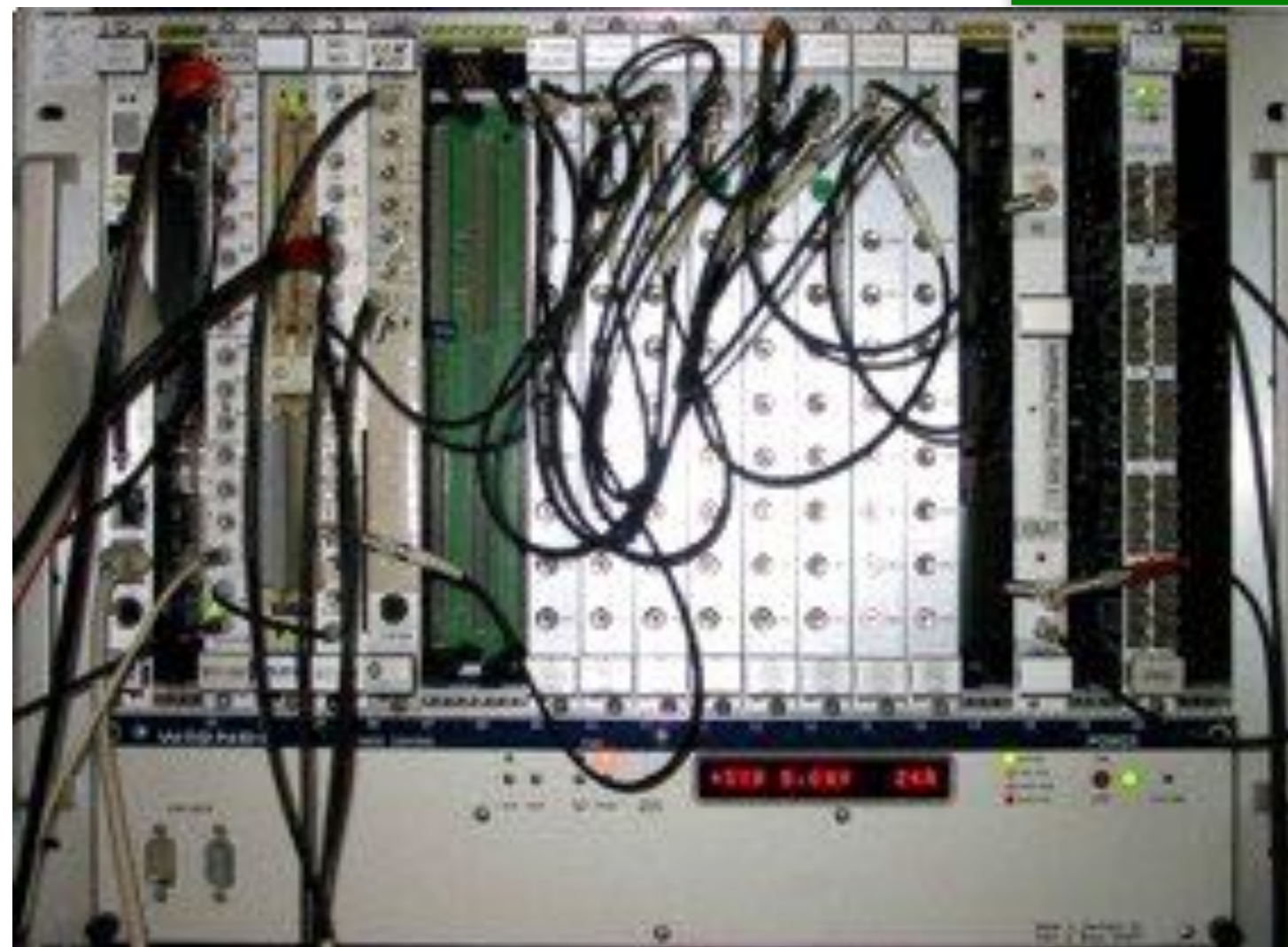
Important Milestones to Reach the Goals

- ◆ **Reliability** workshop ILC (30 km)
Availability with a huge number of subsystems: 0.999^N
- ◆ **XFEL Crate-Standard** workshop
Definition of the crate standard to use—> MicroTCA and ATCA
Building prototypes in-house and by industry
- ◆ **MTCA.4 PICMG** standard from accelerator-labs and industry
Collaboration to define specifications
- ◆ **Helmholtz Validation Fonds (4 Mil. €)**
In-house developments with licenses to industry
Product development by industry
Gaining a strong partnership
- ◆ **MicroTCA TechLab**



From VME (FLASH) → MicroTCA (XFEL)

VME is 35 years old!!!



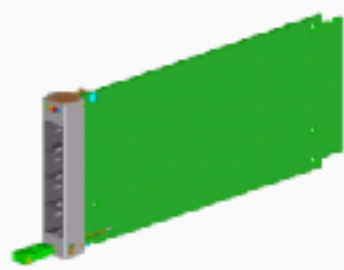
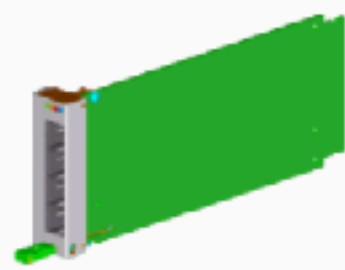
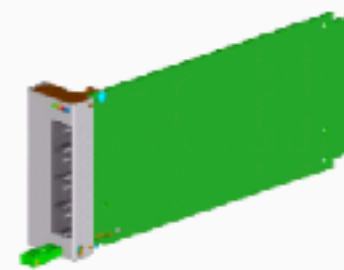
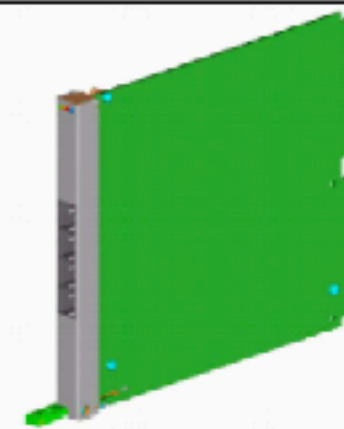
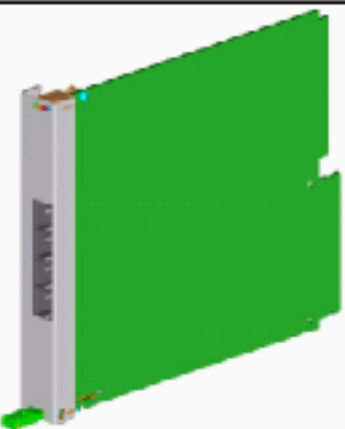
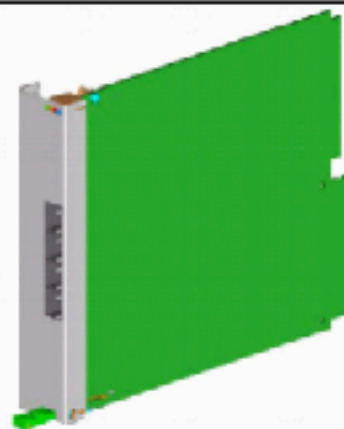
- Redundant fans & power supplies
- Internal clock & trigger distribution
- Modular: reusable components
- Complete remote management
- Modern high-speed data transfer
- Highest signal quality
- I/O cables from rear side

The ATCA & MicroTCA Standards

Advanced
Telecom
Computing
Architecture

Advanced
Mezzanine
Card

Micro
Telecom
Computing
Architecture

	Compact-Size (3HP)	Mid-Size (4HP)	Full-Size (6HP)
Single modules	 73.8x13.88x181.5mm	 73.8x18.96x181.5mm	 73.8x28.95x181.5mm
Double modules	 148.8x13.88x181.5mm	 148.8x18.96x181.5mm	 148.8x28.95x181.5mm



ATCA



MTCA.0

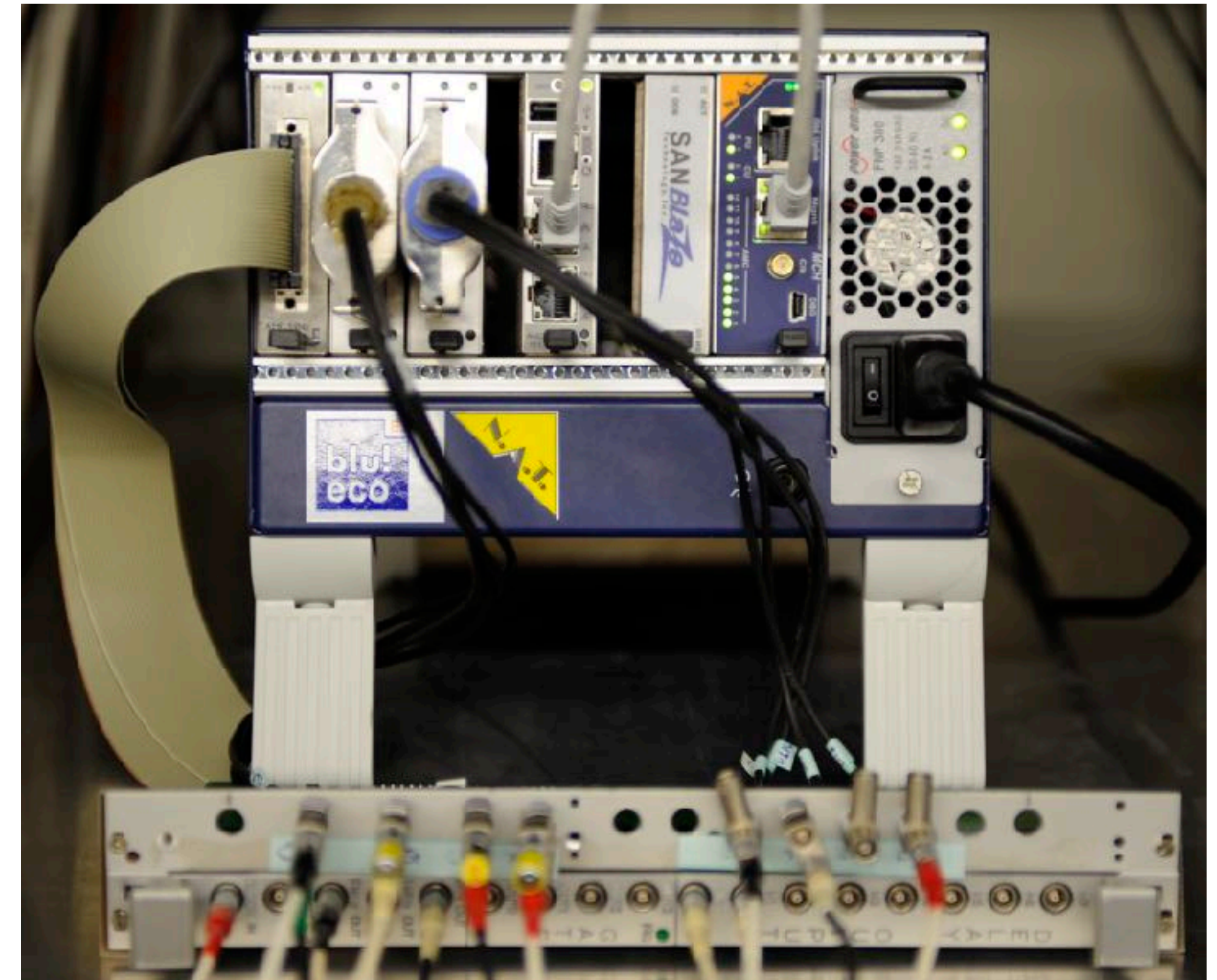
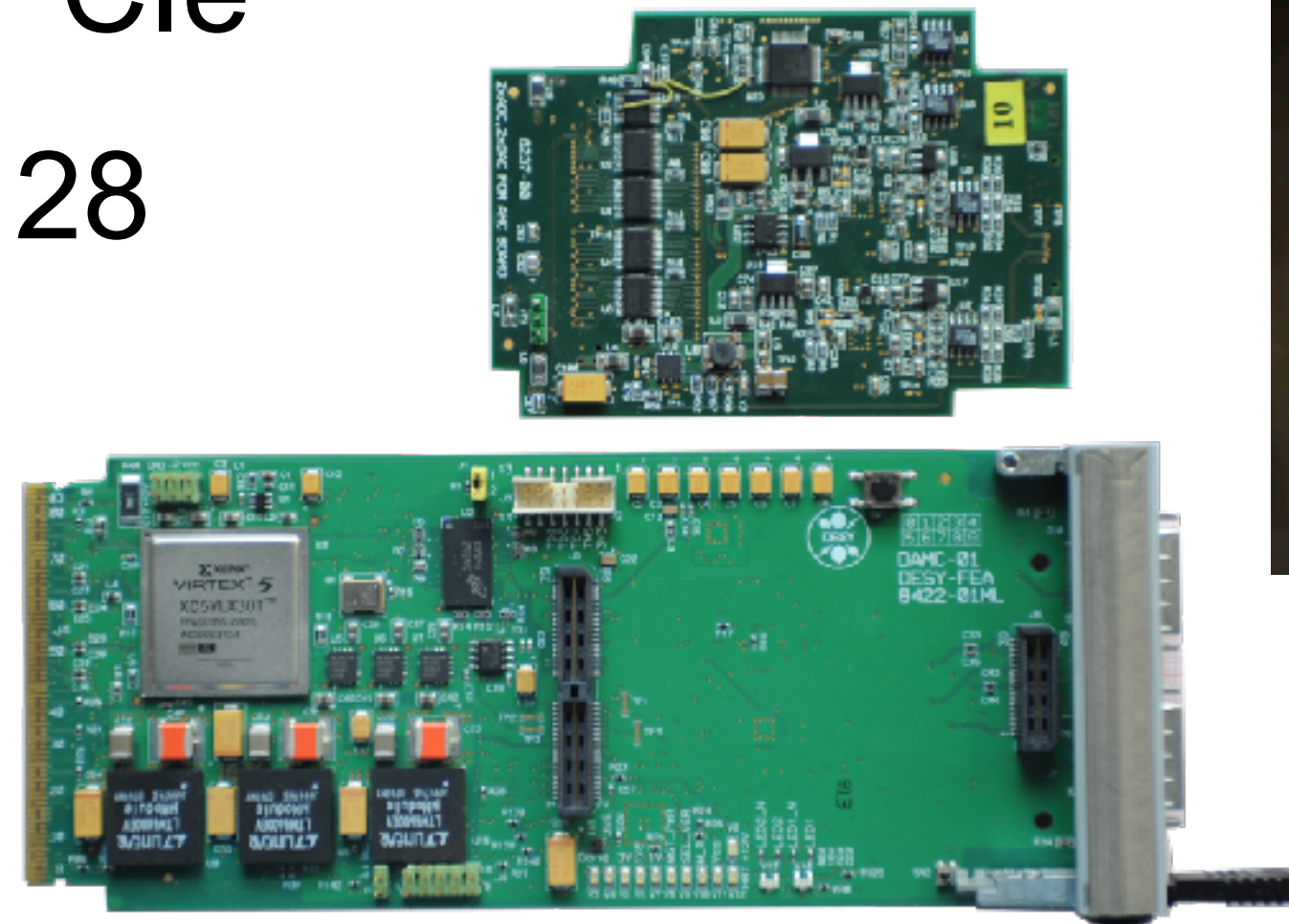


MTCA.4

Evaluation of MicroTCA: 2008

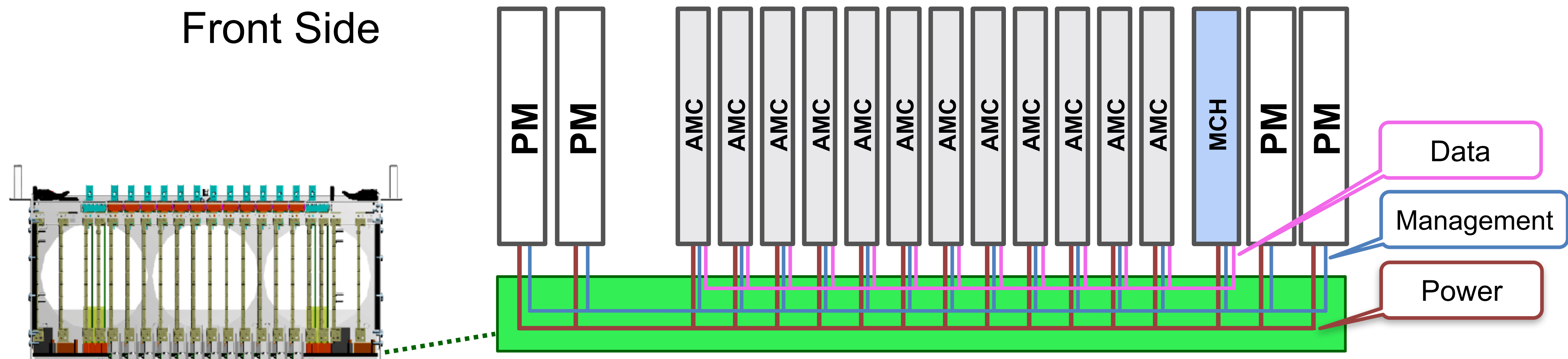
We started with MTCA.0 single modules:

- TAMC100 as carrier for IP Timing
- DESY development DMAC01 to understand the standard:
 - AMC with Virtex 5 and PCIe
 - MMC code on Atmega128
 - 2* ADC 100MSPS

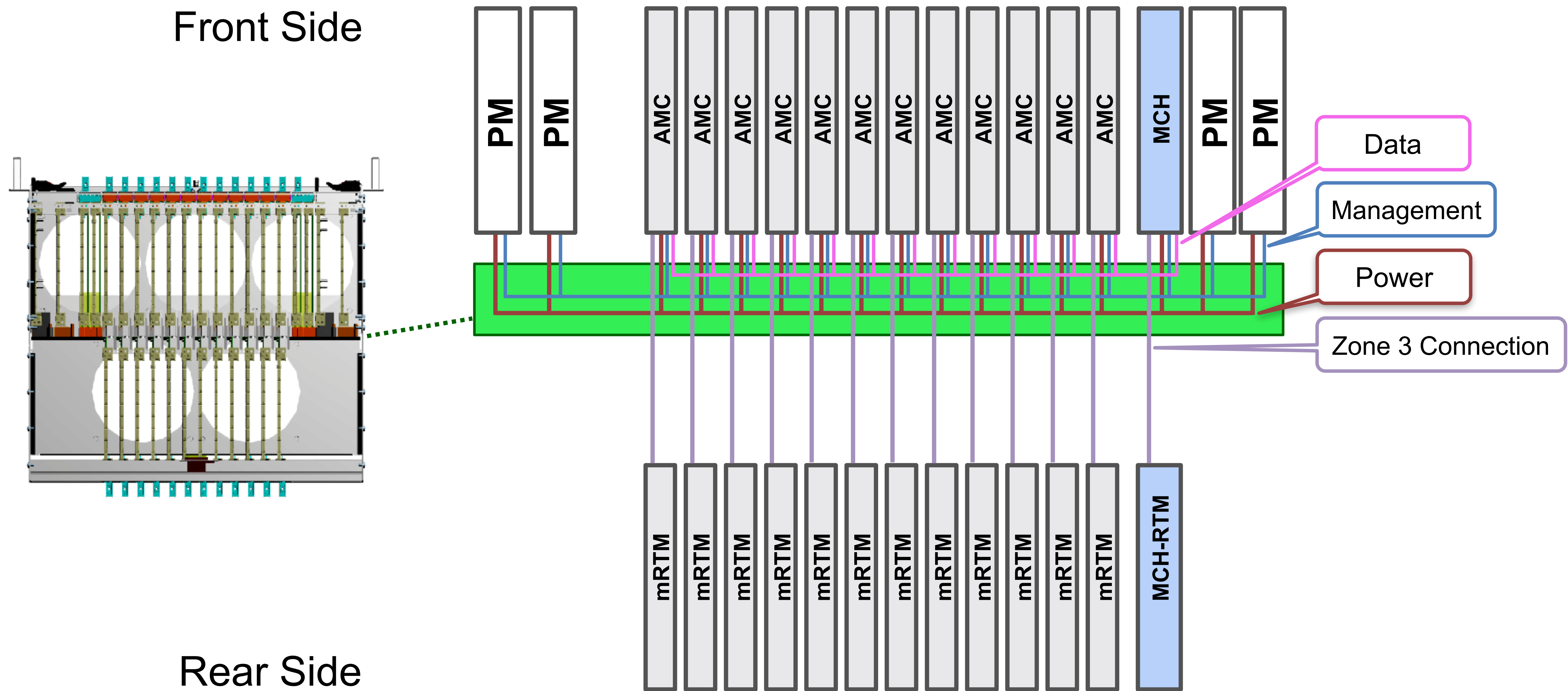


➡ Single modules are too small & cables from front are not optimal

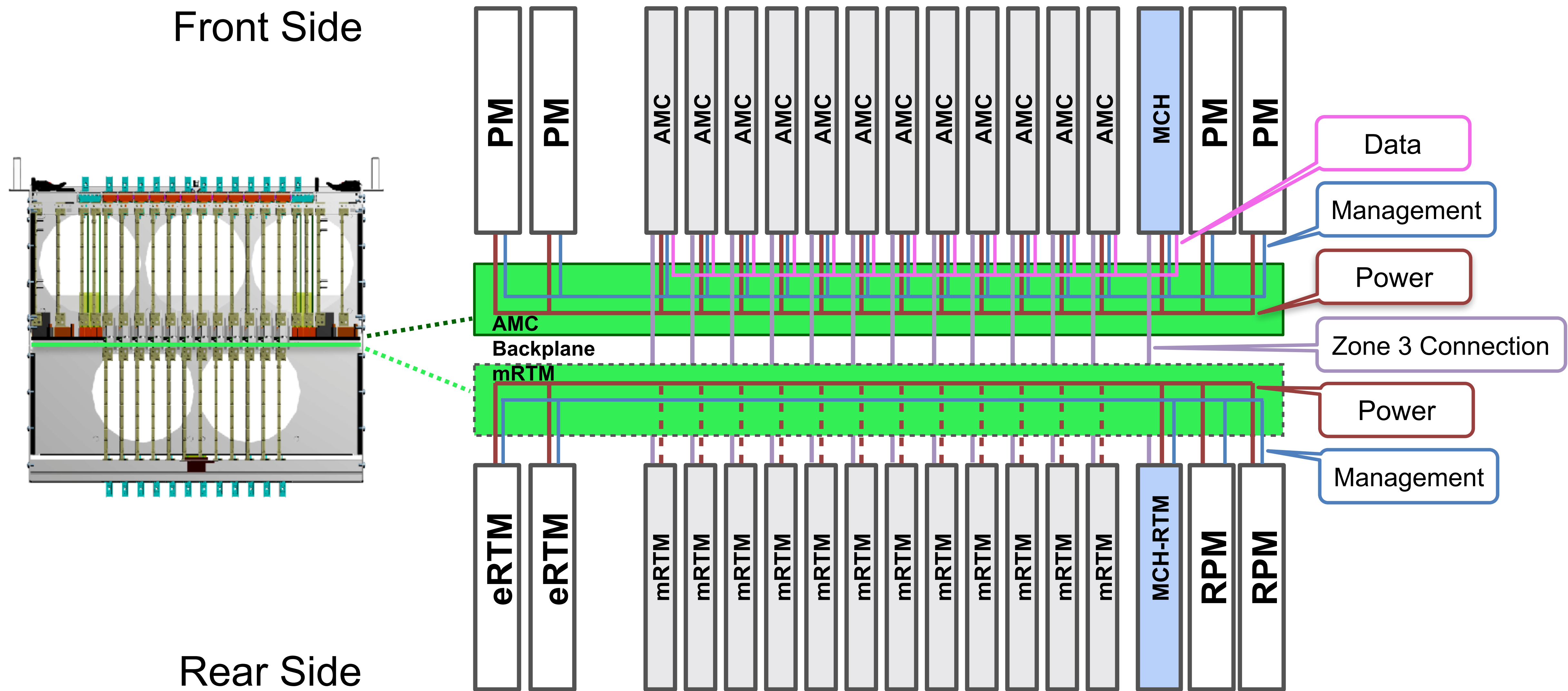
MicroTCA Generations: **MTCA.0** MTCA.4 MTCA.4.1



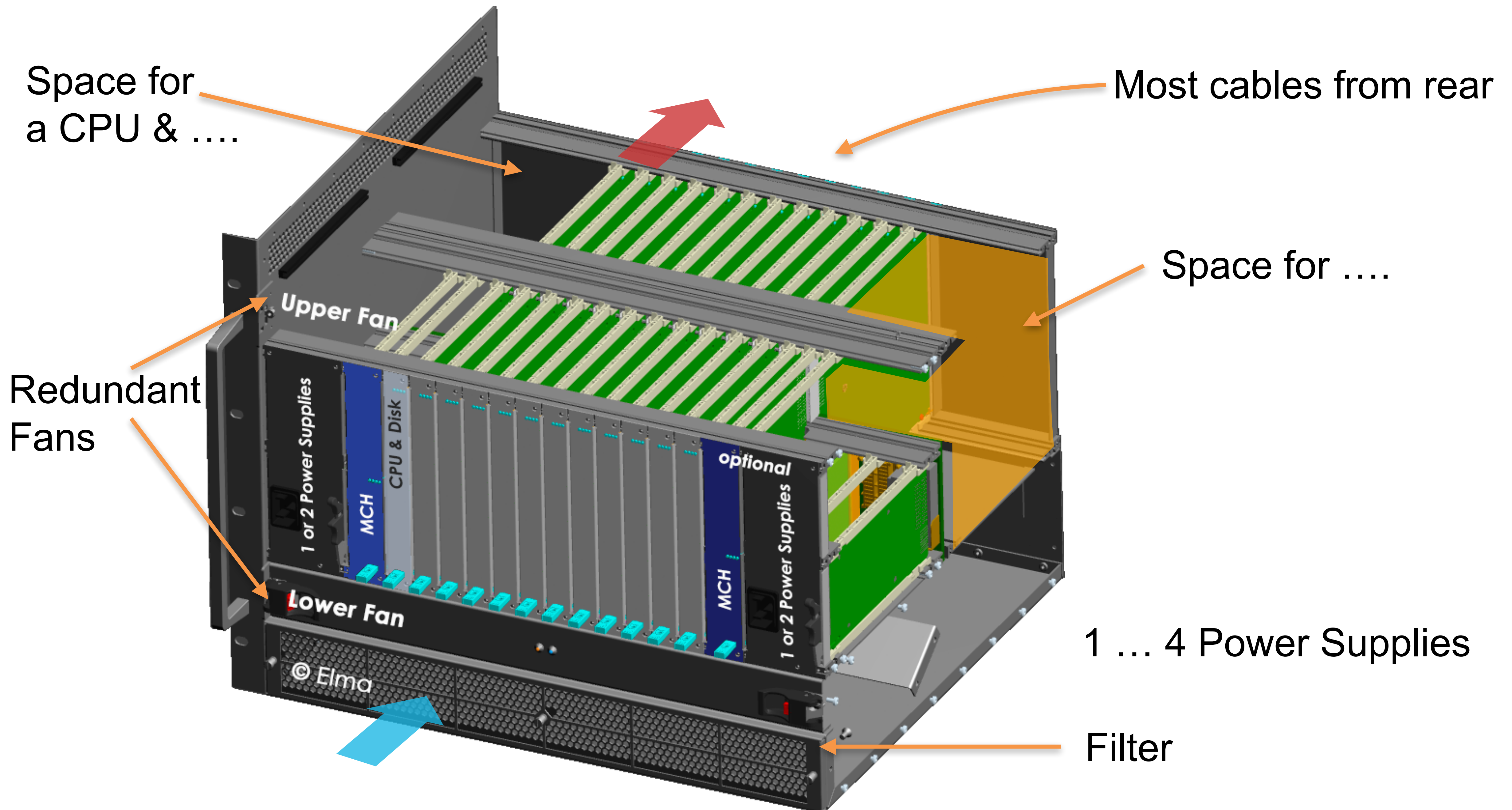
MicroTCA Generations: MTCA.0 **MTCA.4** MTCA.4.1



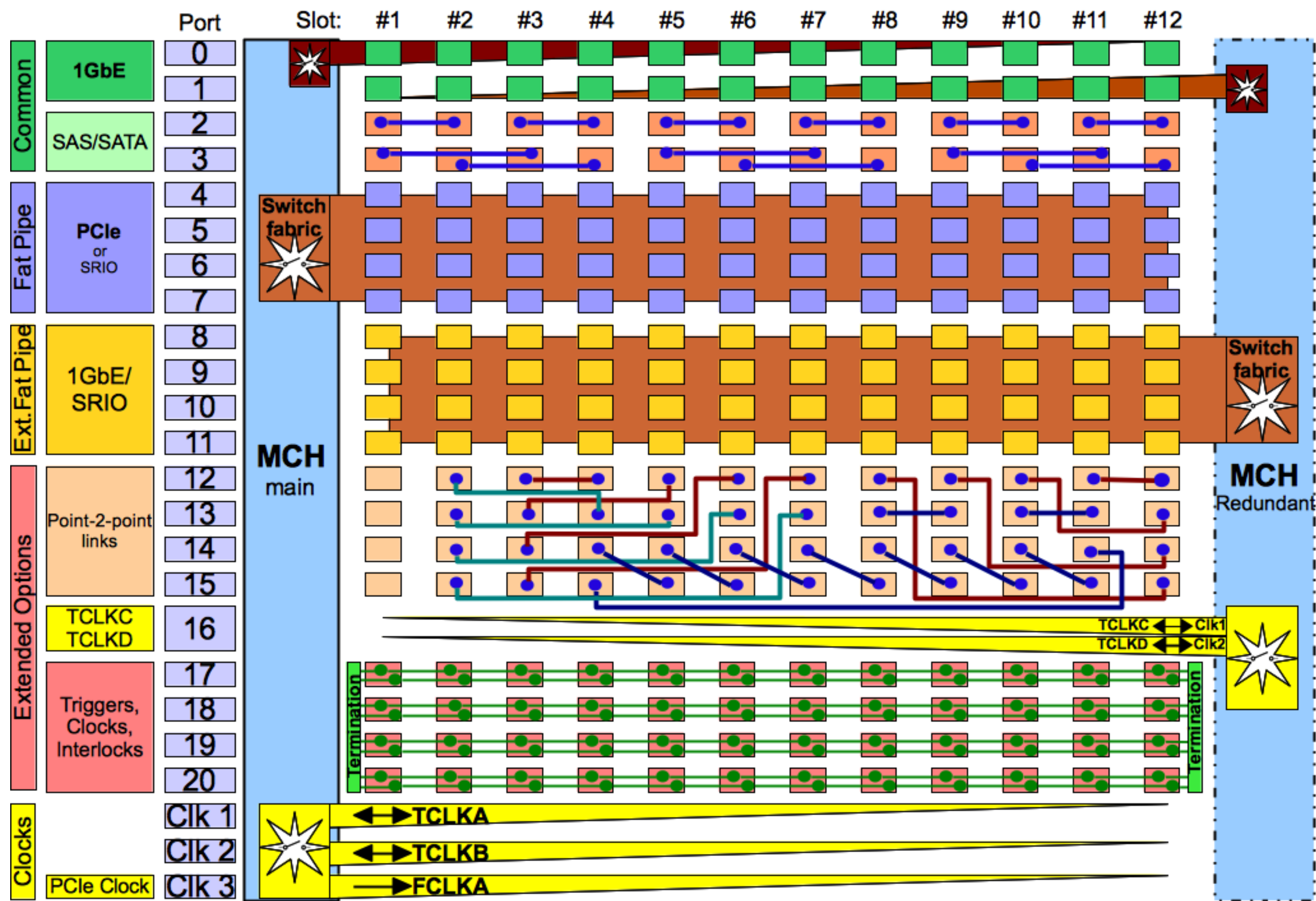
MicroTCA Generations: MTCA.0 MTCA.4 **MTCA.4.1**



MicroTCA.4: A Modular Crate System



MicroTCA.4 Backplane: High Speed Differential Links



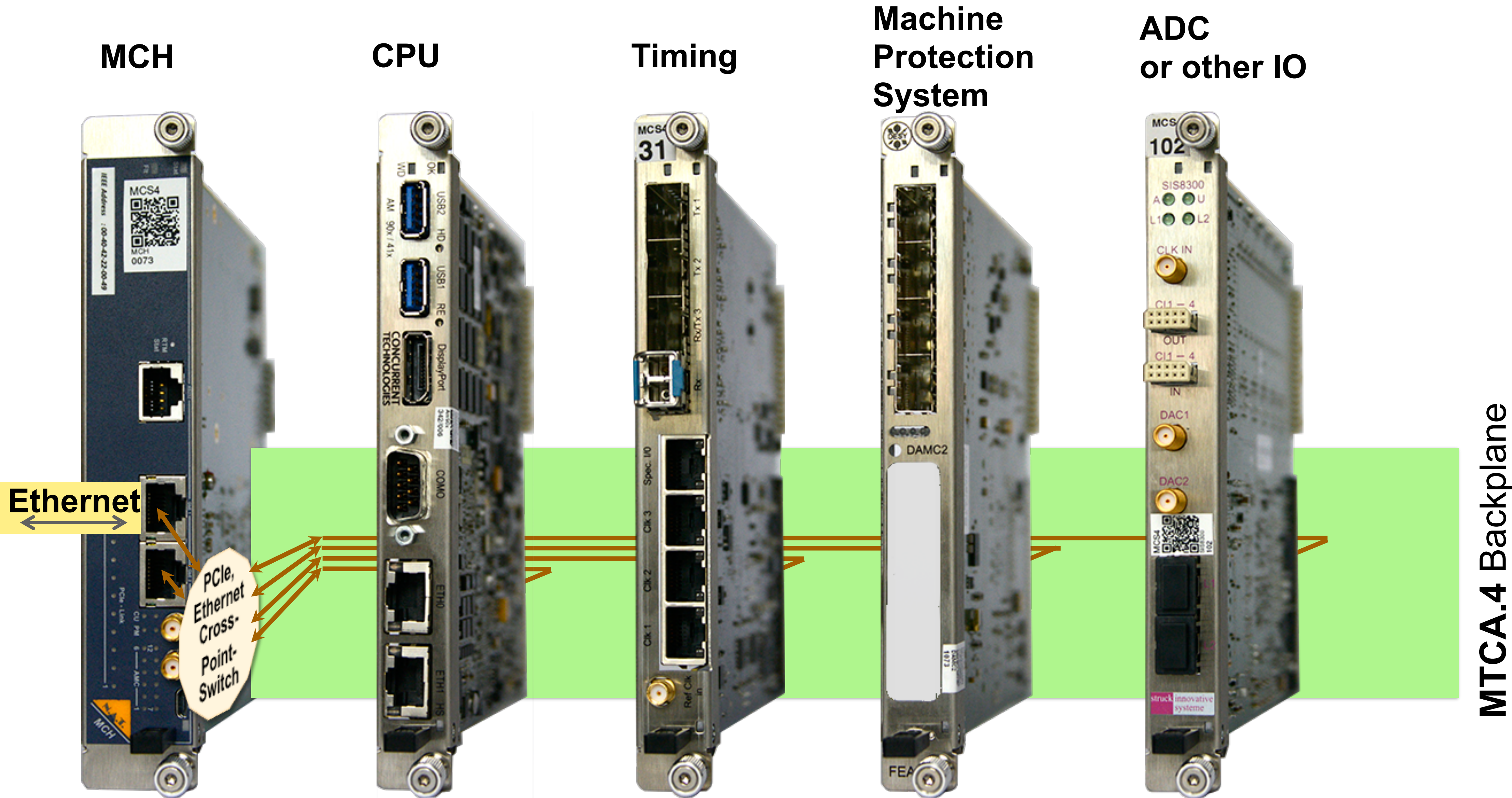
New in MTCA.4 :

Point-to-Point Links

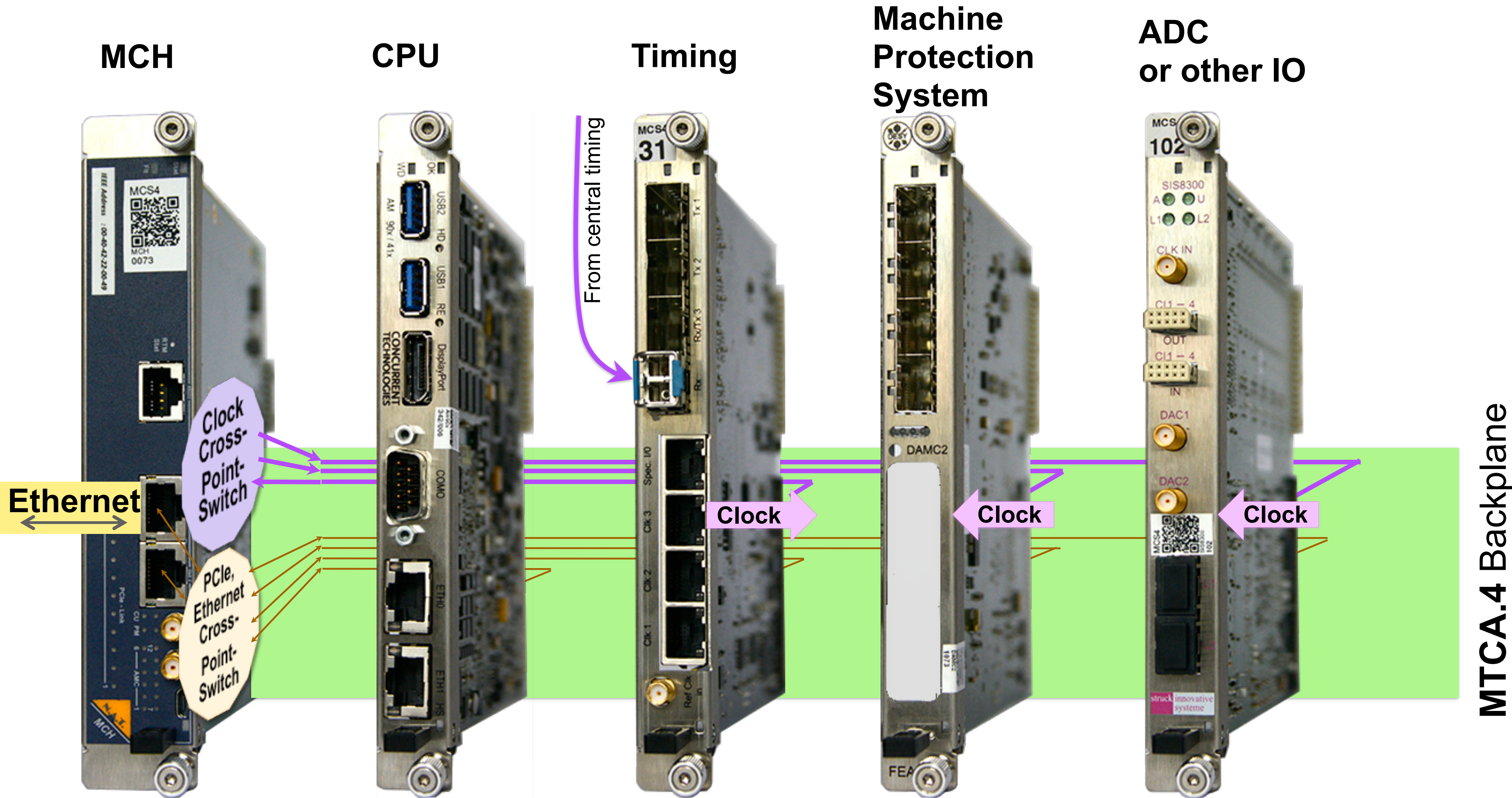
MLVDS
Multi-Point Bus

Bi-Directional
Clocks

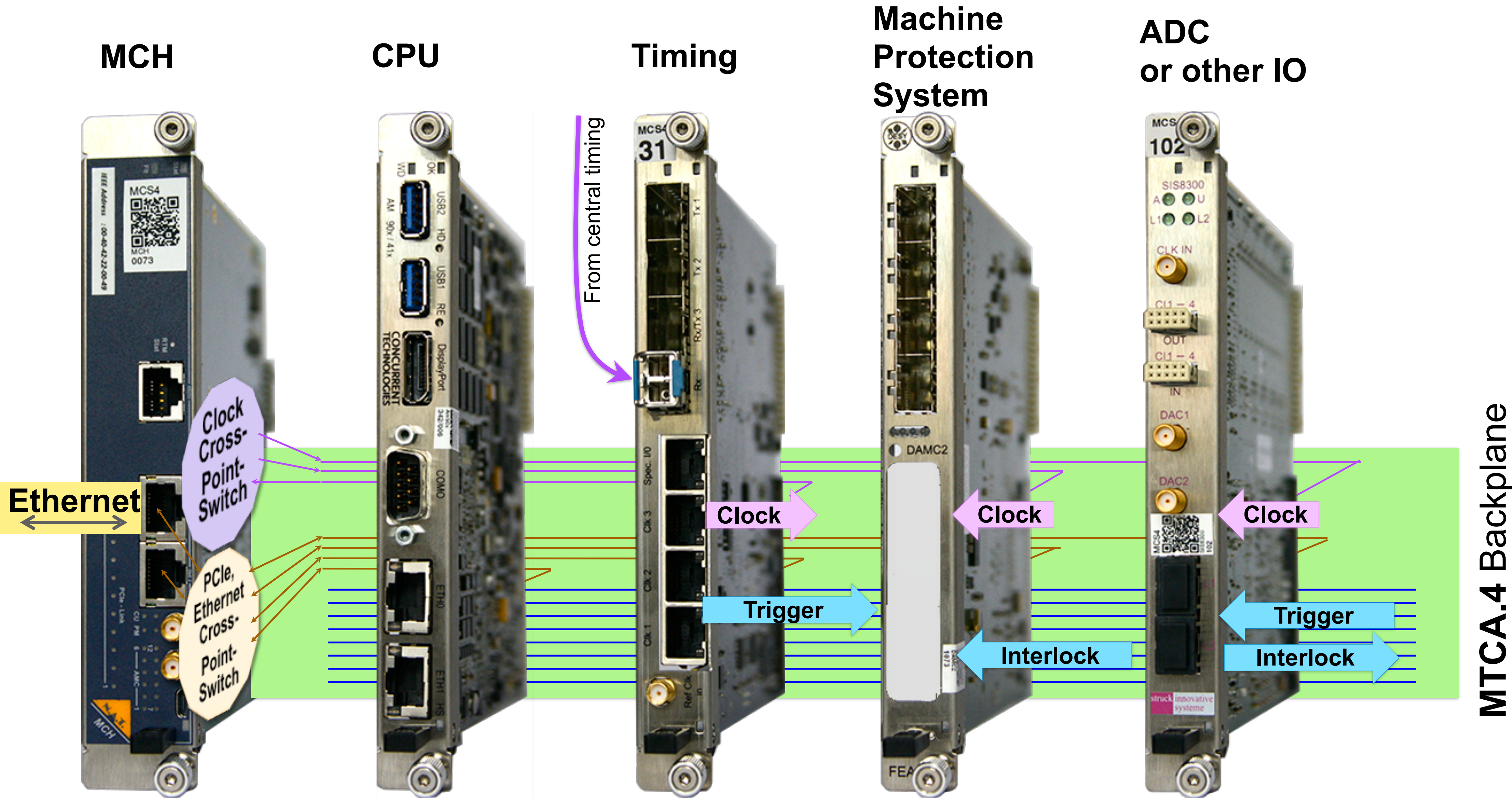
Ethernet, PCIe, Clock as Star; Trigger, Interlocks as Bus



Ethernet, PCIe, Clock as Star; Trigger, Interlocks as Bus

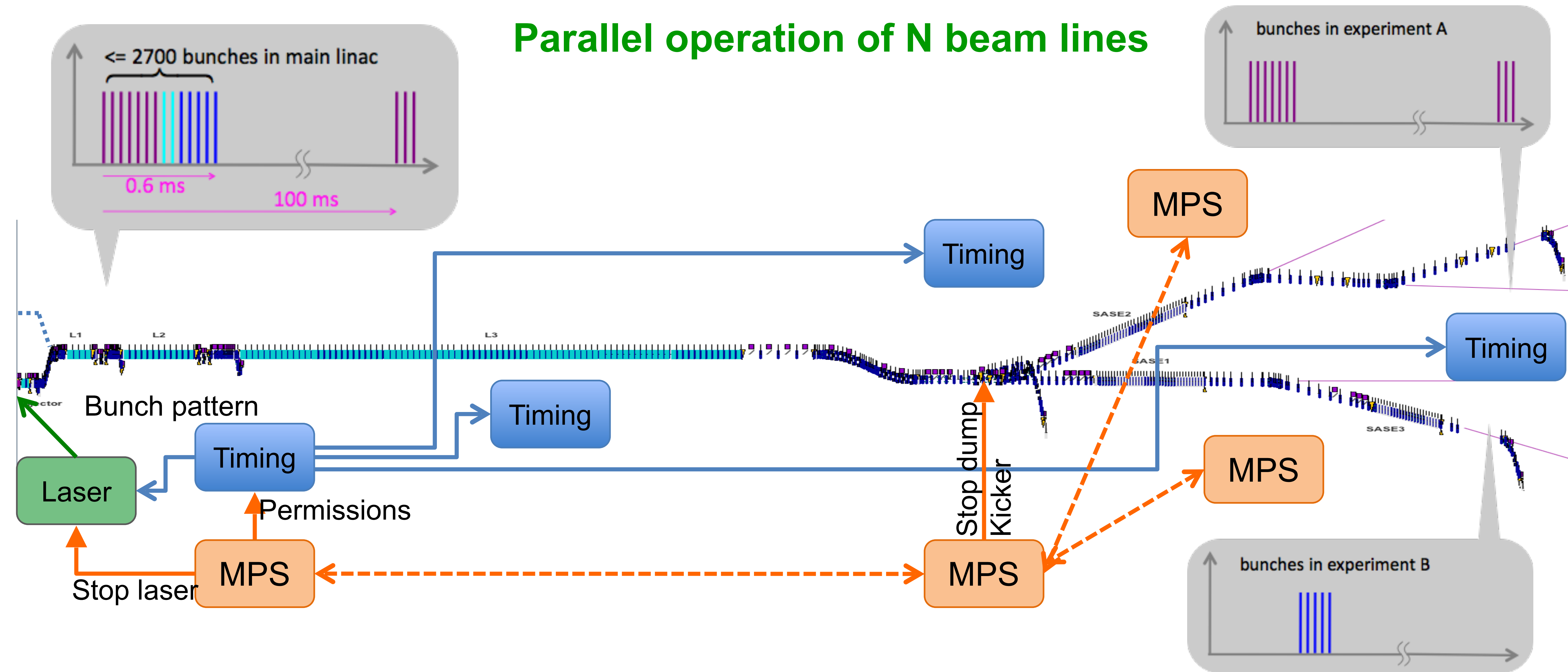


Ethernet, PCIe, Clock as Star; Trigger, Interlocks as Bus



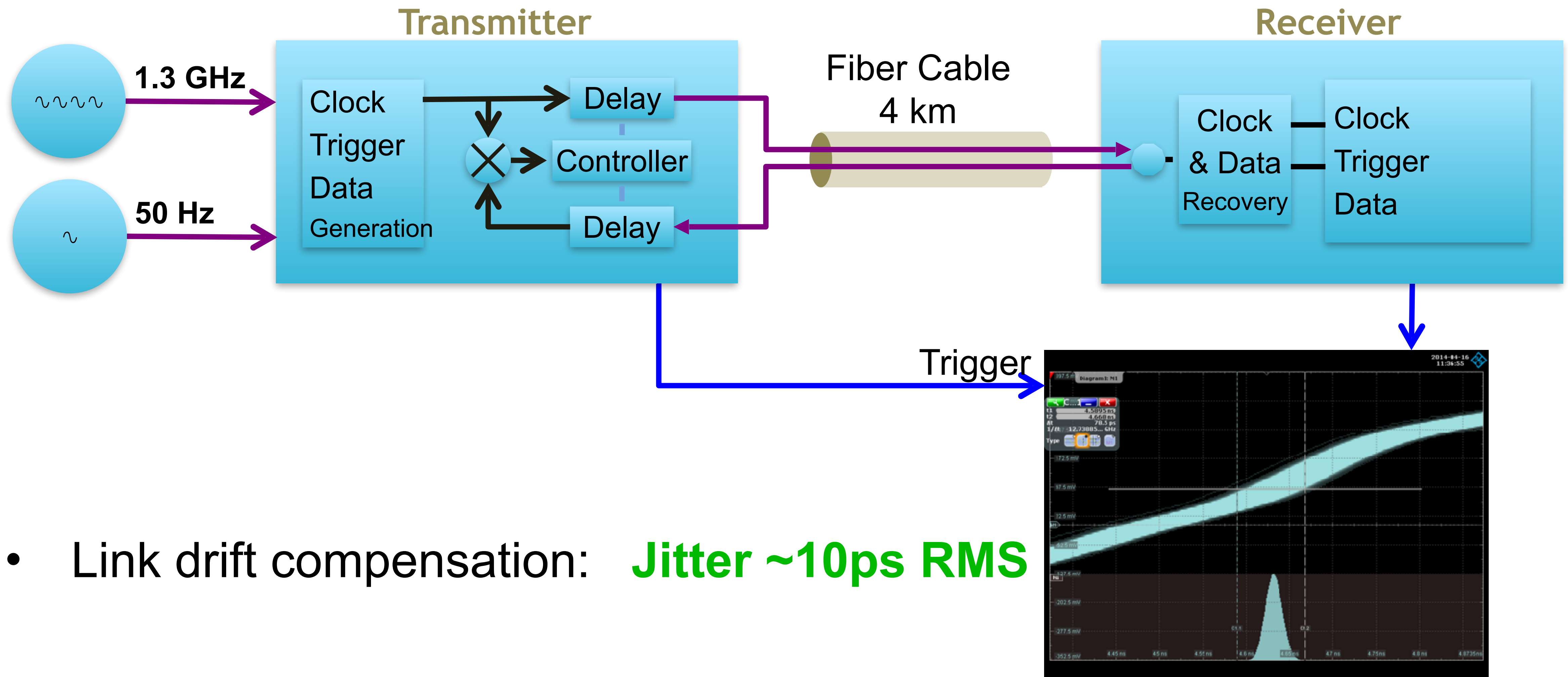
Timing Synchronises, MPS Permits

Parallel operation of N beam lines



The Timing System

- Distributes:
 - Triggers, gates, clocks (10ns ... 5ps resolution)
 - Bunch information (charge, destination,...), unique ID



- Link drift compensation: **Jitter ~10ps RMS**

MicroTCA.4 Timing Receiver / Transmitter

Can be used as a **timing receiver** or **transmitter**

Transmitter Piggyback with link delay

Optional **RTM**:
9 transmitters,
Further triggers or clocks

MicroTCA **backplane:**
TCLKA and TCLKB,
8 * M-LVDS

IN OUT OUT OUT
Fiber optics

3 * Trigger out
1 * Clock out

3 * Trigger out
1 * Clock out

3 * Trigger out
1 * Clock out

4 * General I/O

RTM Timing Extension Modules

9 Lemo outputs (50 Ohm):

- Triggers, Clocks, Data
- 3 channels with 5ps resolution



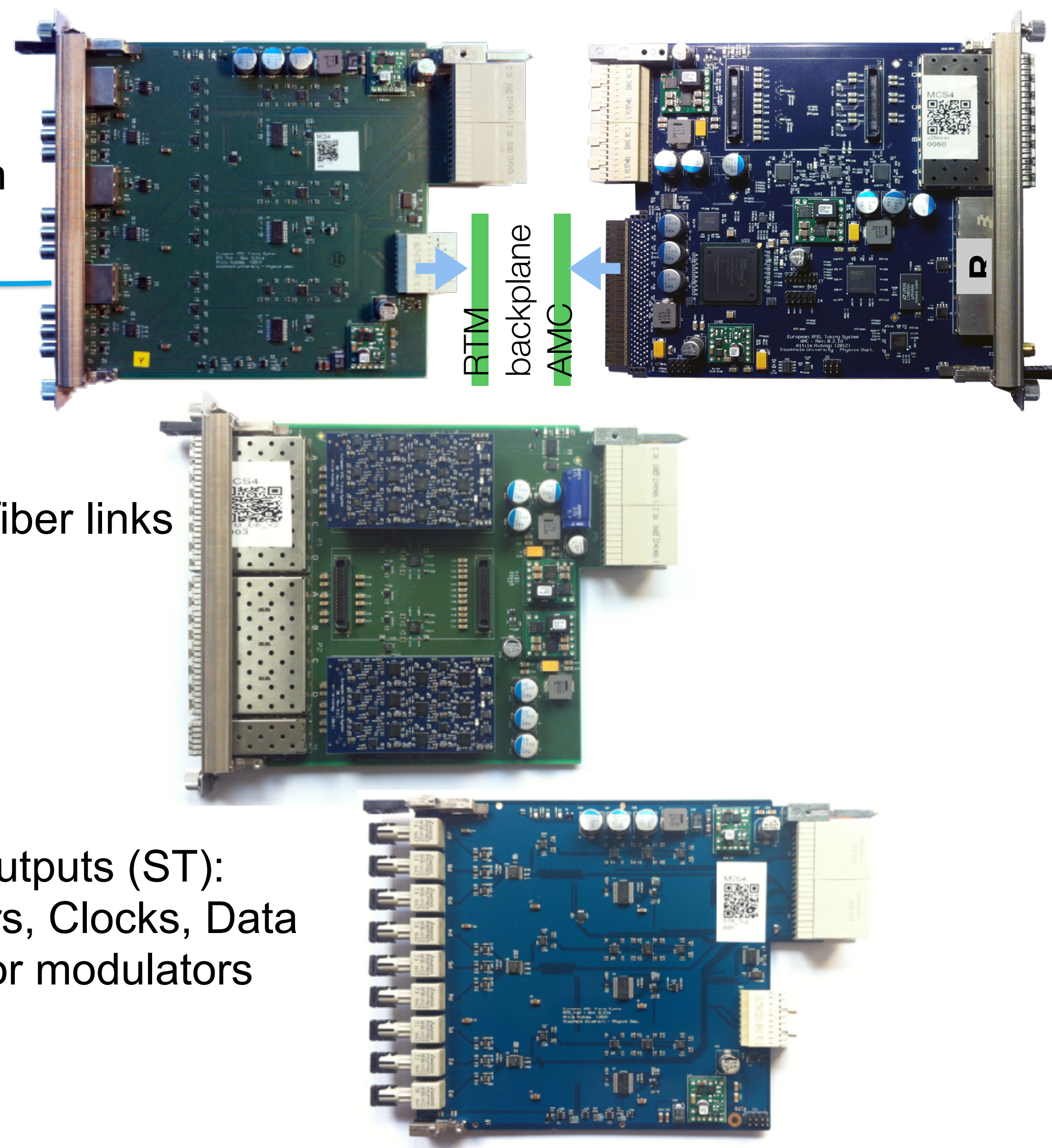
> 100 m

9 SFP outputs:

- length compensated fiber links

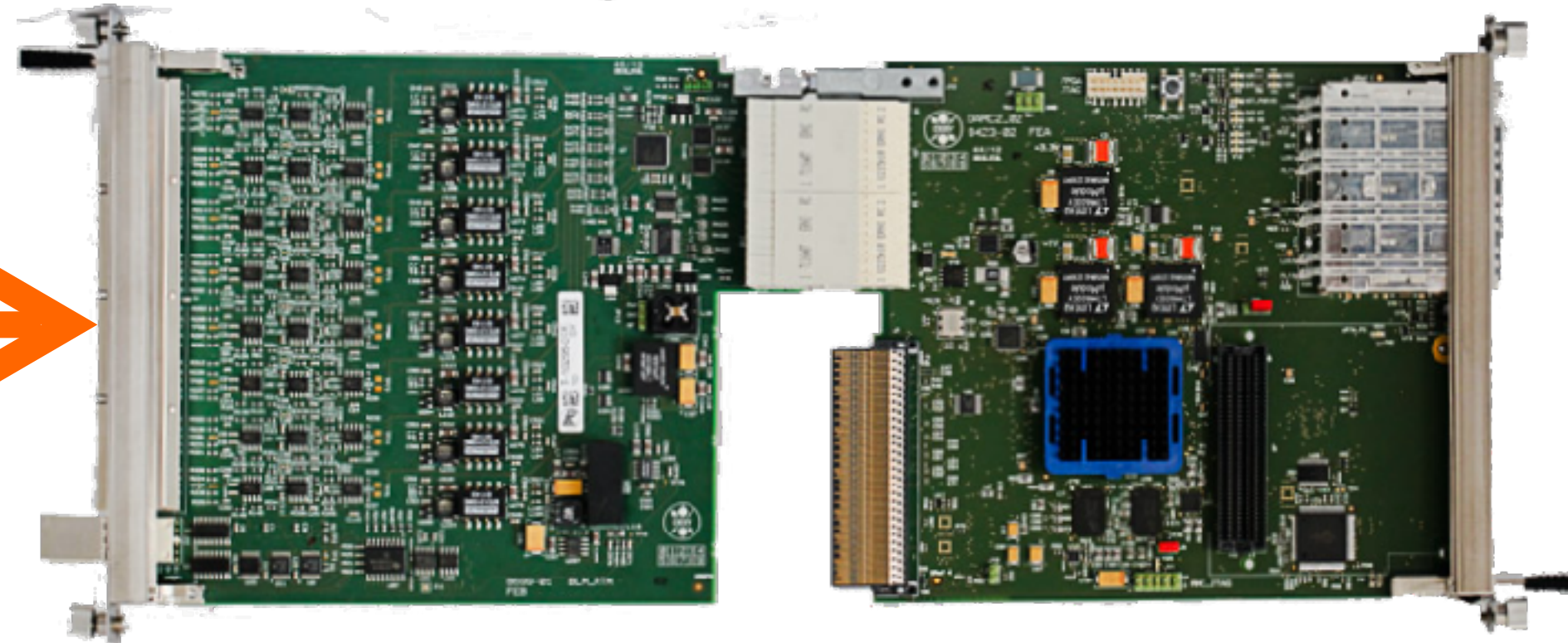
9 Fiber outputs (ST):

- Triggers, Clocks, Data
- used for modulators



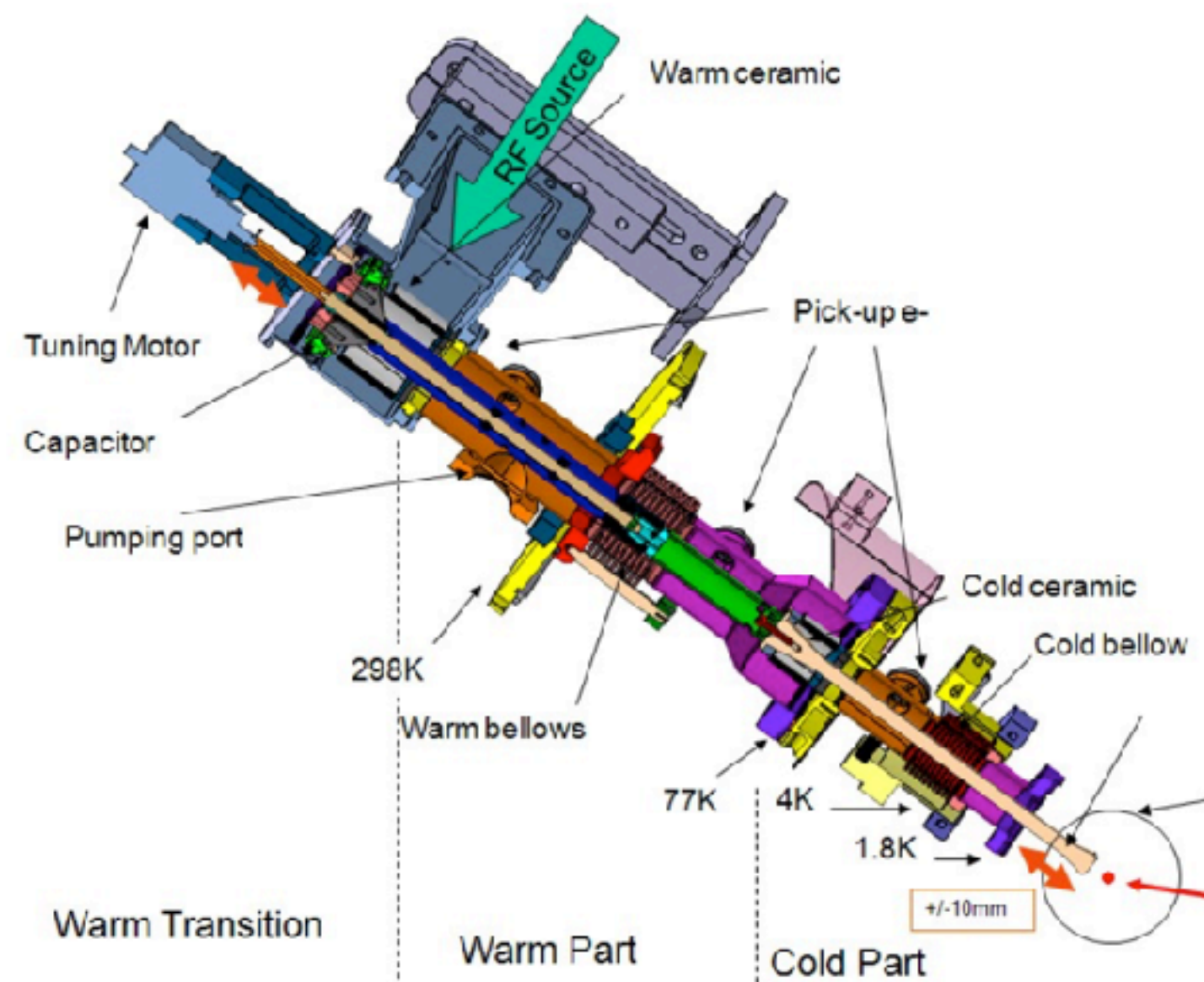
Beam-Loss and Coupler Interlock

~350 Multipliers

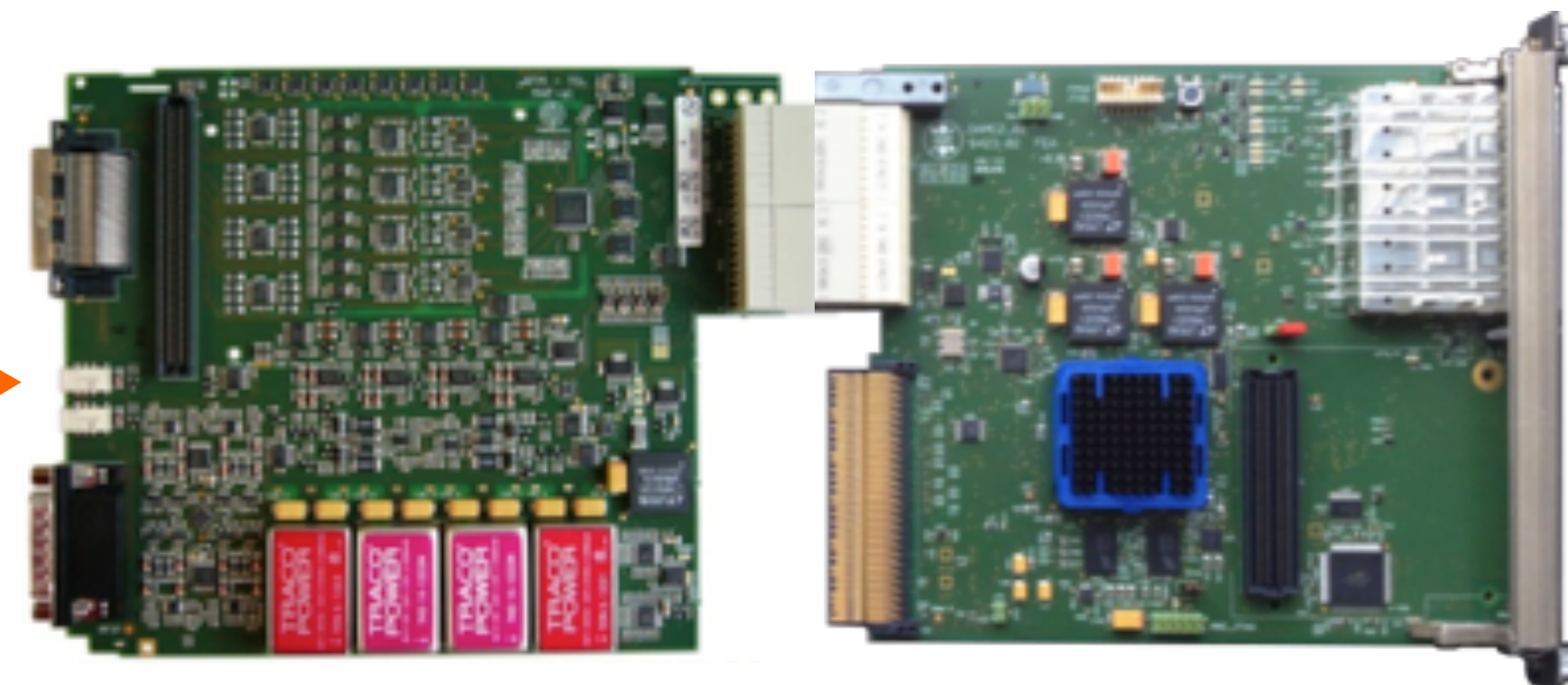


Beam Loss Monitors:

- PhotoMultiplier readout RTM
- DAMC2 with interlock logic



784 Power Couplers



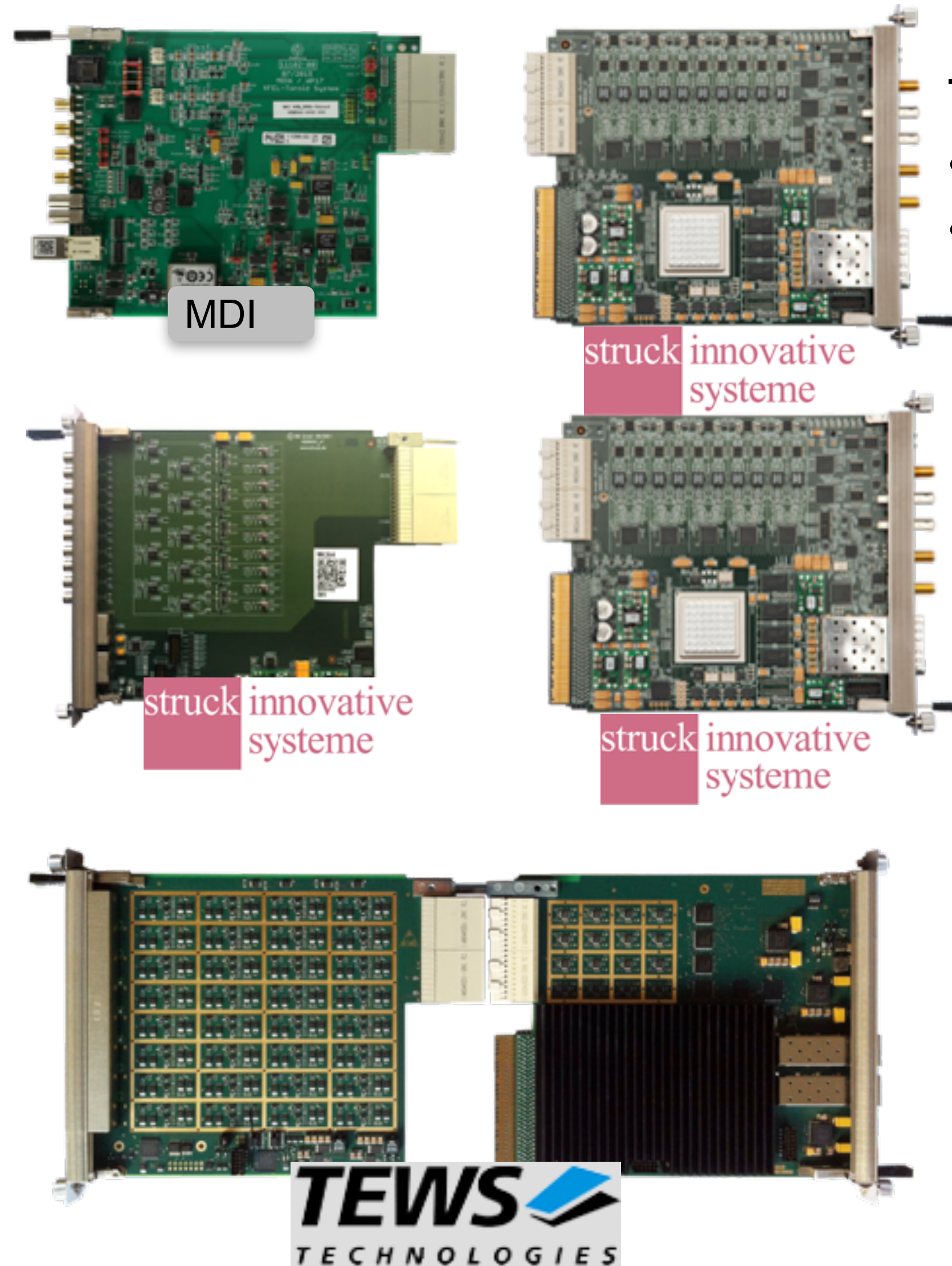
Coupler Interlocks:

- Analog readout RTM
- DAMC2 with interlock logic

Diagnostics: Based on Modular MicroTCA

Photon Gas Monitor Detector:

- ADC @ ≤ 7 GSPS



Toroid Protection:

- Analog readout RTM
- SIS8300 ADC @ 108 MSPS

Kicker, FC, etc. readout:

- Amplifier RTM
- SIS8300 ADC @ 108 MSPS

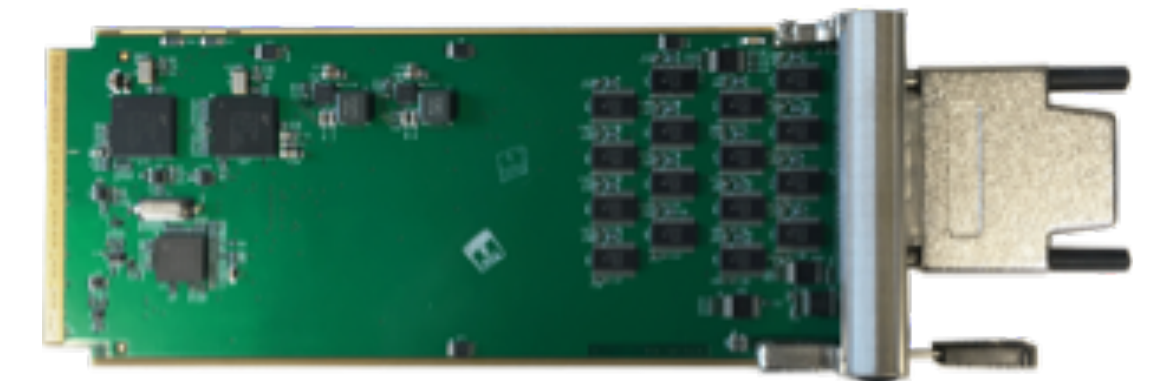
128 channel Spectrometer:

- Shaper/Amplifier RTM
- 32 ch. ADC @ 54 MSPS

Magnets, Vacuum, Cameras, slow IO, ...



Kontron: 4* Ethernet IO



Tews: 16 * RS-232 IO



Concurrent
CPU: i7 Quad-Core
PCIe Gen3
Redundant SSD
Remote console

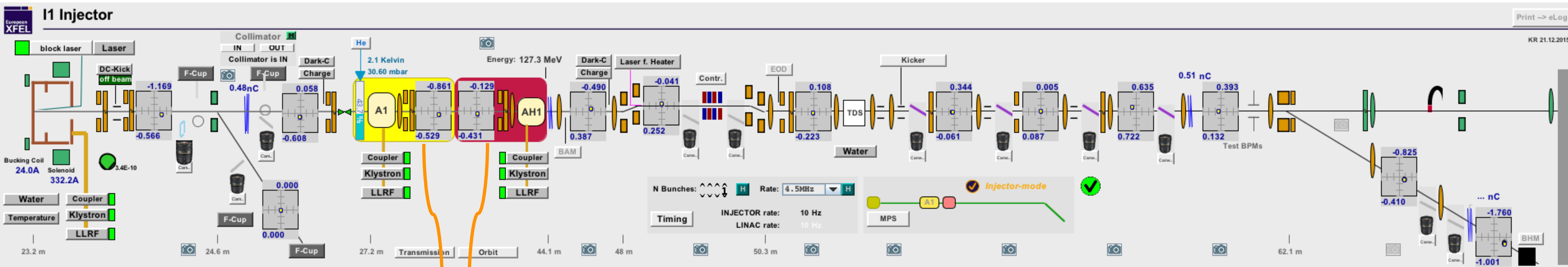


ESD: 4* CAN IO



ESD: Digi/analog IO

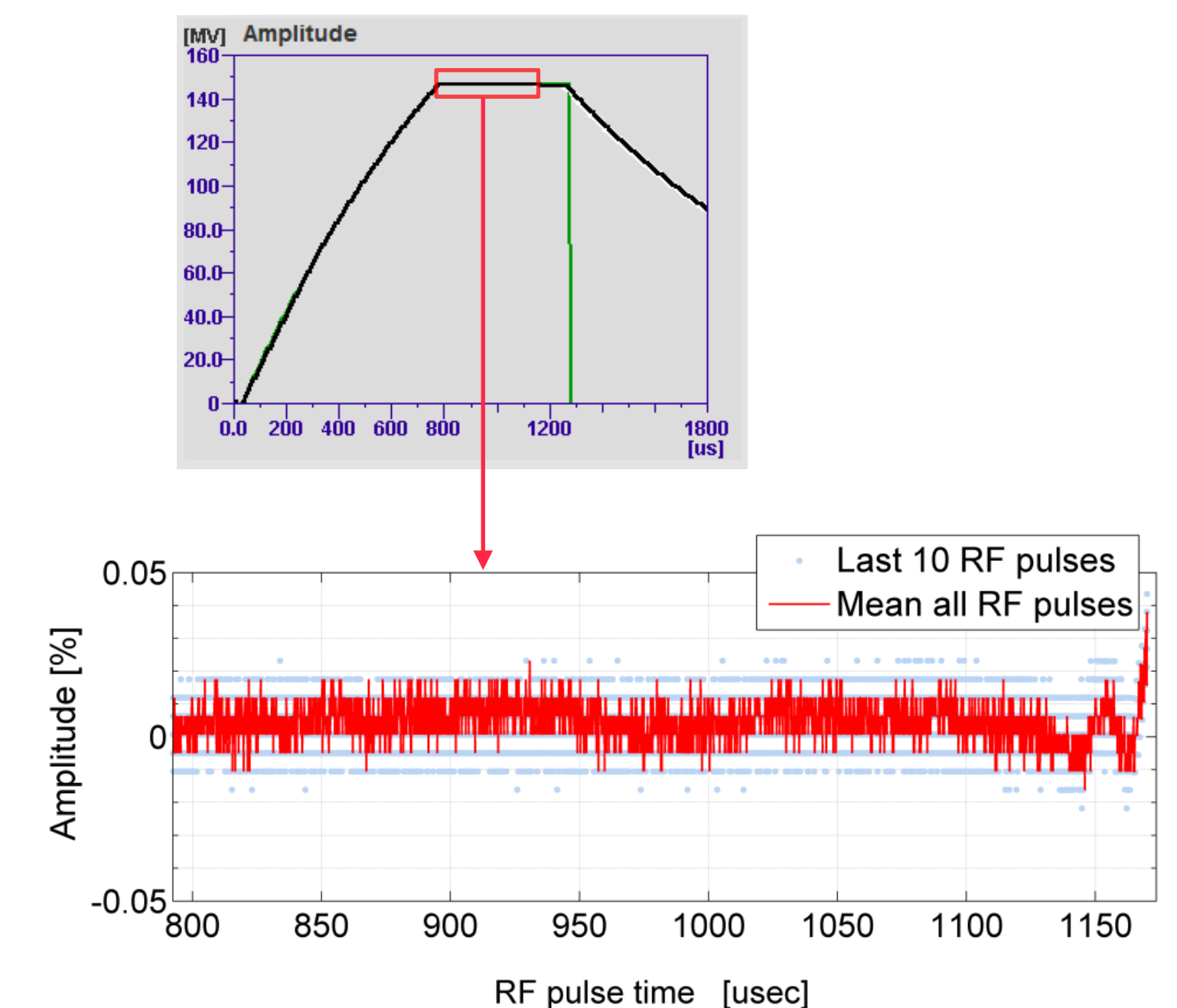
XFEL Injector: Controls Rack for 1.3 and 3.9 GHz



Rear

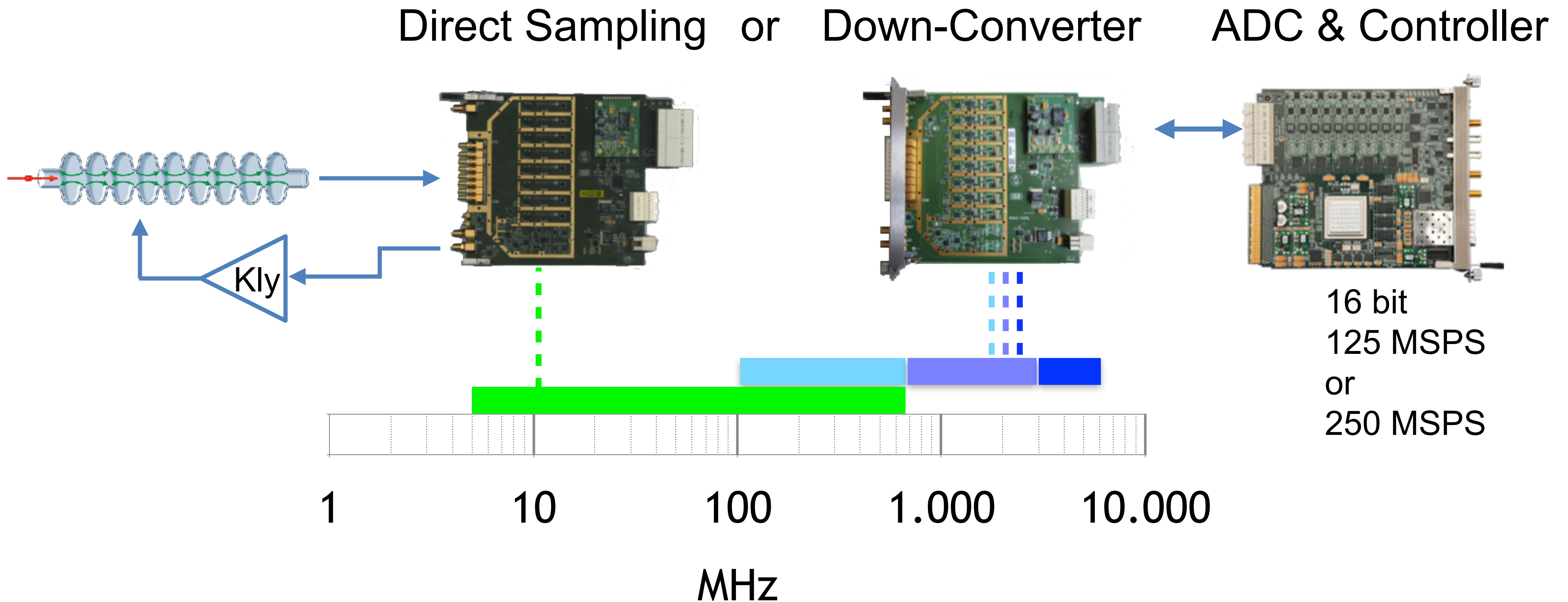


Front



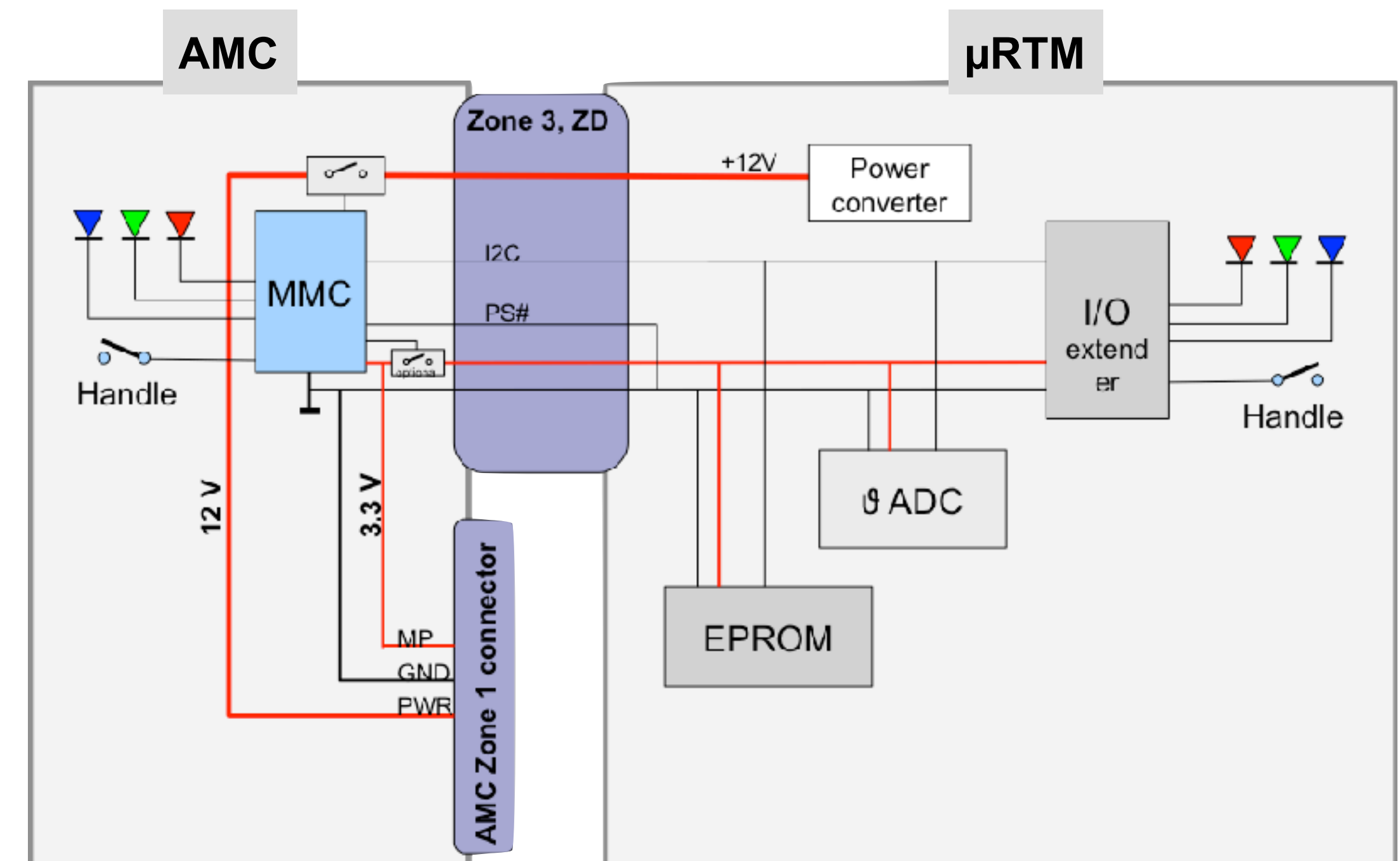
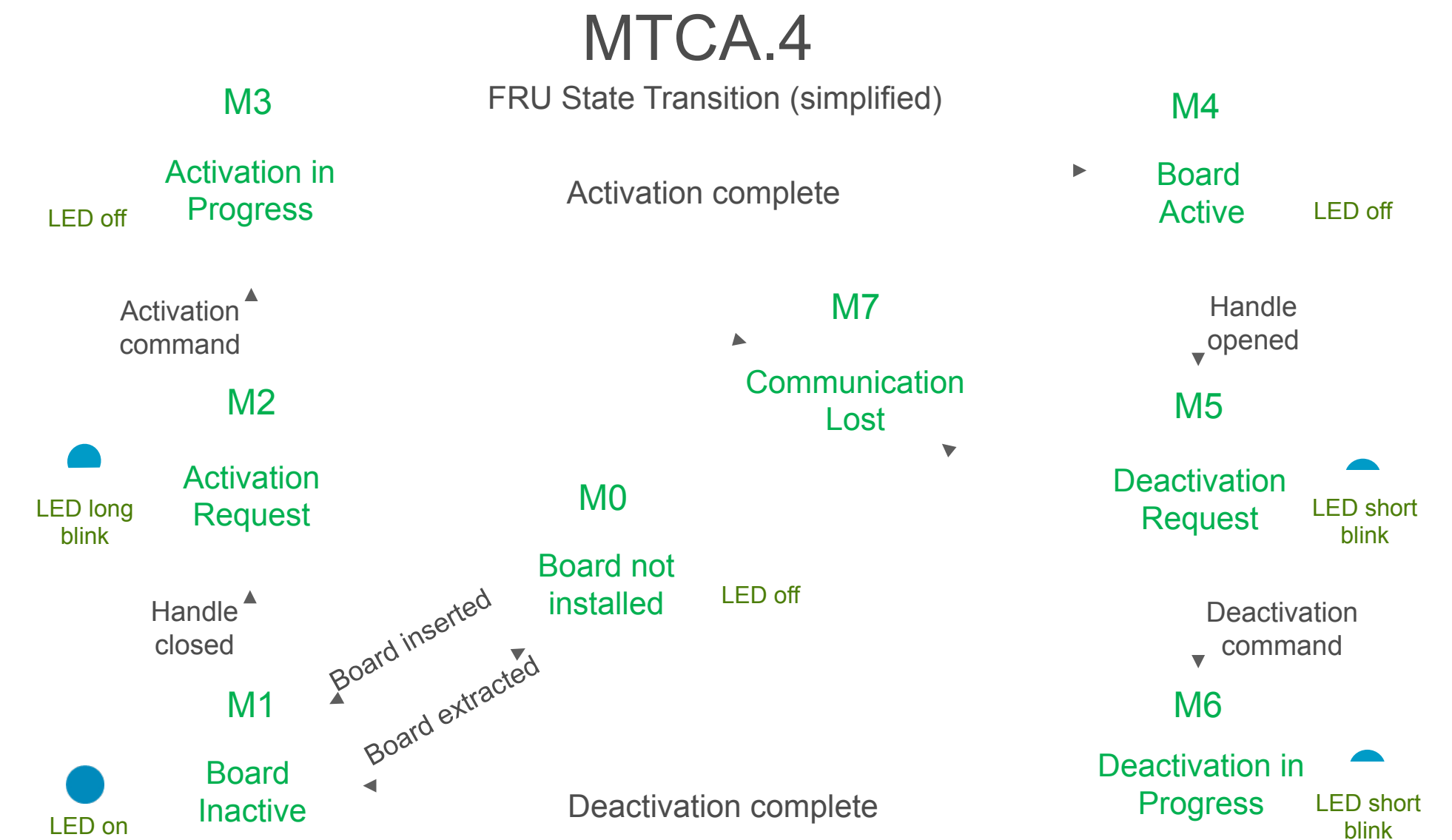
$$\sigma(dA/A) = 0.0057 \%$$

A Modular LLRF System: for a Wide Application Range

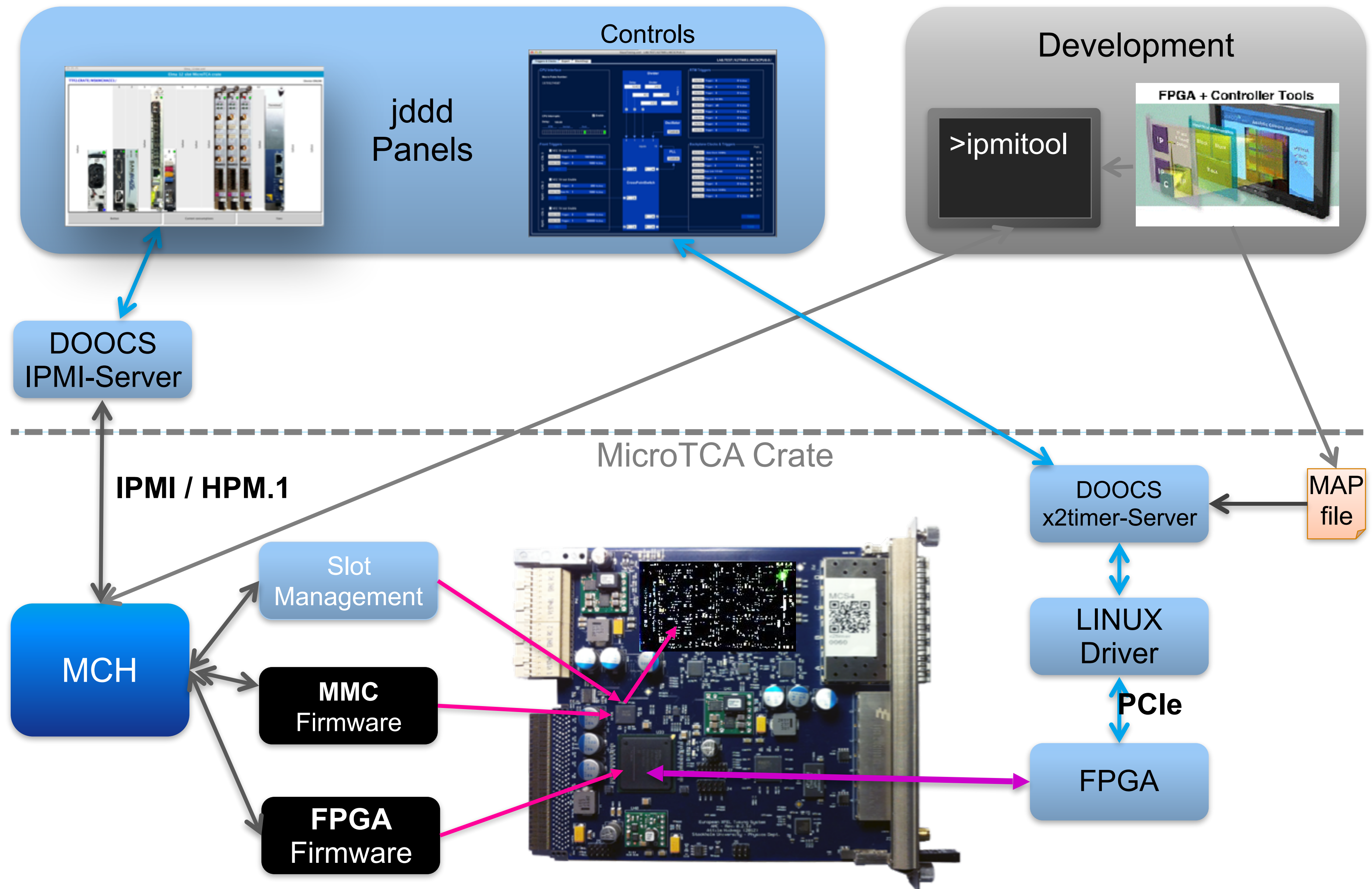


MicroTCA Management

- Power management
- Temperature and fan control
- Verifikation of compatibility (keying)
- Hot-swap (incl. DOOCS server)
- Remote power-cycling
- Remote firmware upgrades
- PCIe, Ethernet, Clock configuration
- Status and error information
- MTCA.4.1: Classes for RTM



Integration of Controls, Management and Development



Remote Management: Racks, Crates, Modules

XTIN UG2-5

XTIN UG7

L1 - CS1/B1

L2 - CS2

L3 - CS3/B2

L3 - CS3/B2

XHM

XFELcpuXHM1

x2timer

x2timer.4

x2timer.1

x2timer.5

x2timer.2

x2timer.6

x2timer.3

OK

WD

Crate

uTCA Mon

UG3

XFELcpuKLY39

ADC 0

x2timer

OK

WD

Crate

uTCA Mon

XFELcpuLLGUN1KLM

x2timer

OK

WD

Crate

UG4

XFELcpuDIHOM1

x2timer

OK

WD

Crate

uTCA Mon

XFELcpuLGUN1

x2timer

OK

WD

Crate

UG5

XFELcpuTIME1

TimerMain

x2timer

x2timer.s3

x2timer.s4

x2timer.s5

x2timer.s6

x2timer.s7

x2timer.s8

x2timer.s9

x2timer.s10

OK

WD

Crate

Rack

LHX

uTCA Mon

MPS

XFELcpuMPS1

MPS.0

MPS.1

MPS.2

MPS.3

MPS.4

MPS.5

MPS.6

MPS.7

MPS.8

MPS.9

OK

WD

Crate

XFEL MicroTCA Crates

Number of entries: 183

XFELMCHDI131L1 :	show	Schroff GmbH	12	●
XFELMCHLASER2 :	show	Schroff GmbH	12	●
XFELMCHLLA6M :	show	Schroff GmbH	12	●
XFELMCHILA2M :	show	Schroff GmbH	12	●
XFELMCHILA2S :	show	Schroff GmbH	12	●
XFELMCHDI533L3 :	show	Schroff GmbH	12	●
XFELMCHDI2262S1 :	show	Schroff GmbH	12	●
XFELMCHDI55I1 :	show	Schroff GmbH	12	●
XFELMCHDI94I1 :	show	Schroff GmbH	12	●
XFELMCHDI2360S1 :	show	Schroff GmbH	12	●
XFELMCHLLA7M :	show	Schroff GmbH	12	●
XFELMCHLLA7S :	show	Schroff GmbH	12	●
XFELMCHLLA8M :	show	Schroff GmbH	12	●
XFELMCHLLA8S :	show	Schroff GmbH	12	●

AMTF MicroTCA Crates

Number of entries: 8

MSKMCHAMTF1 :	show	Schroff GmbH	12	●
MSKMCHAMTF2 :	show	ELMA Electronic GmbH	12	●
MSKMCHAMTF3 :	show	Schroff GmbH	12	●
AMTFMTS3MCH :	show	ELMA Electronic GmbH	12	●
AMTFMTS2MCH :	off			
AMTFMTS1MCH :	show	ELMA Electronic GmbH	12	●
MSKMCHAMTF39 :	show	Schroff GmbH	12	●
AMTFMTS39-MCH :	off			

Modules in selected crate: XFEL.CRATE/XFELMCHDI55I1/

Crate

Fans

Power Modules

show graphical

			Serial:	MMC version
CRATE :	Schroff GmbH	IPMB:0x20 Sensor N:87 Type:FRU Hot Swap Event:Transition to M6	info	0000000000000001
RTM11 :	XFEL_Toroid...	Deutsches Elektronen-Synchrotron	info	23
RTM10 :	XFEL_Toroid...	Deutsches Elektronen-Synchrotron	info	29
RTM12 :	XFEL-BLM	Deutsches Elektronen-Synchrotron	info	869902021
RTM8 :	MPS-RTM1	ATP	info	01-047
RTM5 :	XFEL-BLM	Deutsches Elektronen-Synchrotron	info	869902053
RTM4 :	XFEL-BLM	Deutsches Elektronen-Synchrotron	info	869902049
RTM3 :	MPS-RTM1	ATP	info	01-048
RTM2 :	RTM_DB_X2	Stokholm University	info	0001
AMC9 :	AM4301	Kontron	info	9012045838
COOL_UNIT1 :	Fan speed=	0 0 0 0	info	1071502894AC
COOL_UNIT2 :	Fan speed=	3840 3780 3840 1920	info	1071502914AC
AMC2 :	X2TIMER	Stockholm University	info	0028
AMC4 :	DAMC2	Deutsches Elektronen-Synchrotron	info	4123
AMC11 :	SIS8300L2	Struck Innovative Systeme GmbH	info	125

Control functions:

Cold Reset

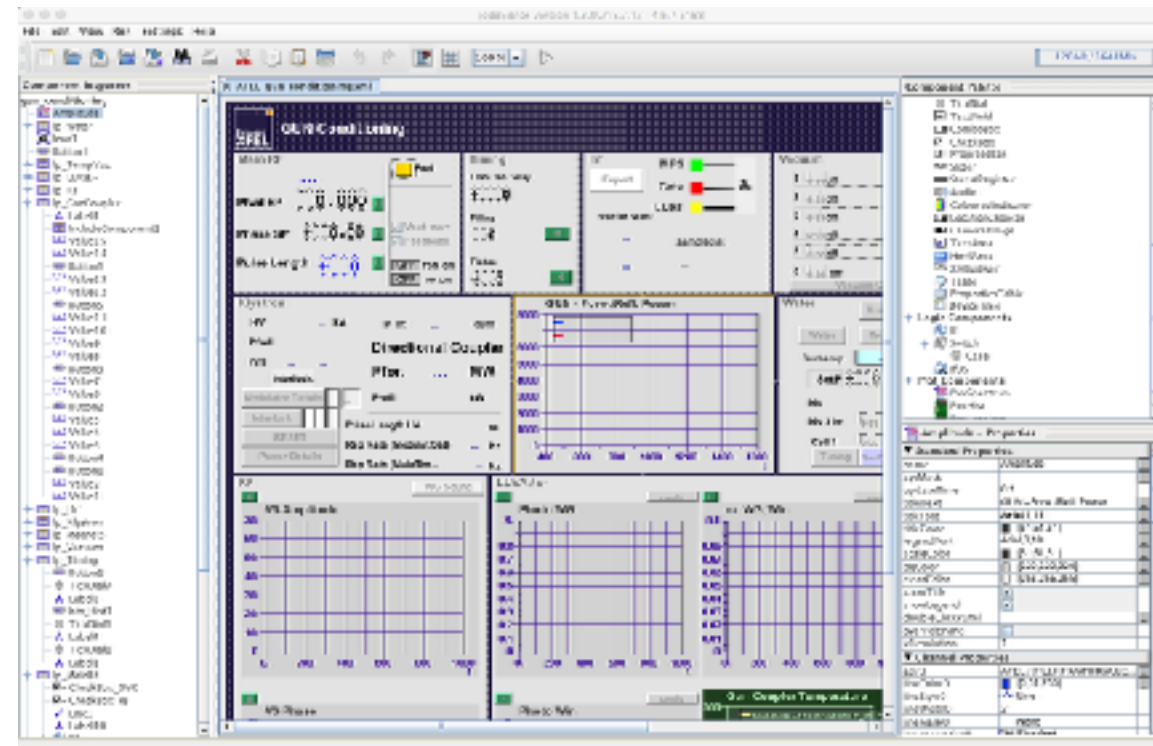
Reboot

8. Oct. 2017 MicroTCA Workshop @ ICALEPCS

Ka

30

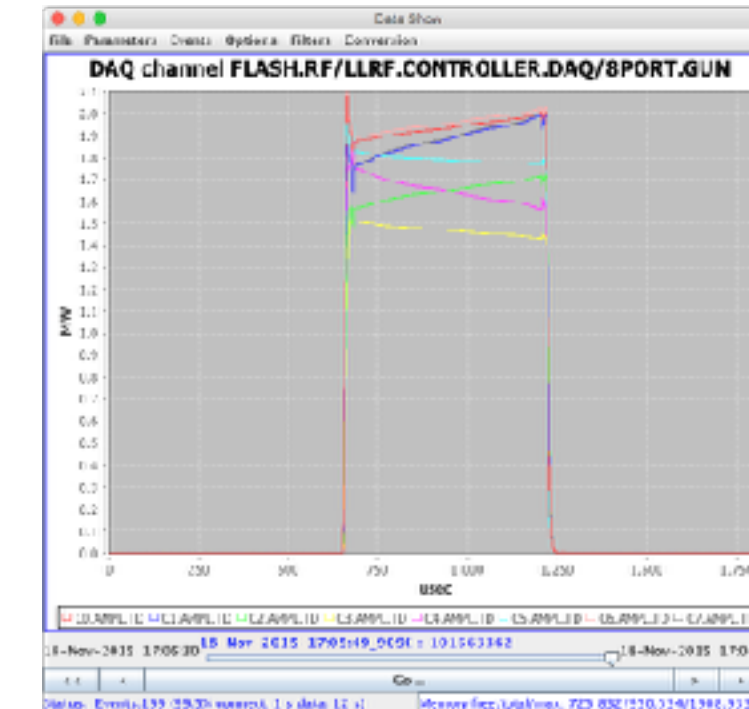
Panel Editor



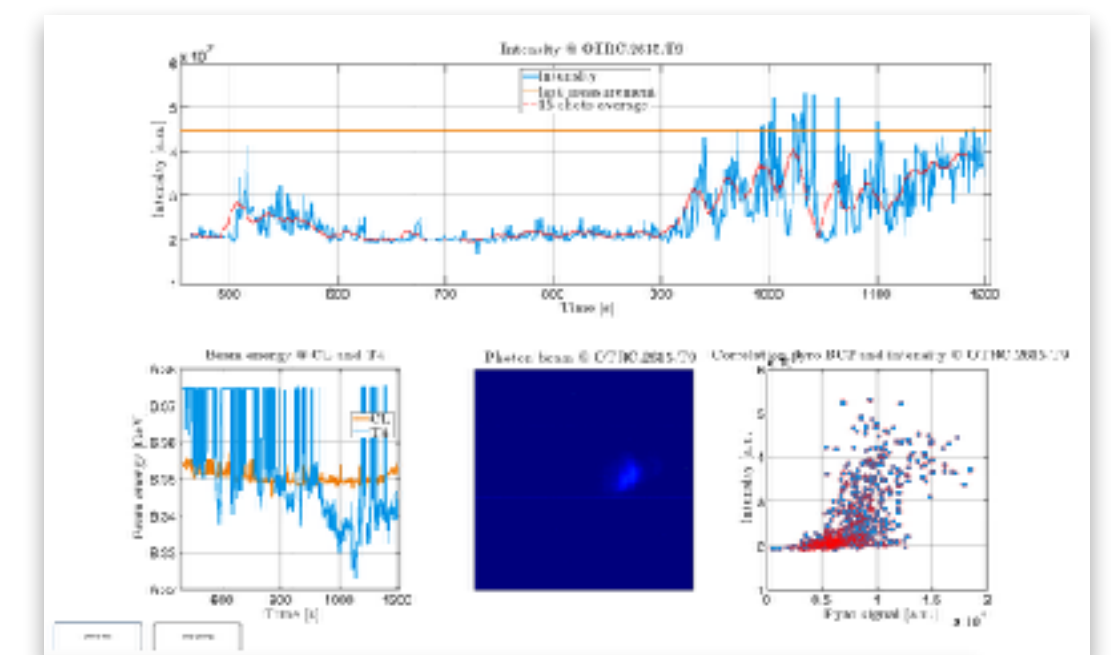
Address Browser



DAQ Data Browser

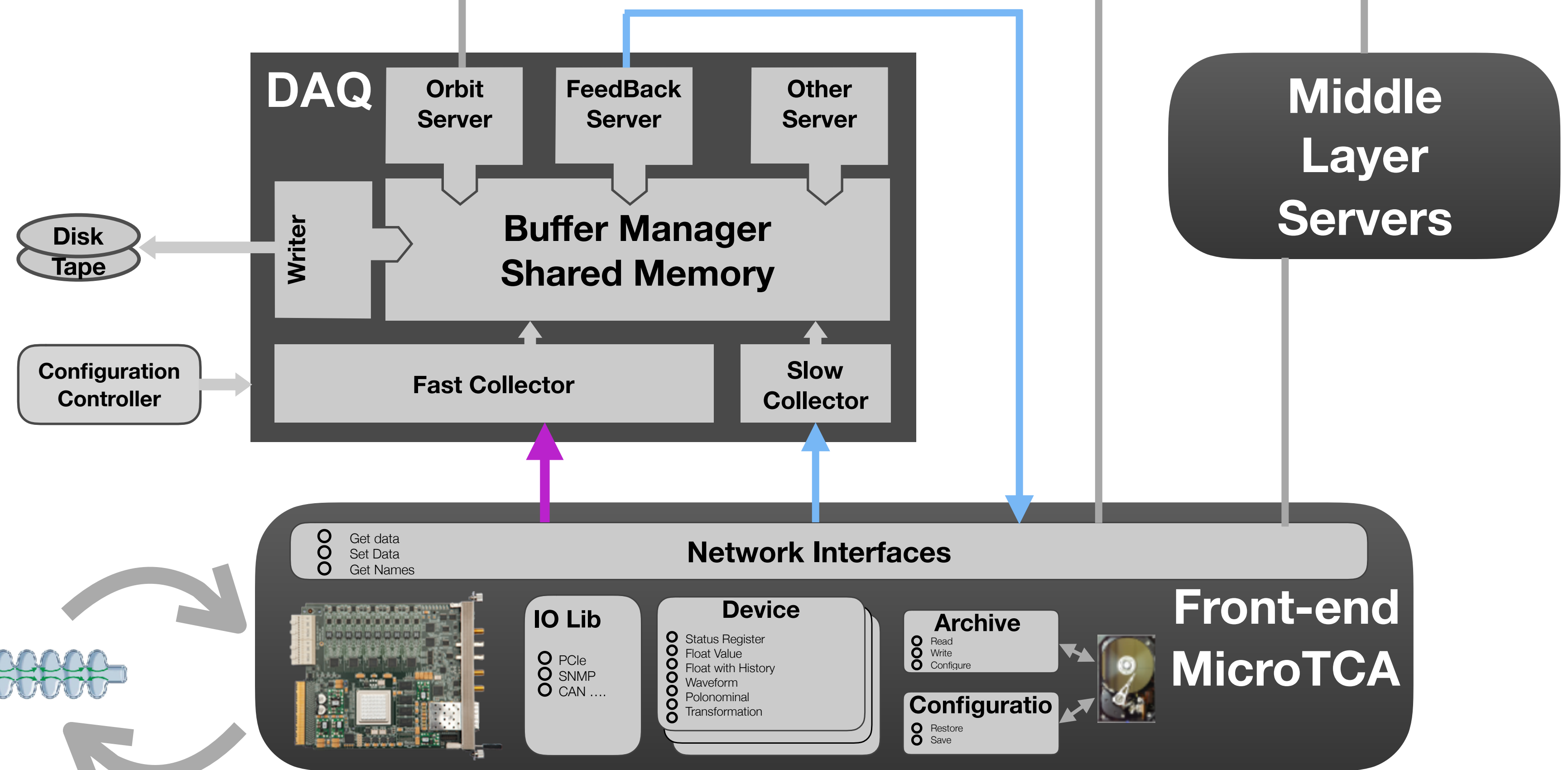
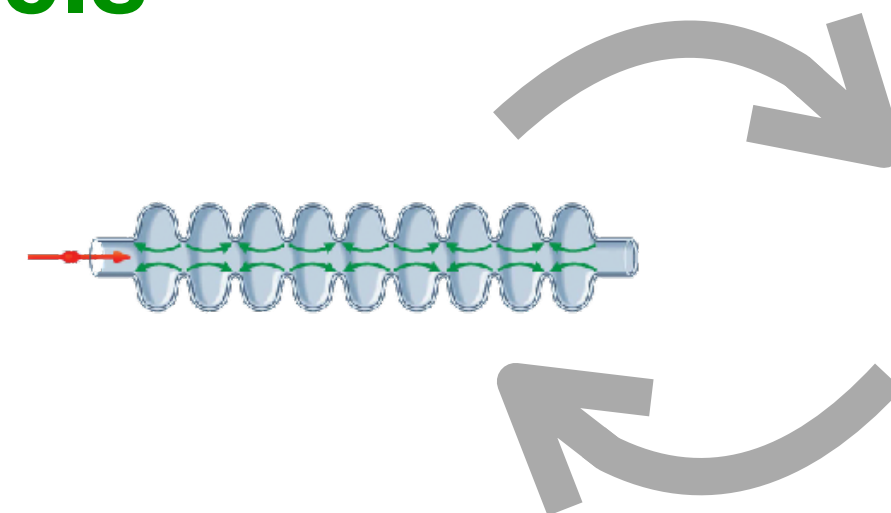


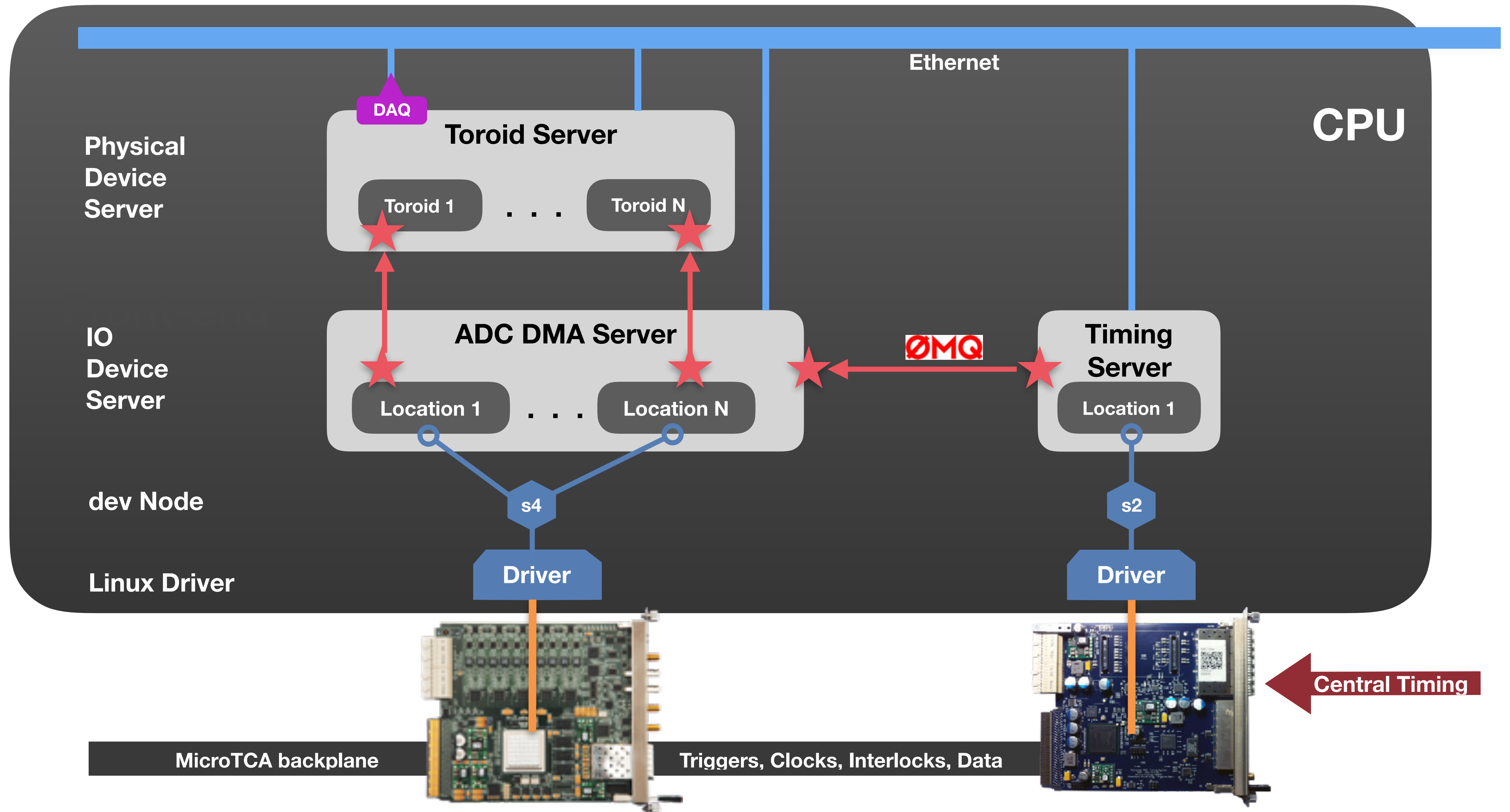
MATLAB & Special Apps



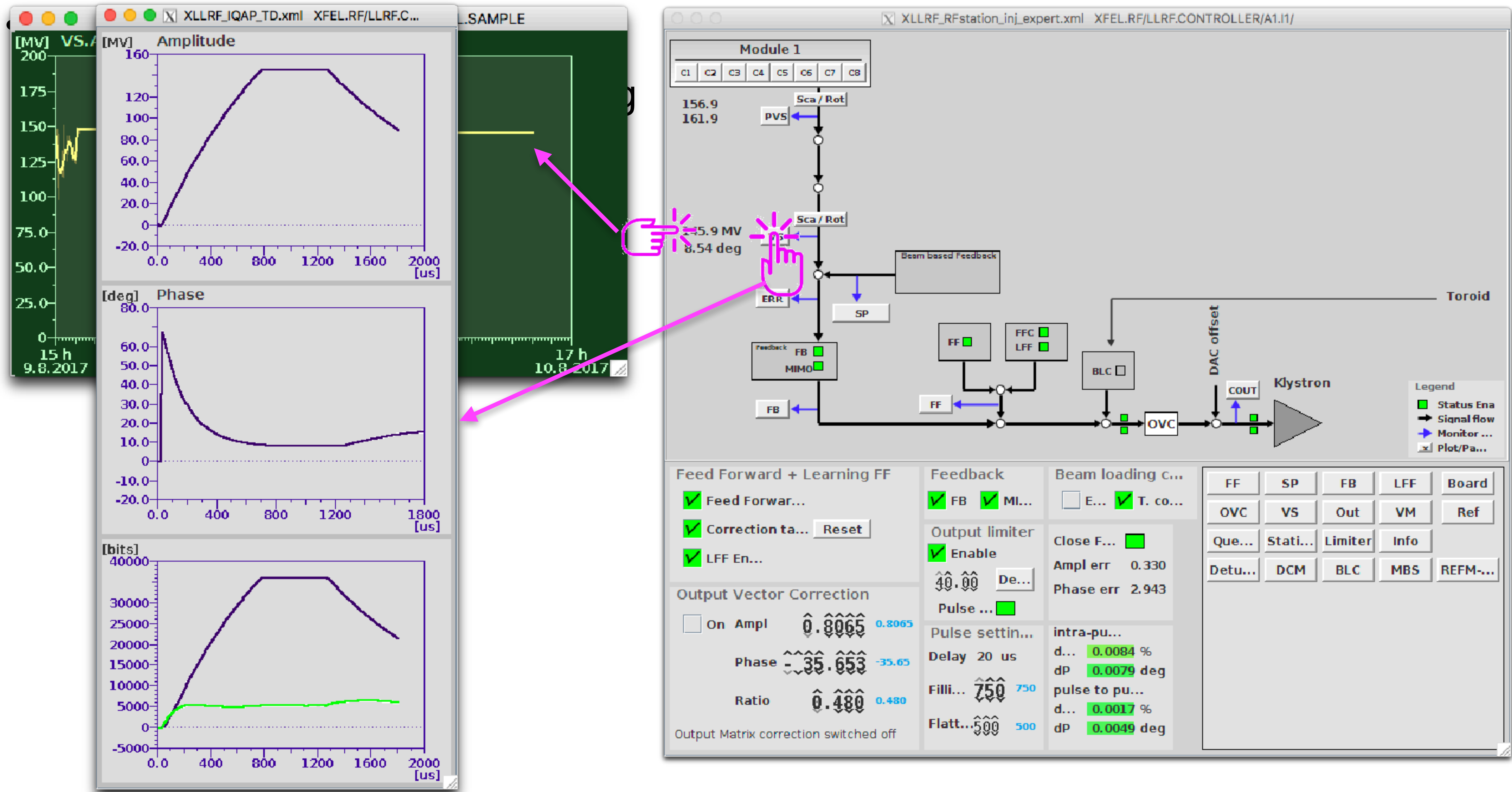
DOOCS Architecture

XFEL:
> 600 000 Channels
Archived





LLRF System: Complex Systems Require Lots of Diagnostics



Summary

- **XFEL** is in operation and delivers beam to experiments
 - Very fast startup since HW & SW was debugged in FLASH & XFEL Injector
- ~ **250 MicroTCA** crates are installed and operational
- Parallel operation of ≥ 2 beam lines:
 - Full HW/SW integration in MPS, Timing, Subsystems
- XFEL is controlled by **DOOCS**, has > 8 M properties (addressable items)
 - All fast data is controlled by MicroTCA, including photon experiments
- **MicroTCA provides:**
 - High speed data transfer
 - excellent analog performance
 - Complete local & remote management
 - Redundancy $\rightarrow$ high availability

Thank you!

6th MicroTCA Workshop for Industry and Research 6th - 7th December 2017 DESY, Hamburg



More information: MTCAWS.desy.de TechLab.desy.de DOOCS.desy.de XFEL.desy.de

Implementation of MicroTCA for Beam Diagnostics and Synchronization

MicroTCA.4 is the main electronic platform for data acquisition and processing at FLASH and the European XFEL.



Matthias Felber
LbSync Team
DESY MSK group

ICALEPCS Workshop
User Experience in MicroTCA

Barcelona, Spain
October 8, 2017

Overview

> Introduction: FELs at DESY (FLASH and European XFEL)

> Optical Synchronization System

- Introduction
- MicroTCA Setups
- Firmware & Software

> Diagnostic Systems & MTCA

- Bunch Arrival Time Monitor
- Bunch Compression Monitor
- Electro-Optic Diagnostic
- Beam Position Monitors
- Charge Measurements

▪ Beam Loss and Beam Halo Monitors

Matthias Felber | Implementation of MicroTCA for Beam Diagnostics and Synchronization | 8th October, 2017 | Page 2



FLASH: Free-electron LASer in Hamburg

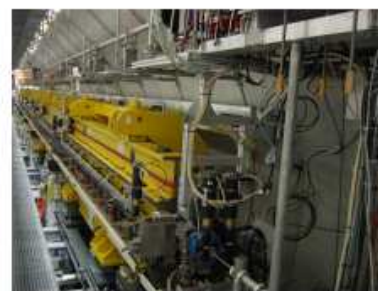
> 3rd harmonic sc module 3.9 GHz



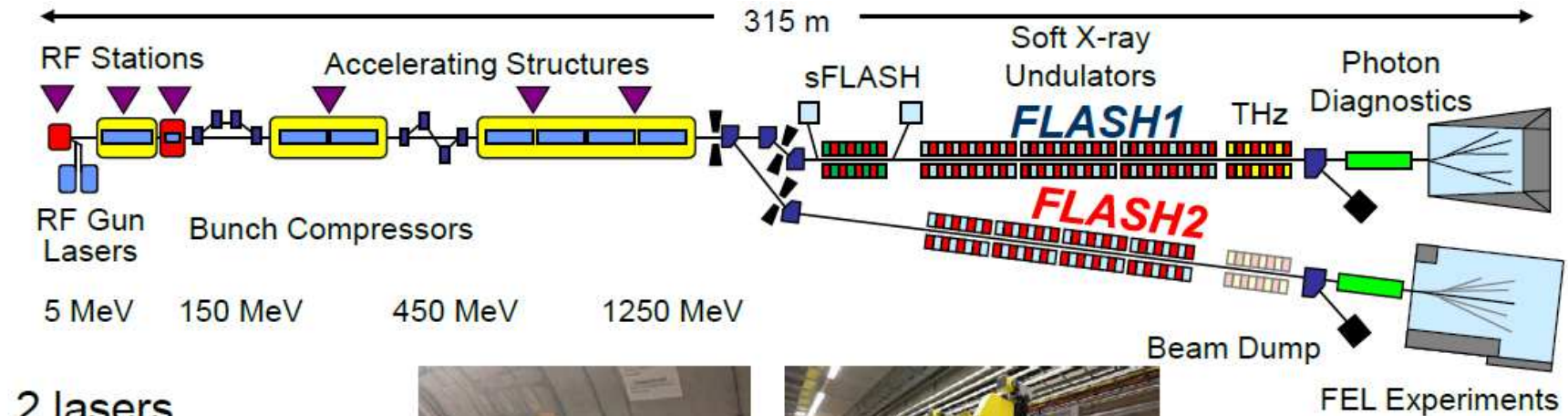
> TESLA type superconducting accelerating modules 1.3 GHz



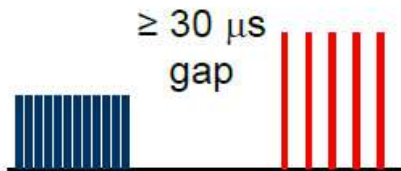
> FLASH1 fixed gap undulators



> FLASH1 Experimental Hall



2 lasers



> Extraction to FLASH2

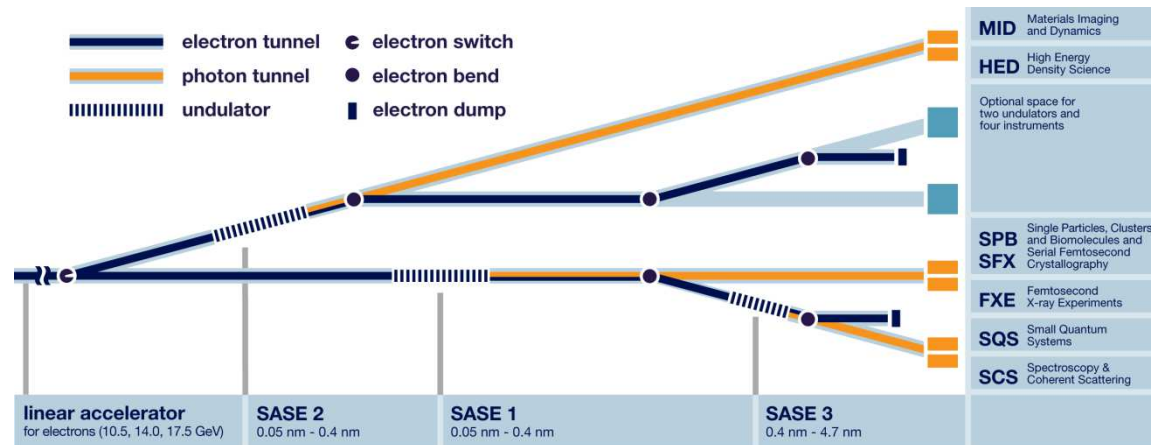
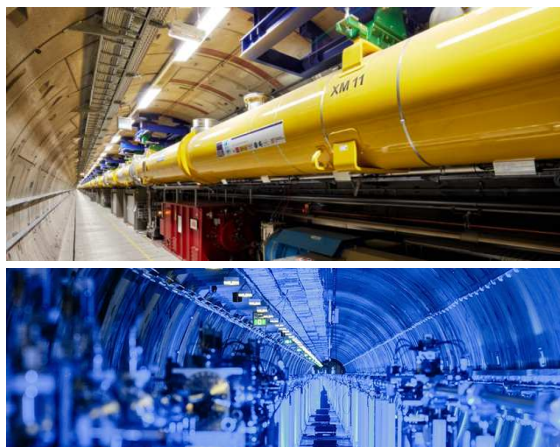
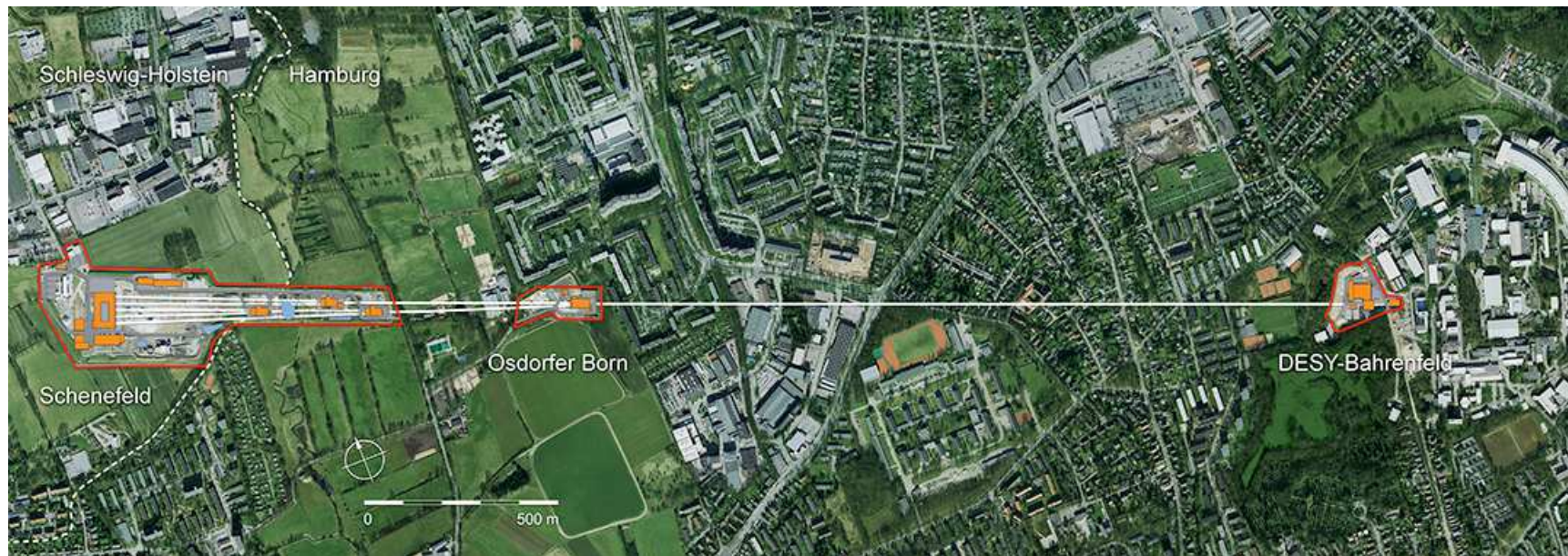


> FLASH2 variable gap undulators



> FLASH2 Experimental Hall

European XFEL

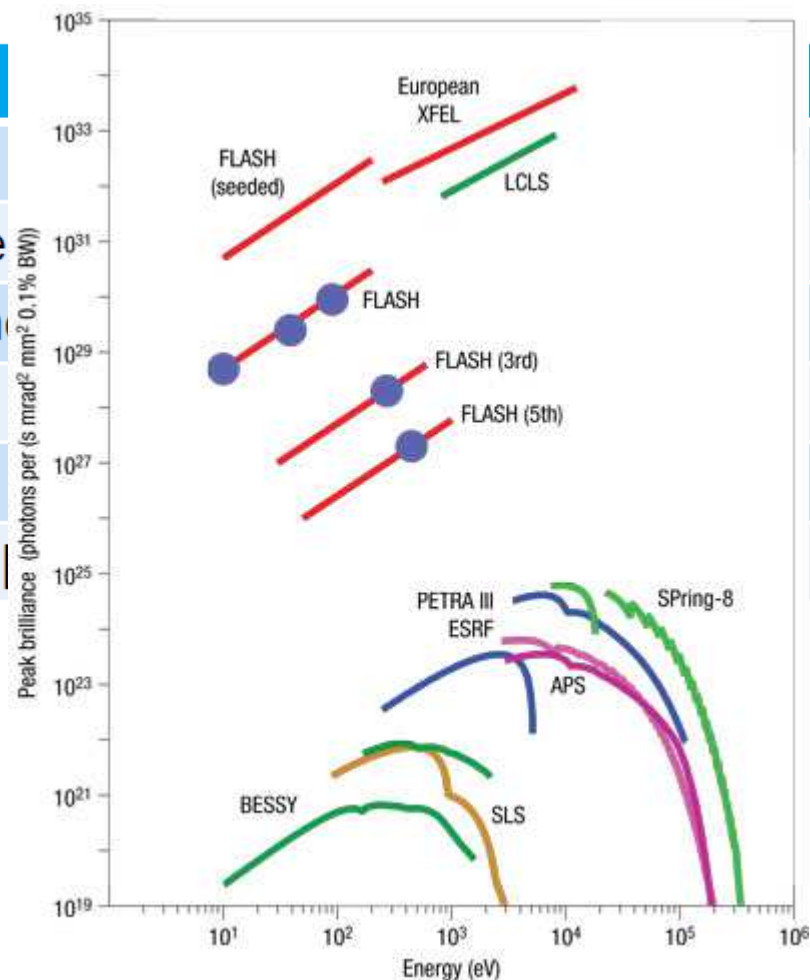


Typical Parameters of European XFEL and FLASH

	XFEL	FLASH
Max. energy [GeV]	17.5	1.25
Pulse repetition rate [Hz]	10	10*
Max. bunch frequency [MHz]	4.5	1
Max. pulse duration [μm]	600	800
Charge [nC]	0.02 – 1	<0.1 – 1
Photon wavelength [nm]	0.05 - 6	4.2 – 45

Typical Parameters of European XFEL and FLASH

Max. energy [GeV]
Pulse repetition rate
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Charge [nC]
Photon wavelength



FLASH

1.25

10*

1

800

<0.1 – 1

4.2 – 45

Introduction to the optical Synchronization System



Introduction – Optical Synchronization System

Provide a global, femtosecond stable reference for the synchronization of timing-critical systems of the accelerator



Introduction – Optical Synchronization System

Provide a global, femtosecond stable reference for the synchronization of timing-critical systems of the accelerator

Synchronization $\neq$ Timing

- machine trigger (10 Hz)
- digital clocks (LVDS)
- ps stability
- bunch train information
 - rep. rate / pattern
 - inj. laser / beamline
- ... and more...

Rear Transition Module

AMC



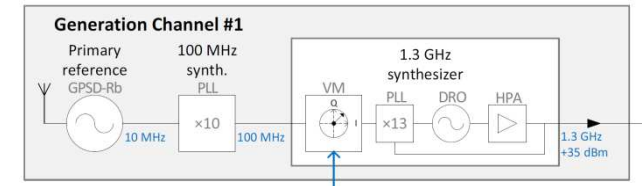
Hardware design @ Physics Department of Stockholm University

Introduction – Optical Synchronization System

Provide a global, femtosecond stable reference for the synchronization of timing-critical systems of the accelerator

> Global accelerator *"clock"*:

- RF Master Oscillator (MO)



Introduction – Optical Synchronization System

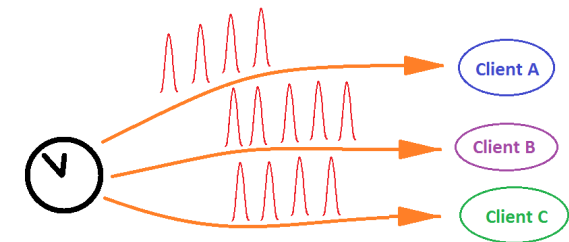
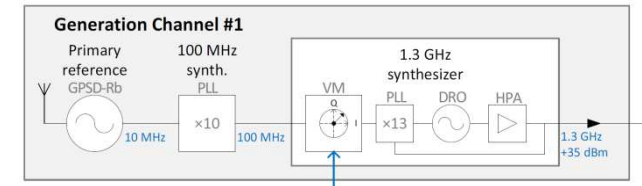
Provide a global, femtosecond stable reference for the synchronization of timing-critical systems of the accelerator

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> Optical Synchronization System:

- Distribute the clock without degrading its performance (jitter/uncertainty)
- Either provide the distributed signal to other subsystems or make use of the distributed signal directly



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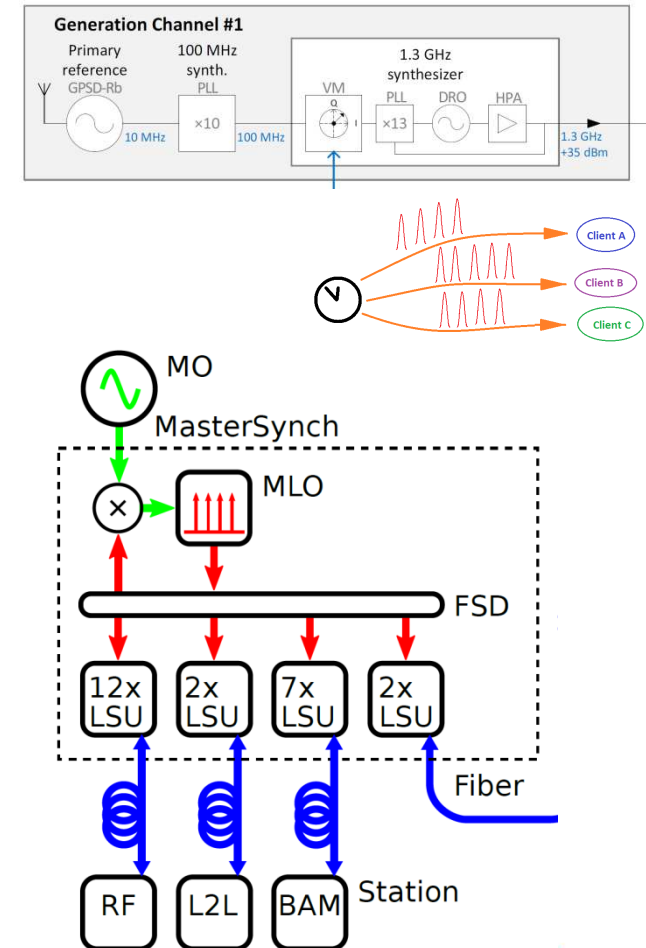
Building blocks

> Source: pulsed laser 'Master Laser Oscillator' (MLO)

- Locked to the MO

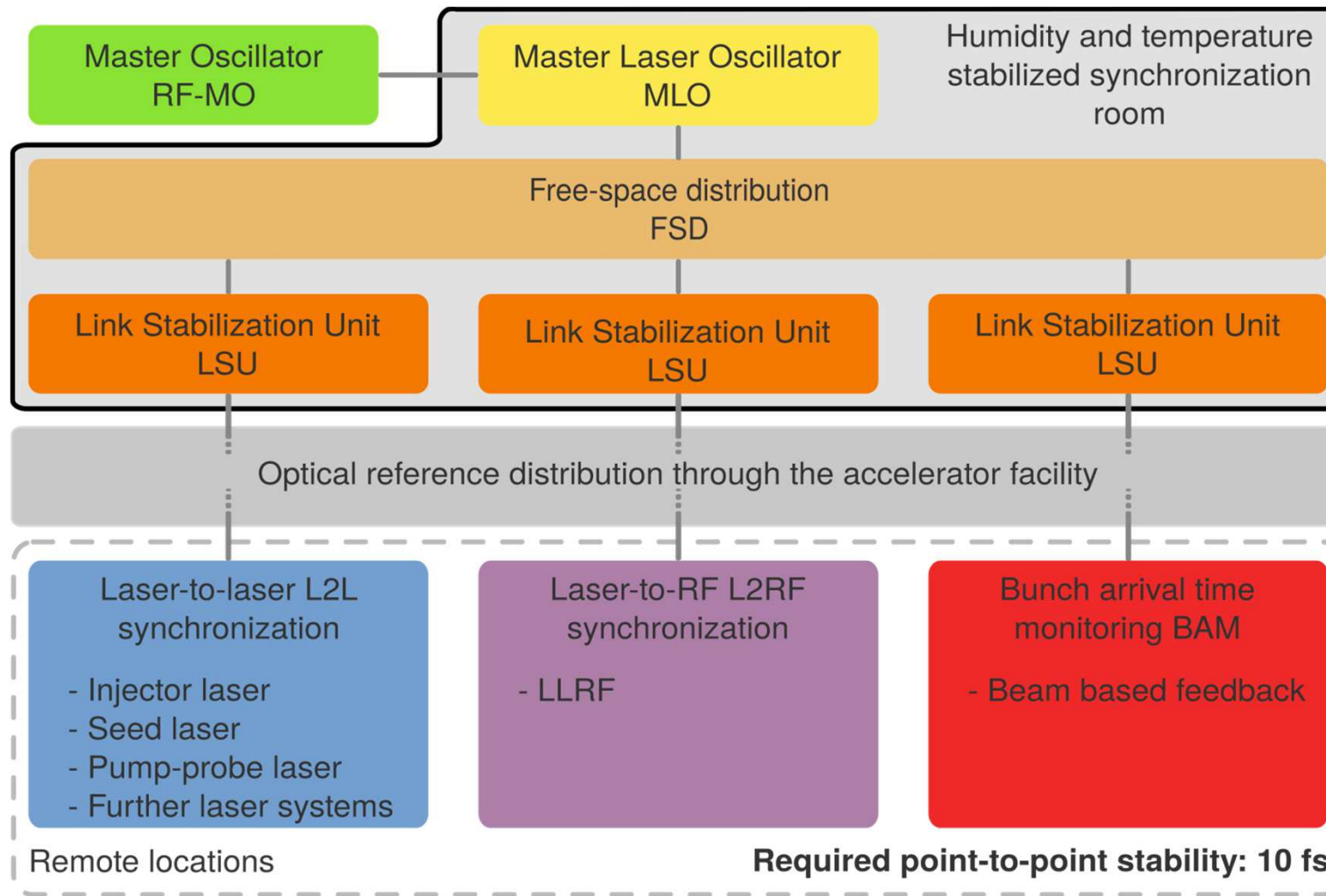
> Distribution medium: optical fiber

- Actively phase stabilized fiber links (LSU = Link Stabilization Unit)



Introduction – Sync Endstations

Provide a global, femtosecond stable reference for the synchronization of timing-critical systems of the accelerator

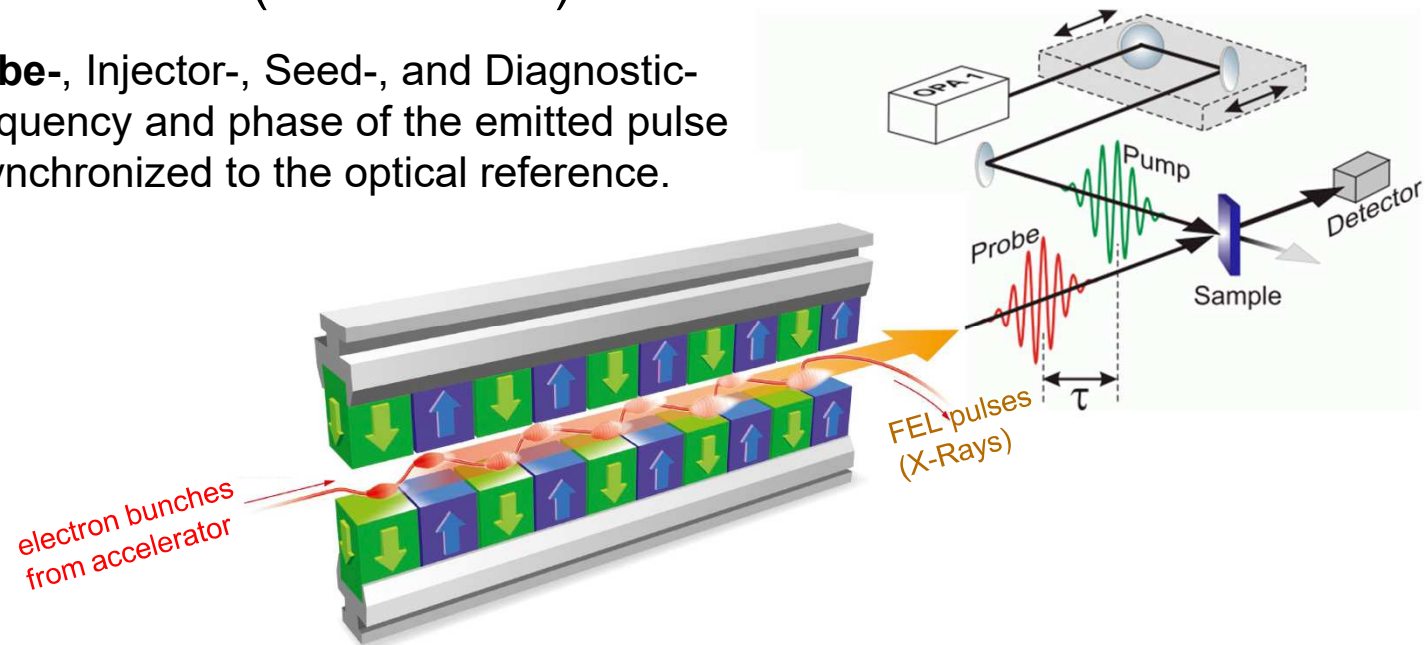


Introduction – Sync Endstations

Provide a global, femtosecond stable reference for the synchronization of timing-critical systems of the accelerator

> Laser synchronization (L2RF & L2L)

- **Pump-Probe-**, Injector-, Seed-, and Diagnostic-lasers: Frequency and phase of the emitted pulse train are synchronized to the optical reference.

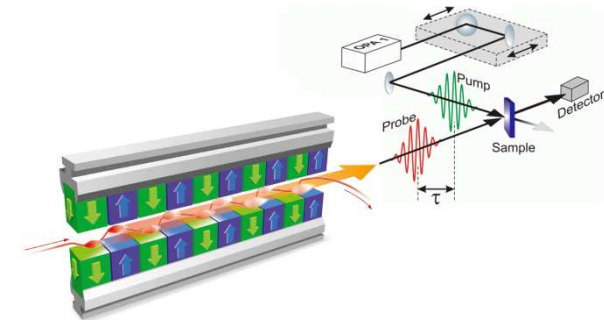


Introduction – Sync Endstations

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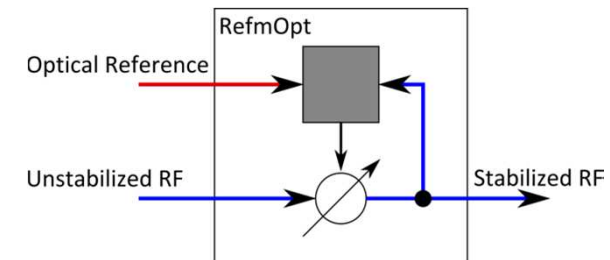
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> RF synchronization (REFM-OPT)

- Providing a synchronized reference for the precise **control of the accelerating field** in the cavities (LLRF) depends on a stable RF reference which is provided by the synchronization system

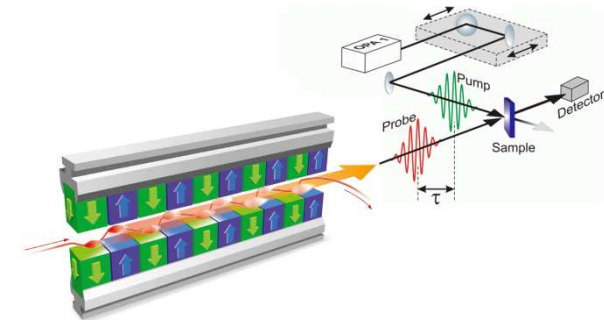


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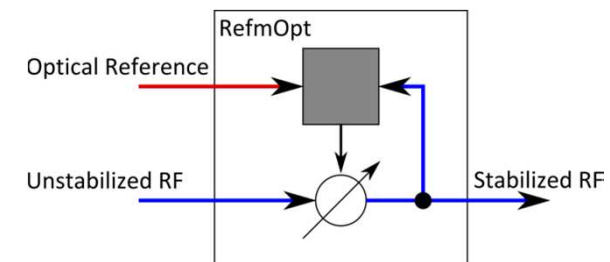
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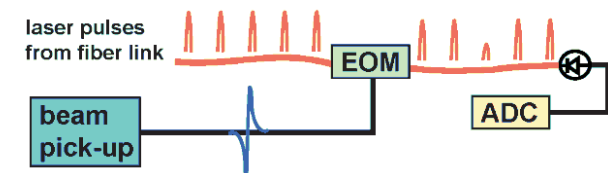
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> Bunch arrival time measurements (BAM)

- **Beam-Based Feedback** to synchronize (= stabilize) the arrival time of individual bunches to the optical reference

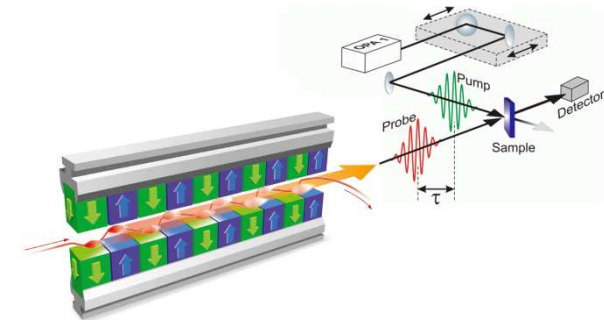


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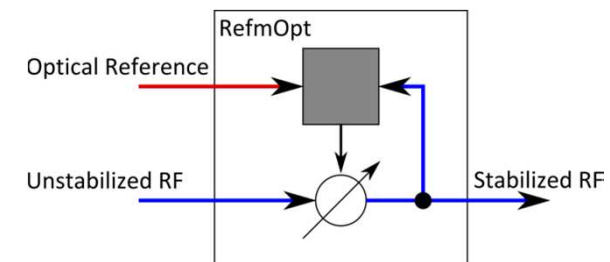
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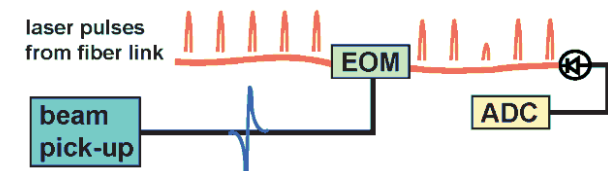
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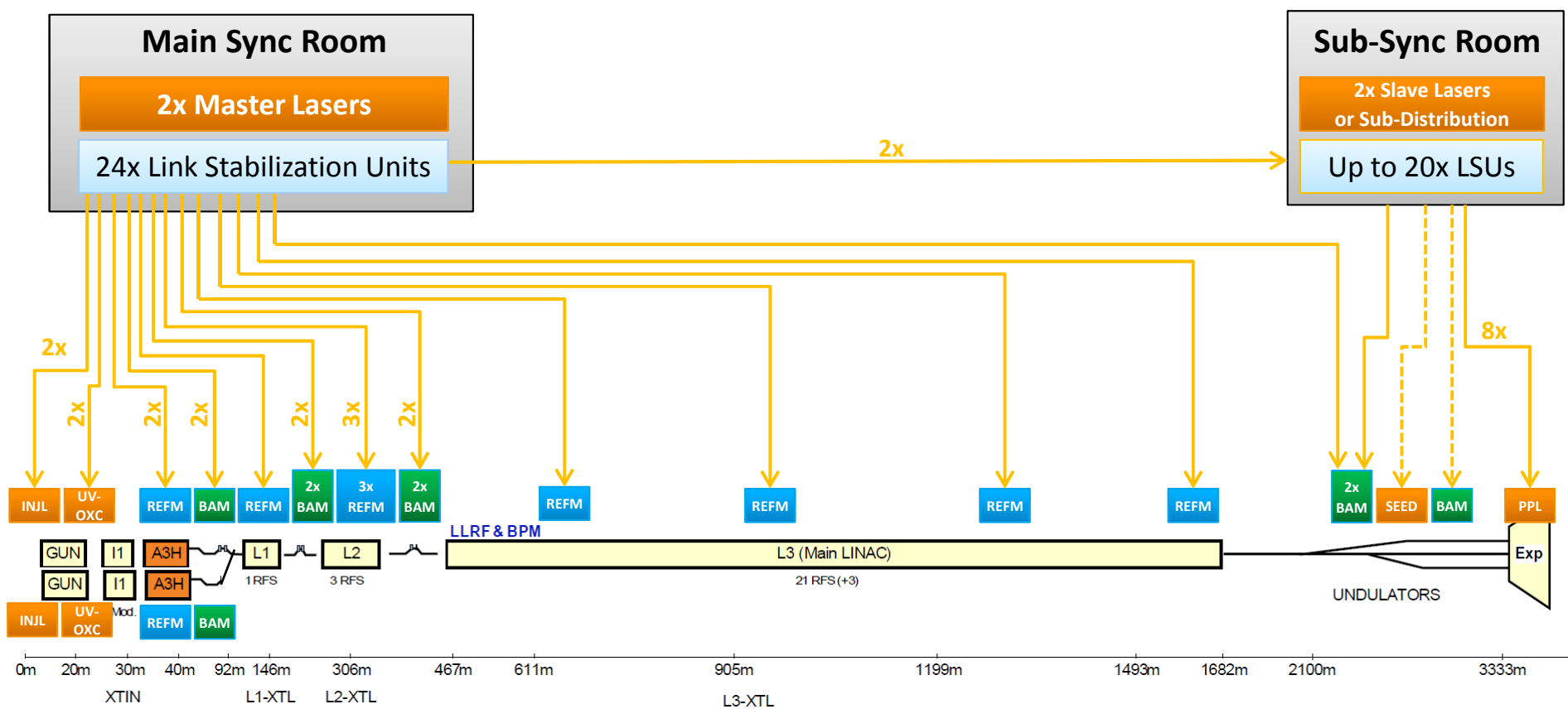
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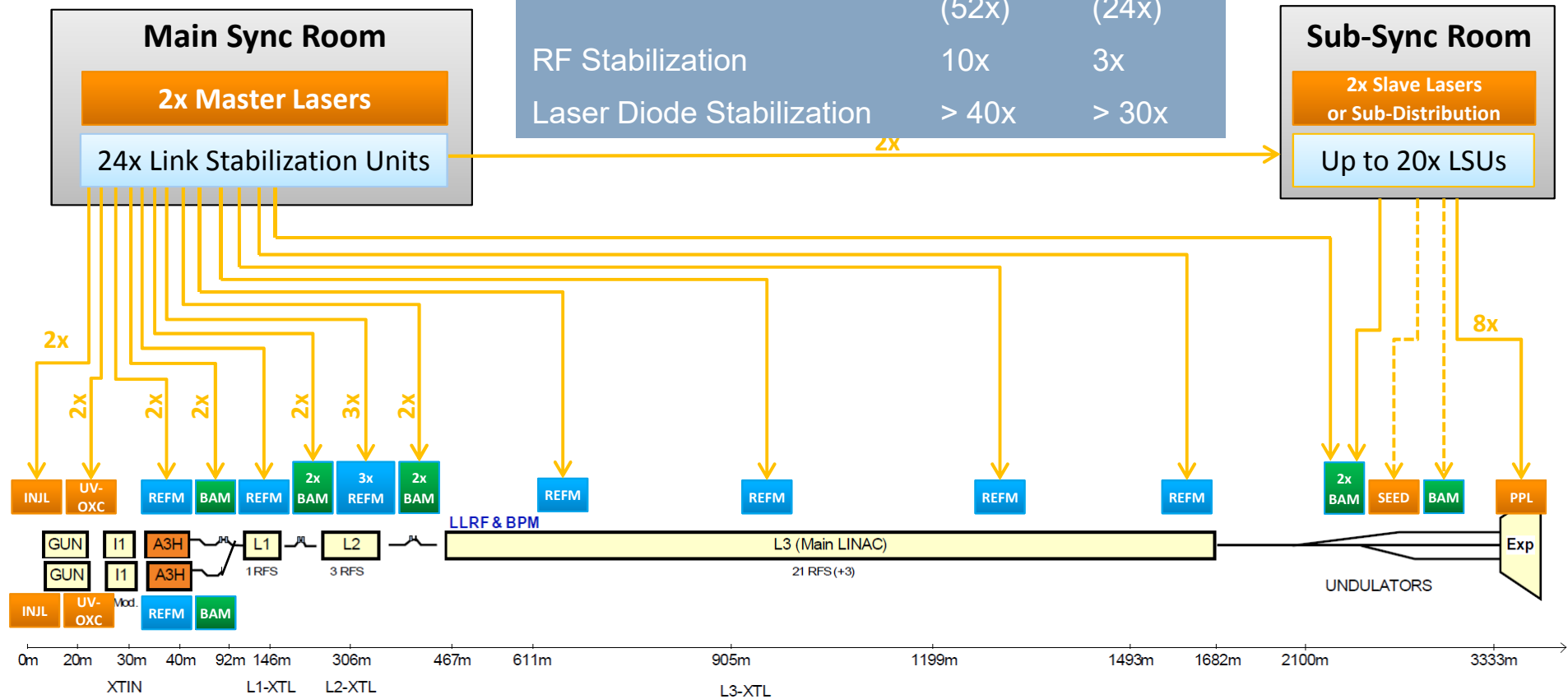
Poster by Michele Viti TUPHA125

Optical Links + End Stations at the European XFEL



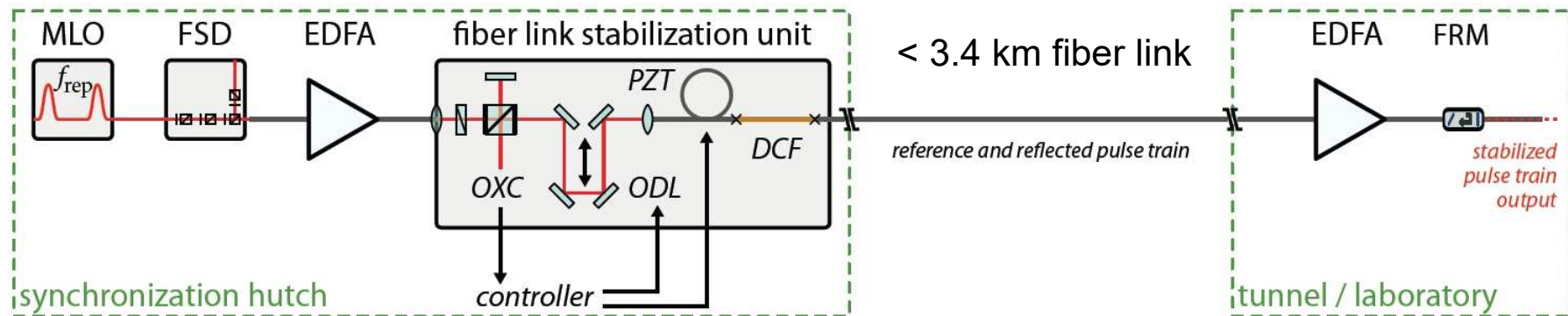
Optical Links + End Stations at the European XFEL

Digital Feedback Loops	E-XFEL	FLASH
Laser Synchronization	10x (15x)	7x (10x)
Link Stabilization	33x (52x)	16x (24x)
RF Stabilization	10x	3x
Laser Diode Stabilization	> 40x	> 30x

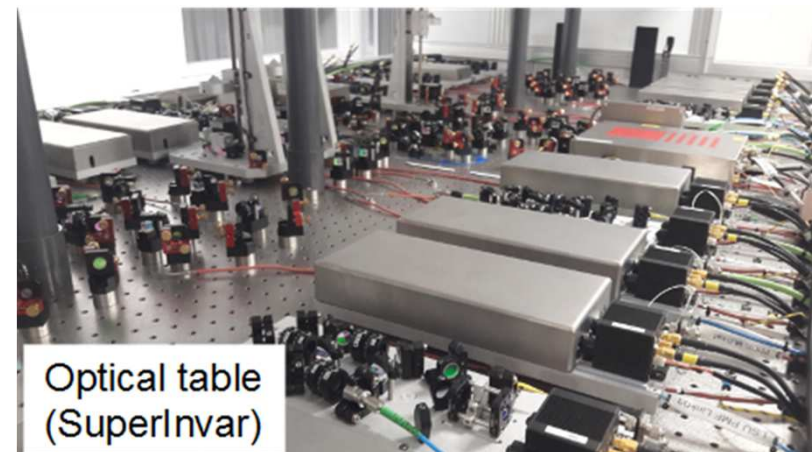


Introduction – Fiber Link Stabilization

- > Long- and short-term phase-stable optical pulse train has to be distributed along ≤ 3.4 km
- > Active stabilization of optical fiber link length / transit time

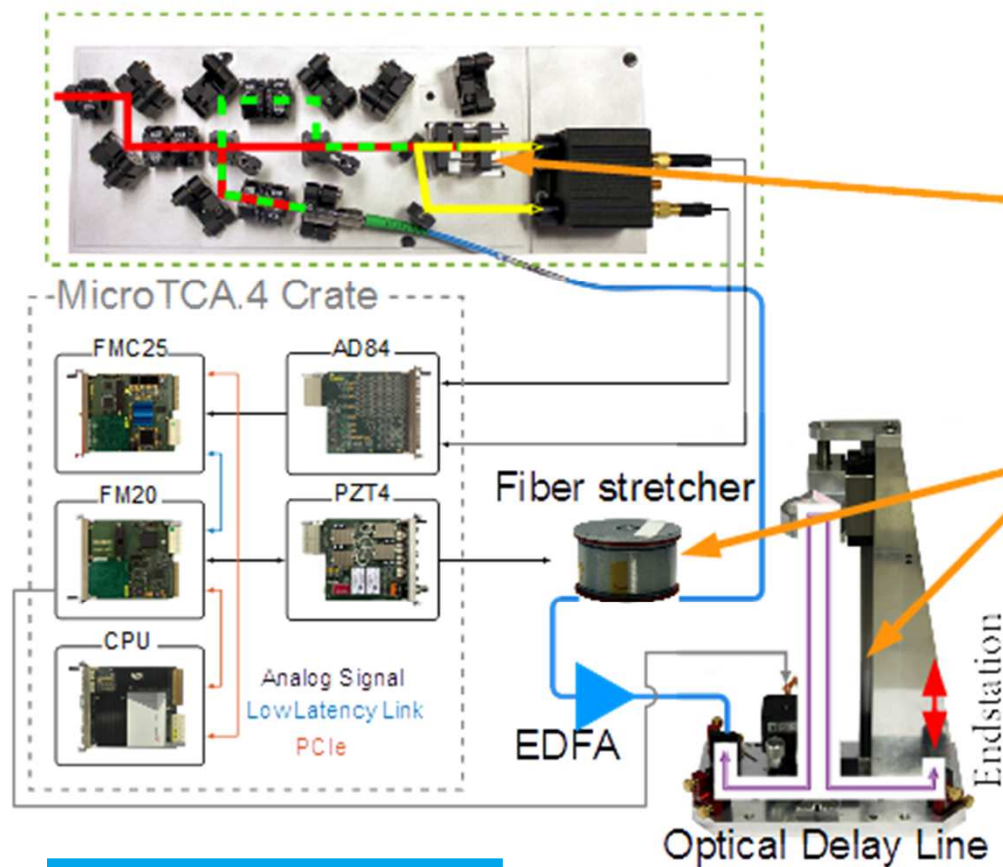


MLO – Master Laser Oscillator
FSD – Free Space Distribution
EDFA – Erbium-Doped Fiber Amplifier
OXC – Balanced Optical Cross-Correlator
ODL – Optical Delay Line
PZT – Piezo Fiber Stretcher
DCF – Dispersion Compensating Fiber
FRM – Faraday Rotating Mirror



MicroTCA Setups for Synchronization

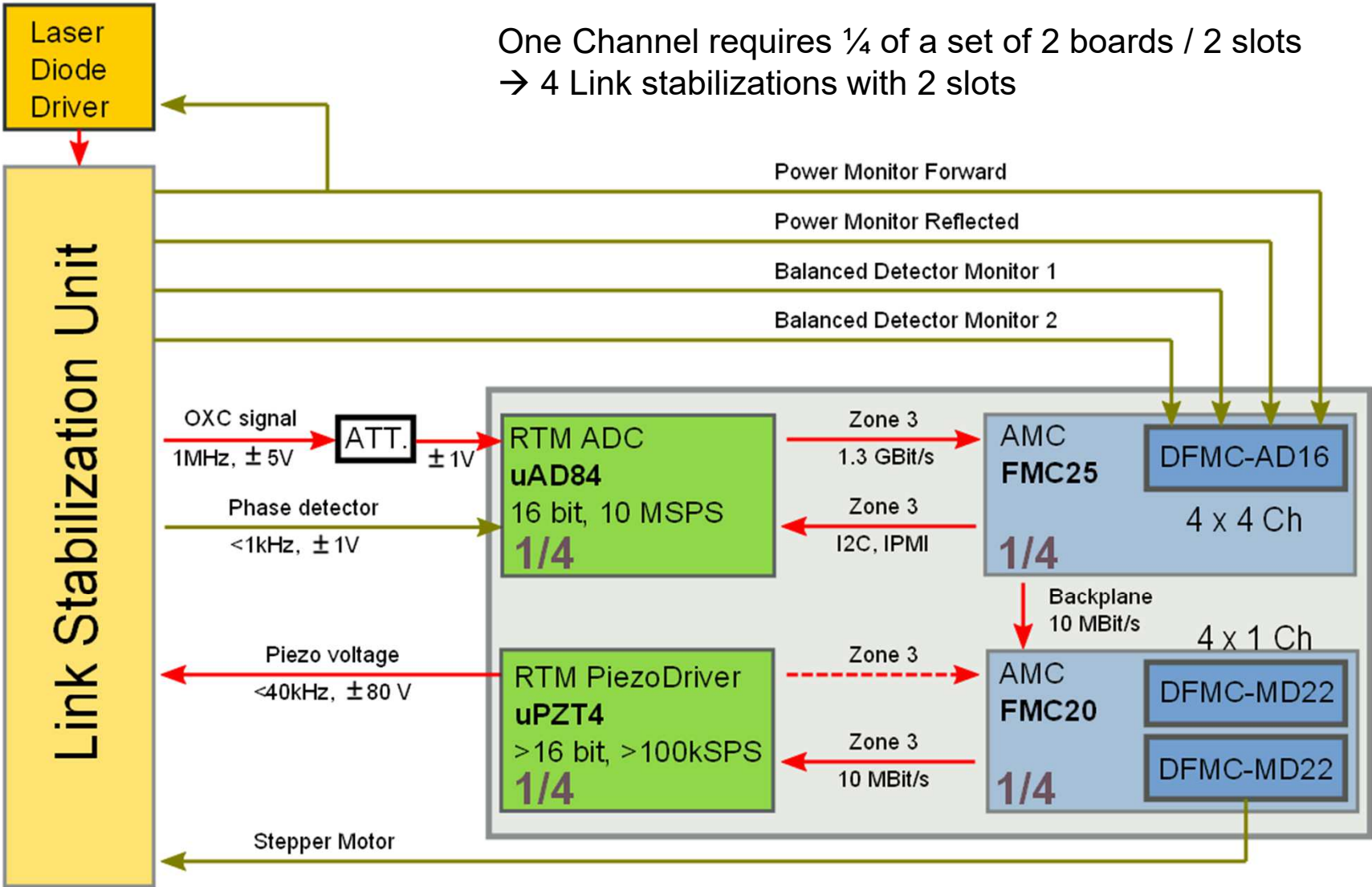
Optomechanics and MicroTCA Boards



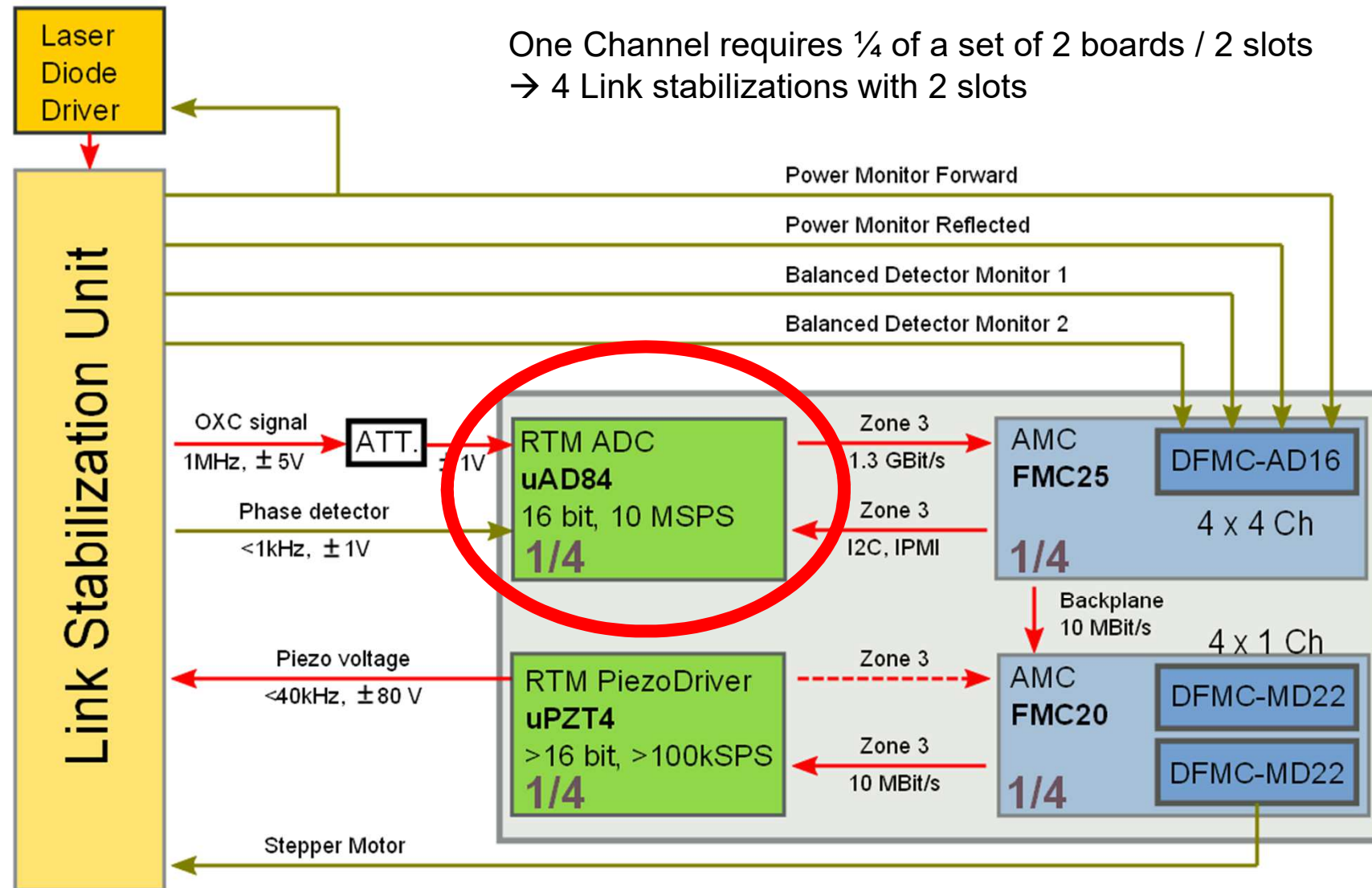
Courtesy: C. Sydlo
Picture by M. Heuer

- Installed fibers influenced by temperature, humidity, vibration
- The balanced optical cross-correlator (OXC) detects timing changes
- The pulse propagation time through the stabilized path is held constant by a fiber stretcher and a motorized optical delay line.
- A lot of custom optomechanics

MTCA Setups for Sync – LSU Control



MTCA Setups for Sync – LSU Control: Building Blocks

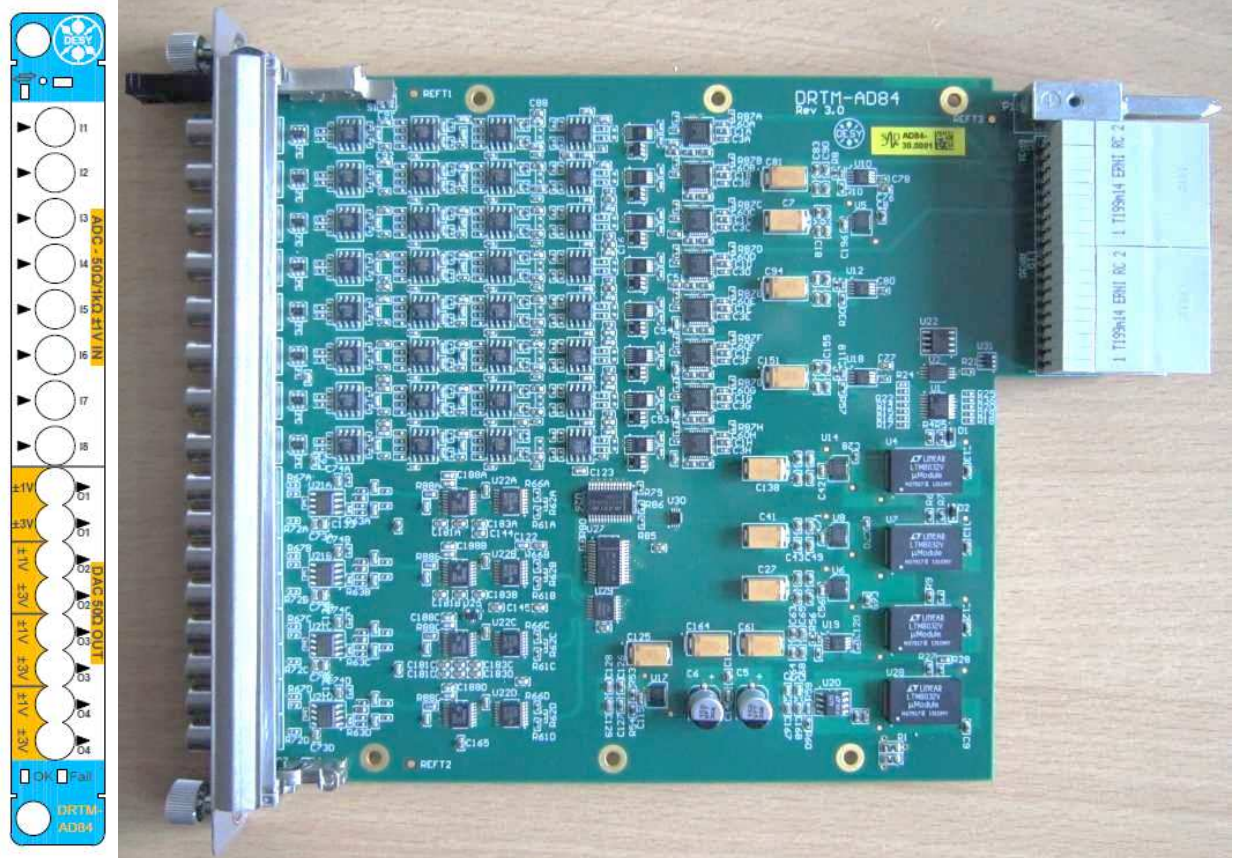


MTCA Setups for Sync – LSU Control: Building Blocks

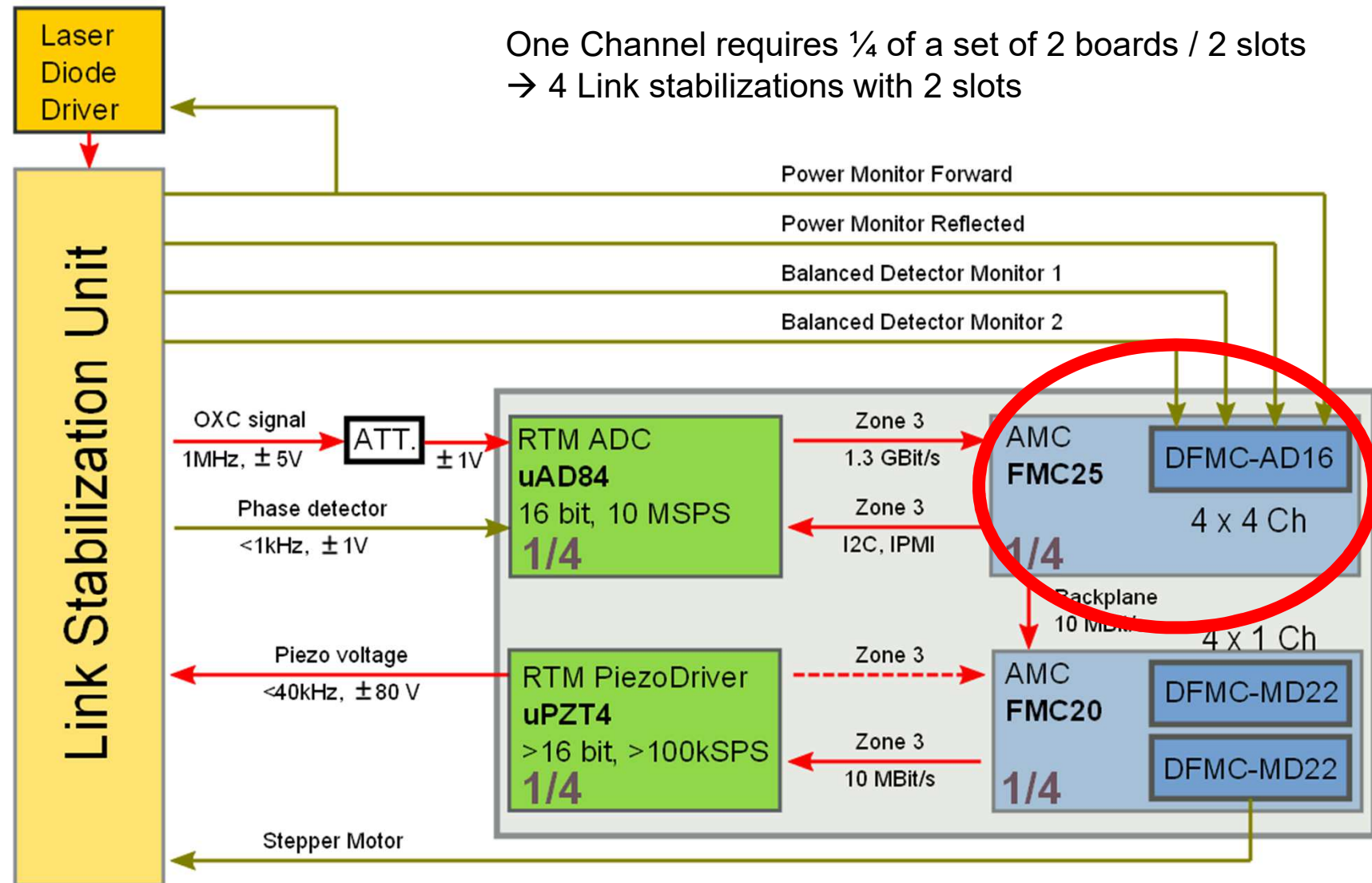
Digitizer-RTM

“DRTM-AD84”

- 8 x ADC:
 - 16 bit
 - 2.7 MSPS (up to 10)
 - 50 Ω or 1 k Ω
 - 90 MHz (2 MHz)
 - ± 1 V
- 4 x DAC
 - 16 bit
 - 1 (16) MSPS
 - ± 1 V / ± 3 V @ 50 Ω
- Zone 3: D1.0 / D1.1



MTCA Setups for Sync – LSU Control: Building Blocks

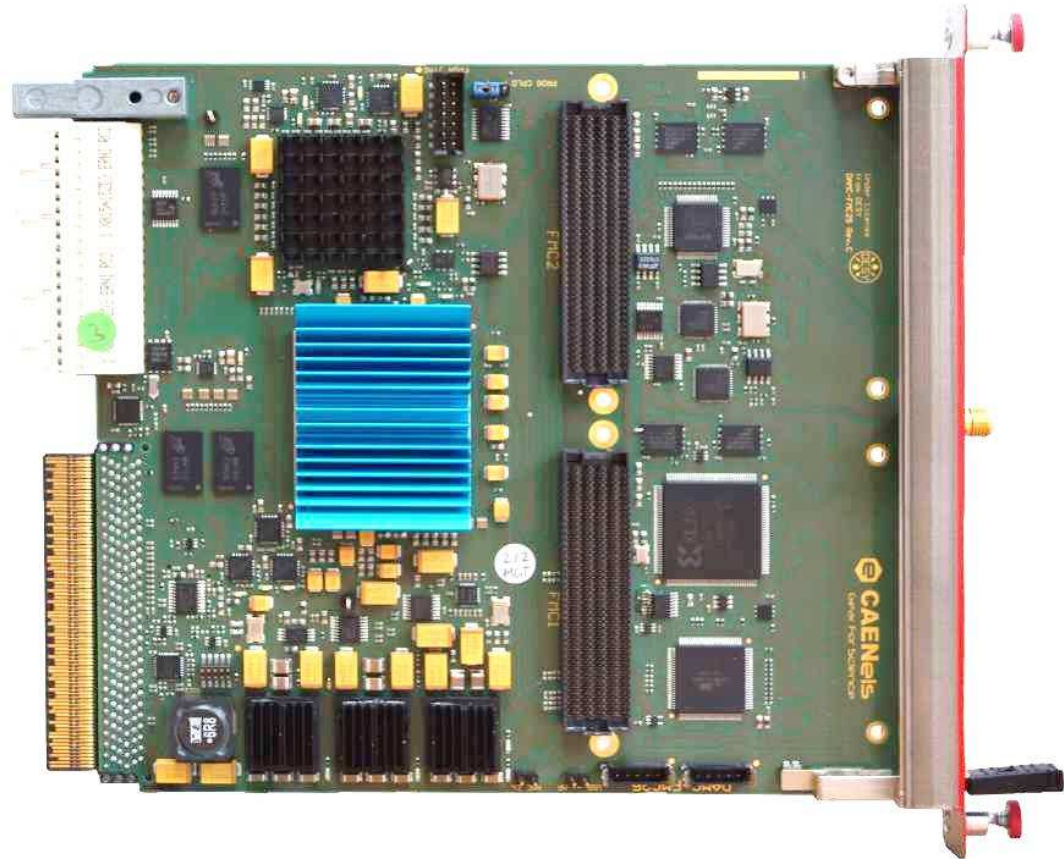


MTCA Setups for Sync – LSU Control: Building Blocks

Controller-AMC

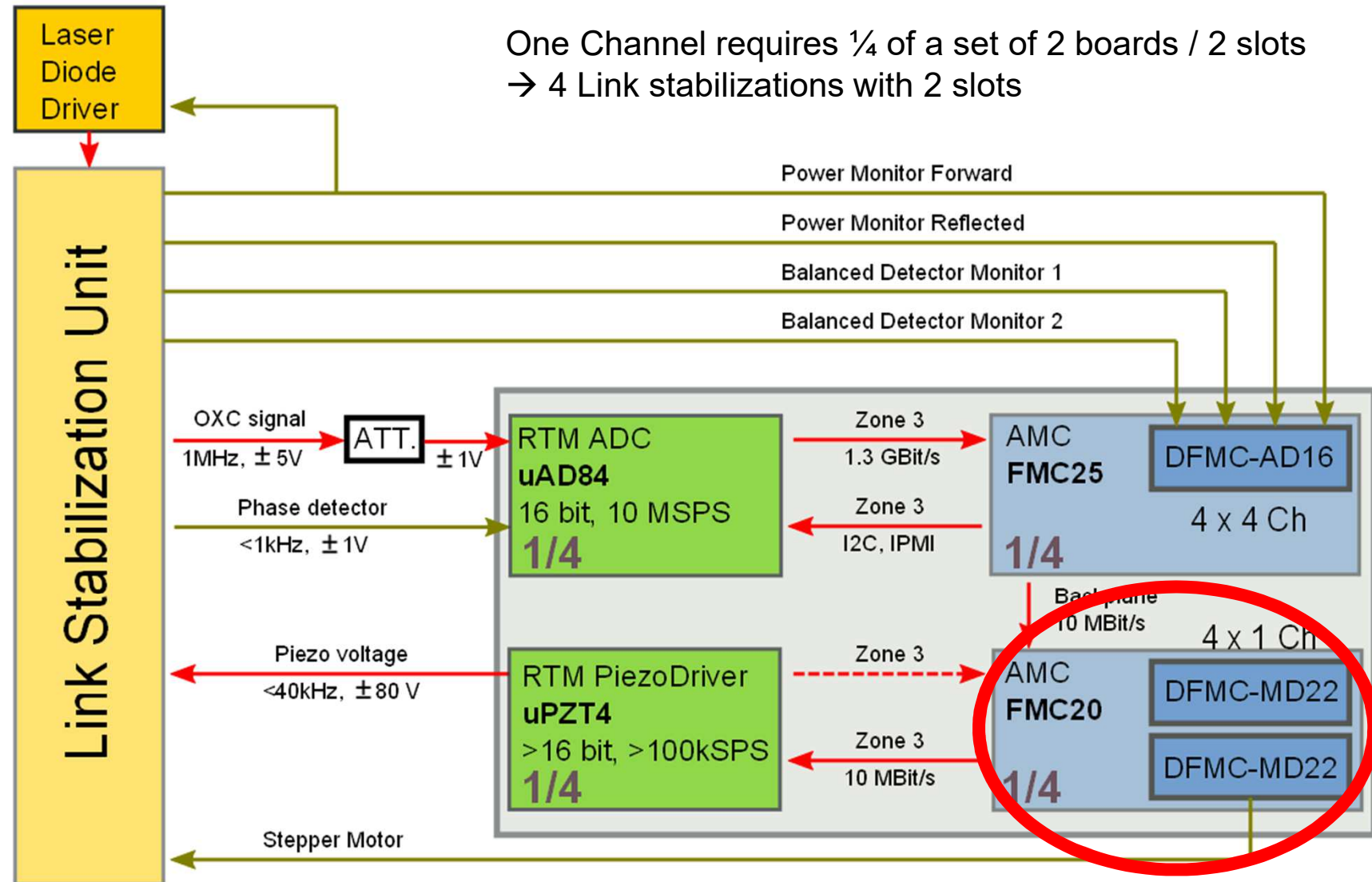
“DAMC-FMC25”

- Processing: Virtex 5
 - XC5VFX70T
 - XC5VFX100T
- Communication:
 - Spartan 6
- 2 x FMC (HPC)
- Zone 3: D1.1 / D1.2 / D1.3



Available at CAENels

MTCA Setups for Sync – LSU Control: Building Blocks



MTCA Setups for Sync – LSU Control: Building Blocks

Carrier-AMC

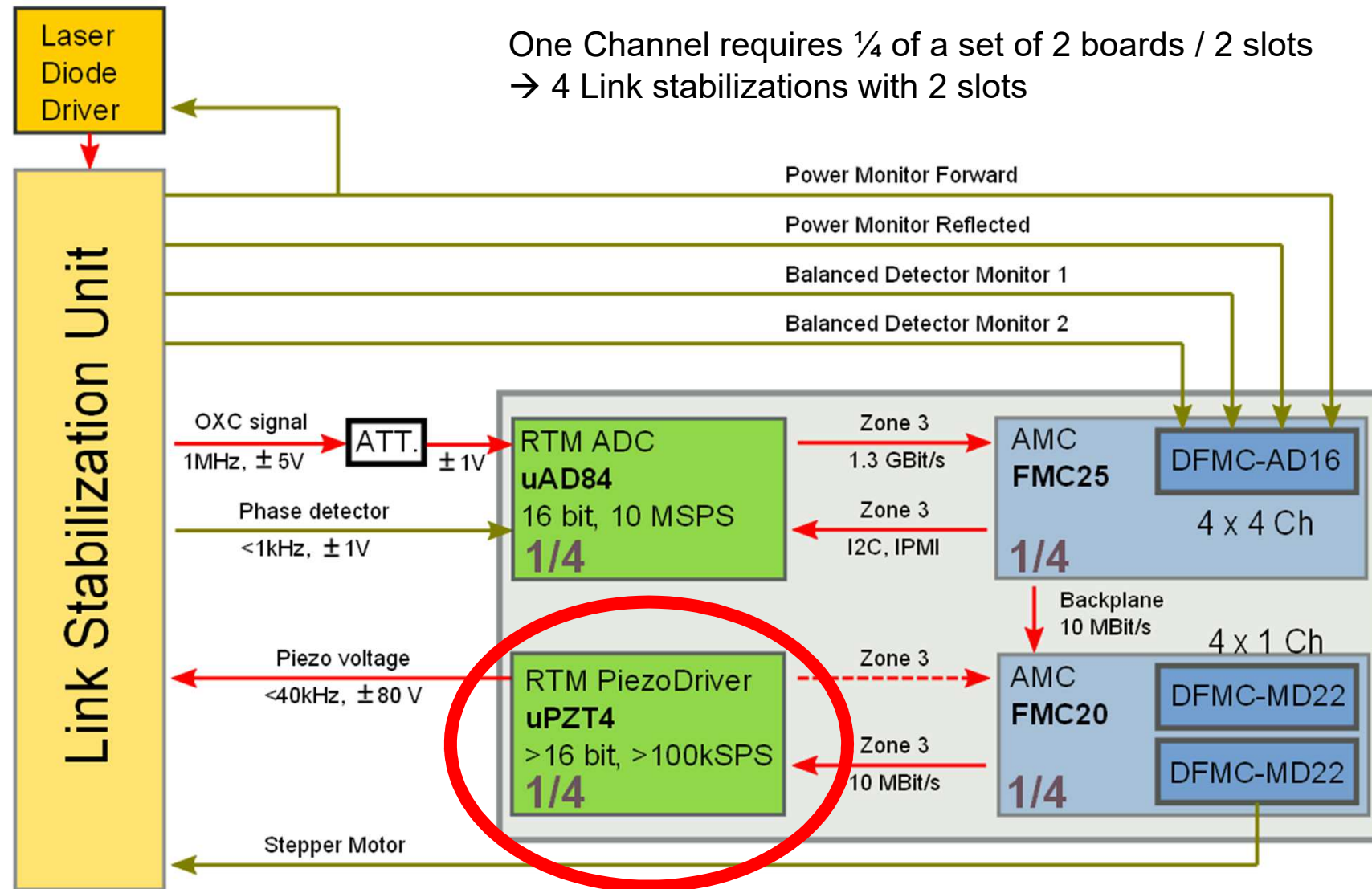
“DAMC-FMC20”

- Processing:
 - Spartan 6 (LX150)
- Communication:
 - Spartan 6 (LX45)
- 2 x FMC (HPC/LPC)
- Zone 3: D1.0



Available at CAENels

MTCA Setups for Sync – LSU Control: Building Blocks

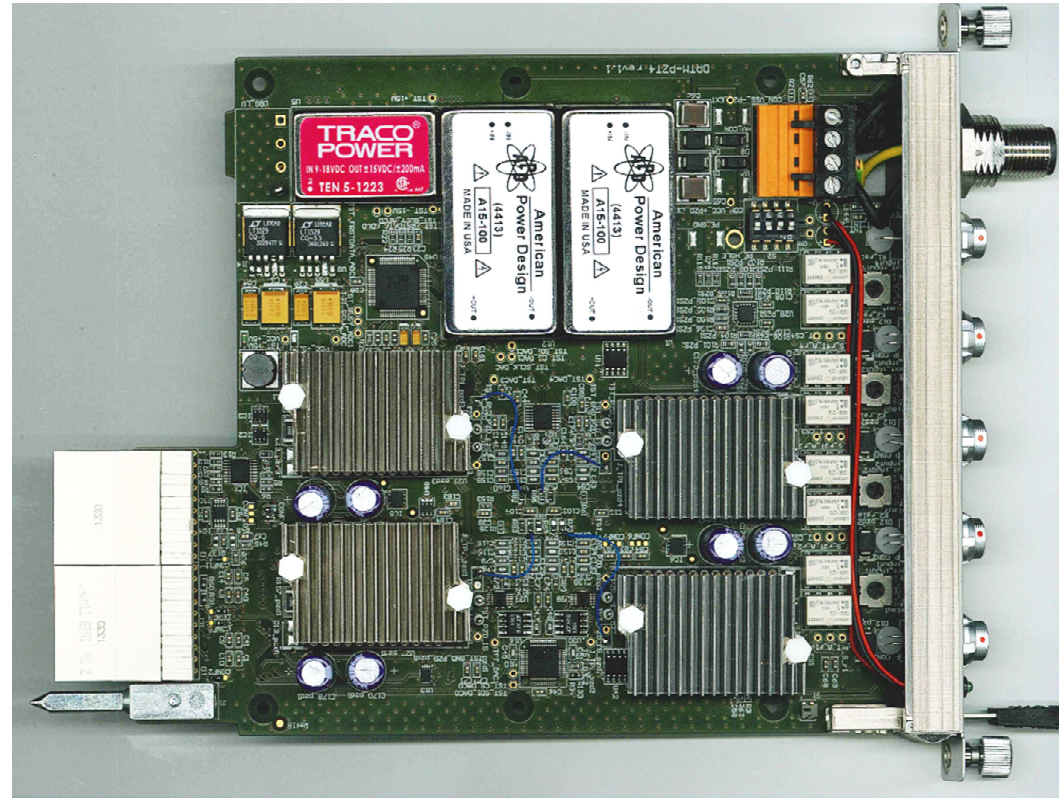


MTCA Setups for Sync – LSU Control: Building Blocks

Piezo Driver-RTM

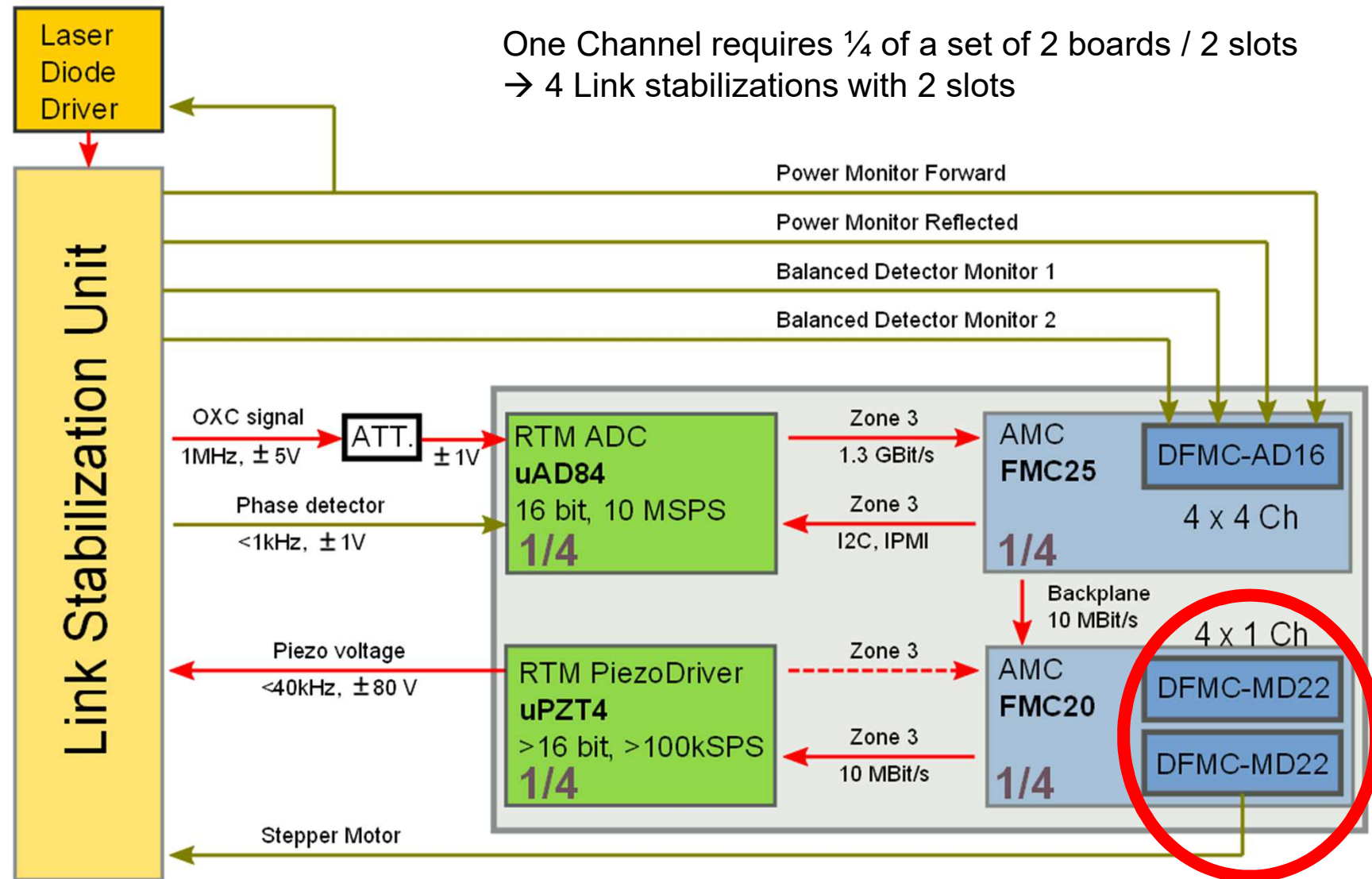
DRTM-PZT4

- 4 x Channel
- HV-Supply
 - On-board ± 100 V
 - Ext. input
- On-board DACs
- Monitoring ADCs
- Interlock support
- Metal-cover
- Zone 3: D1.0 / D1.1
D1.2



soon commercially available

MTCA Setups for Sync – LSU Control: Building Blocks

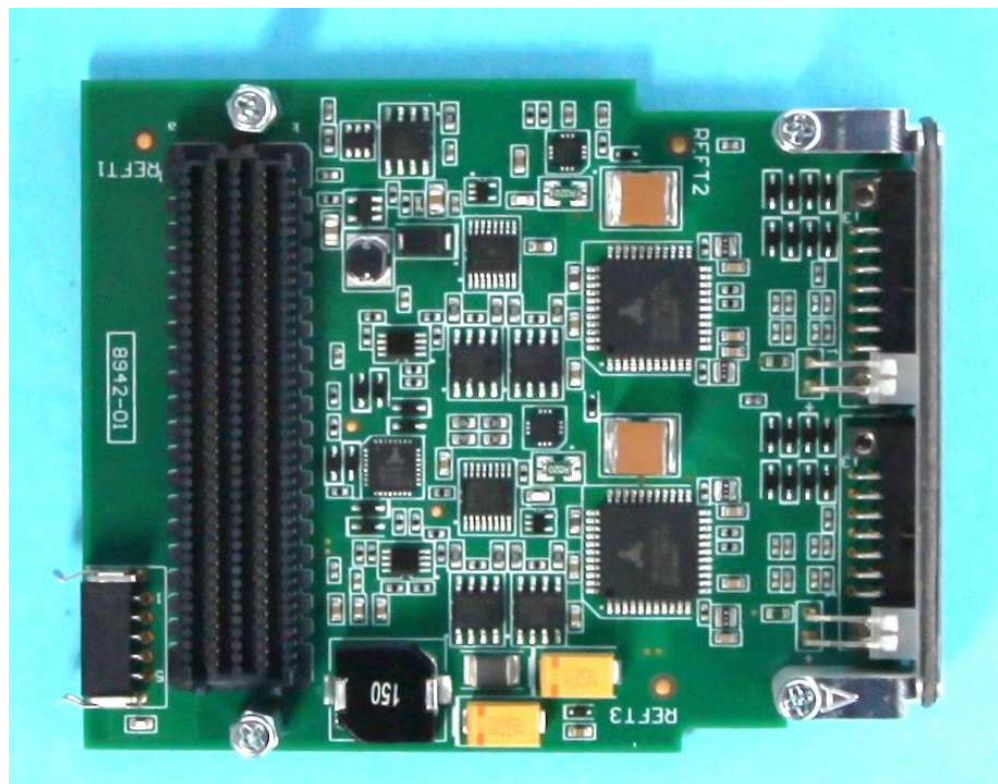


MTCA Setups for Sync – LSU Control: Building Blocks

Motor Driver-FMC

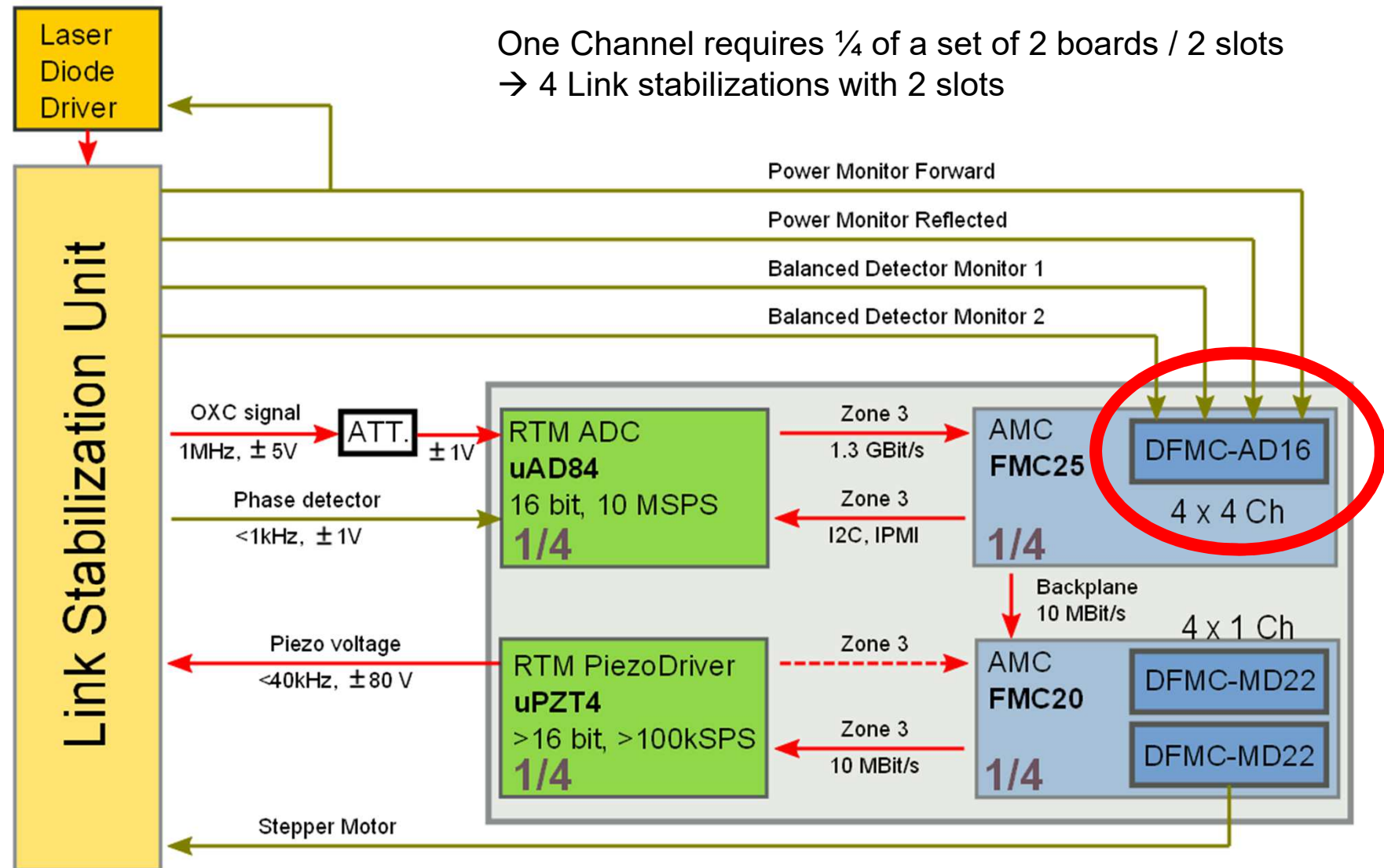
“DFMC-MD22”

- Stepper Motor Driver
- 2 x Channel
- End switch readout
- Encoder readout



Available at CAENels

MTCA Setups for Sync – LSU Control: Building Blocks

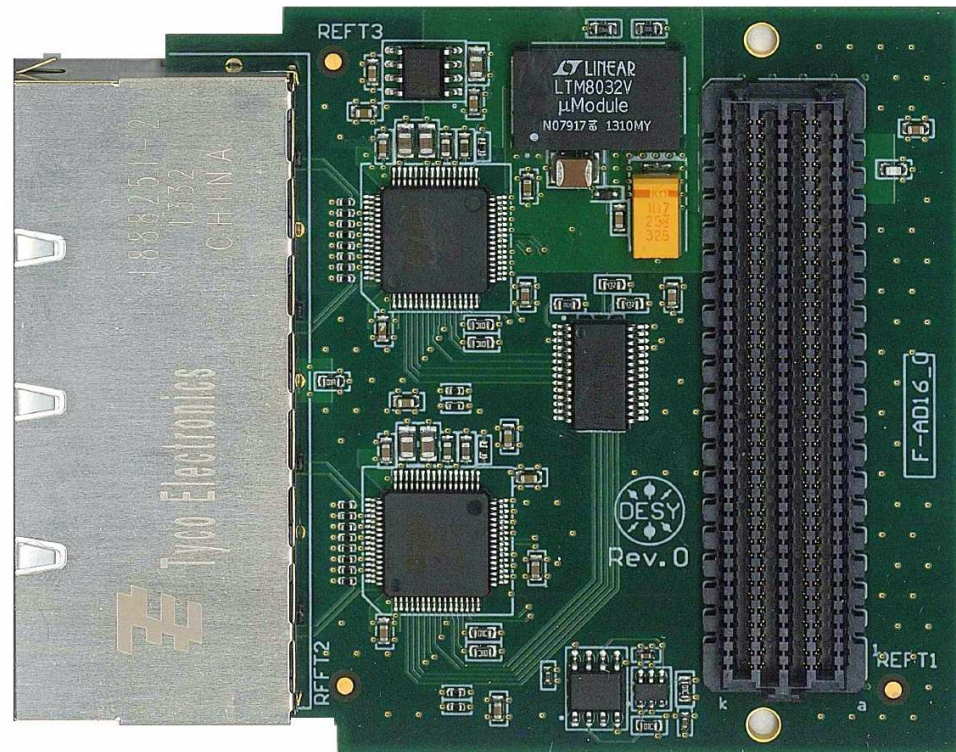


MTCA Setups for Sync – LSU Control: Building Blocks

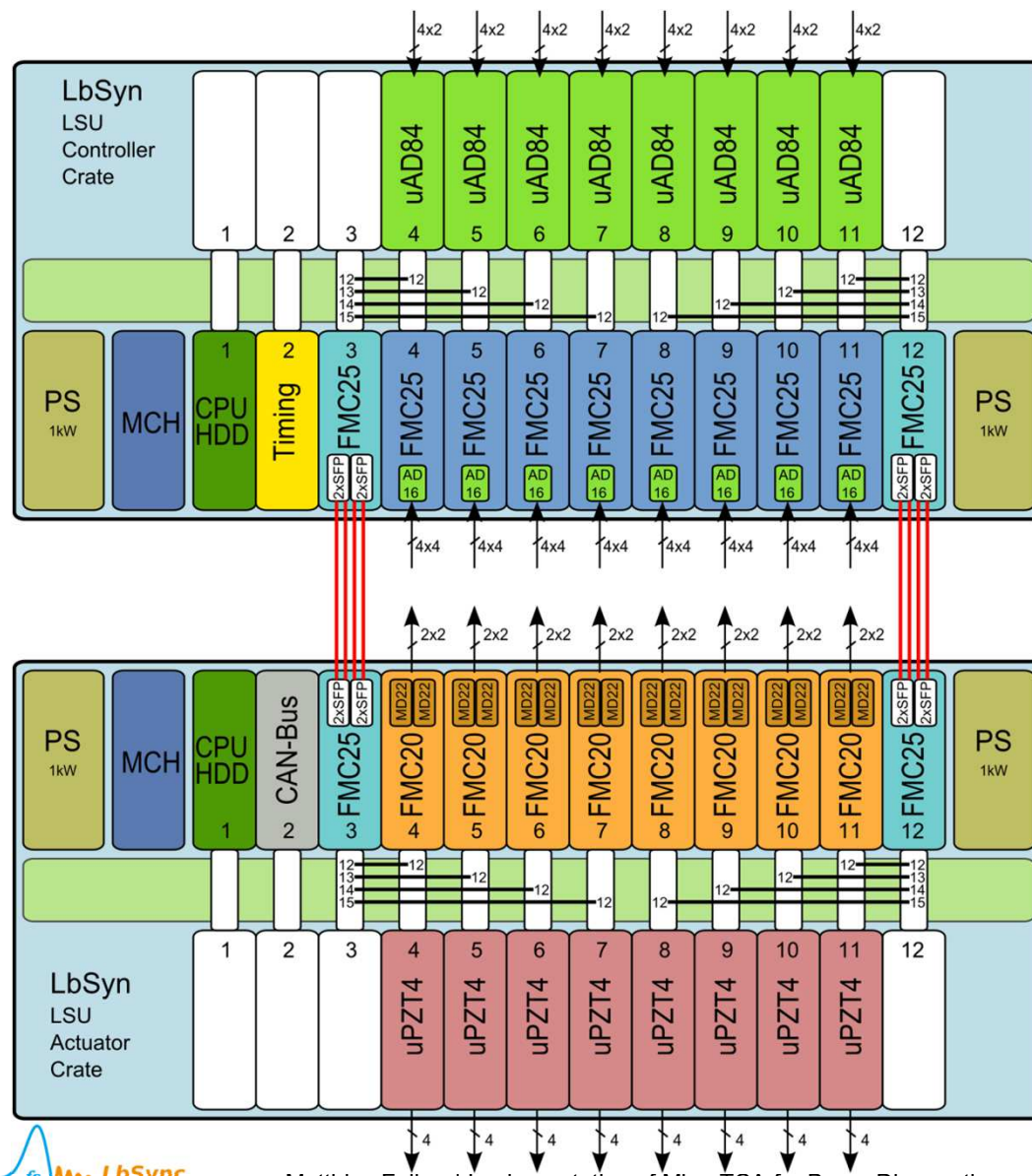
Monitor ADC-FMC

“DFMC-AD16”

- 16 x Channels
 - 18 bit
 - >100 kSPS
 - 1 M Ω
 - 23 kHz / 15 kHz
 - ± 10 V / ± 5 V



LSU Control: MTCA Crate Configuration (max. 32 Links)



ADCs

Controllers

Motor Actuators

Piezo Actuators

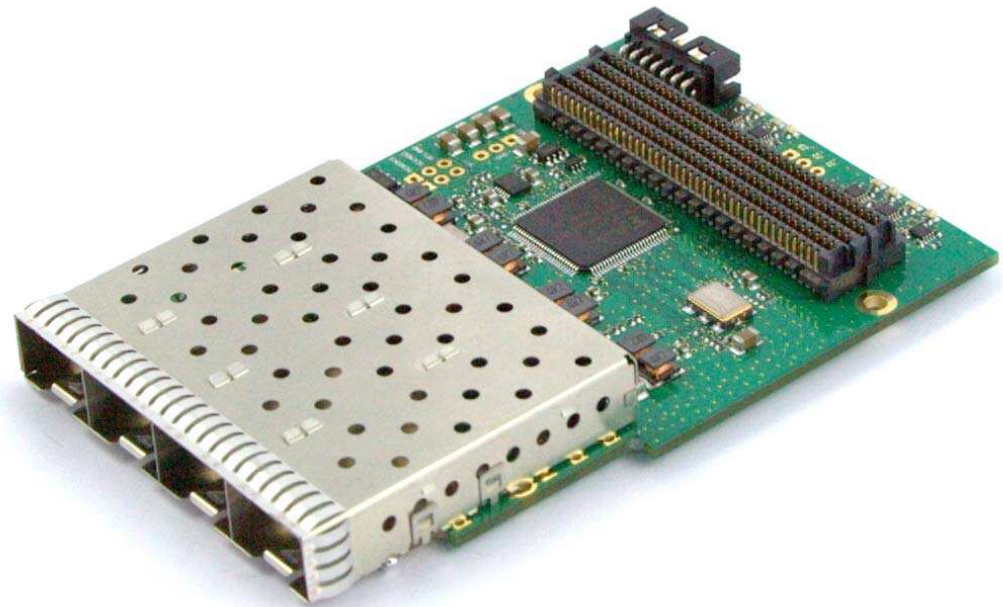


MTCA Setups for Sync – LSU Control: Building Blocks

SFP Communication-FMC

“DFMC-SFP4”

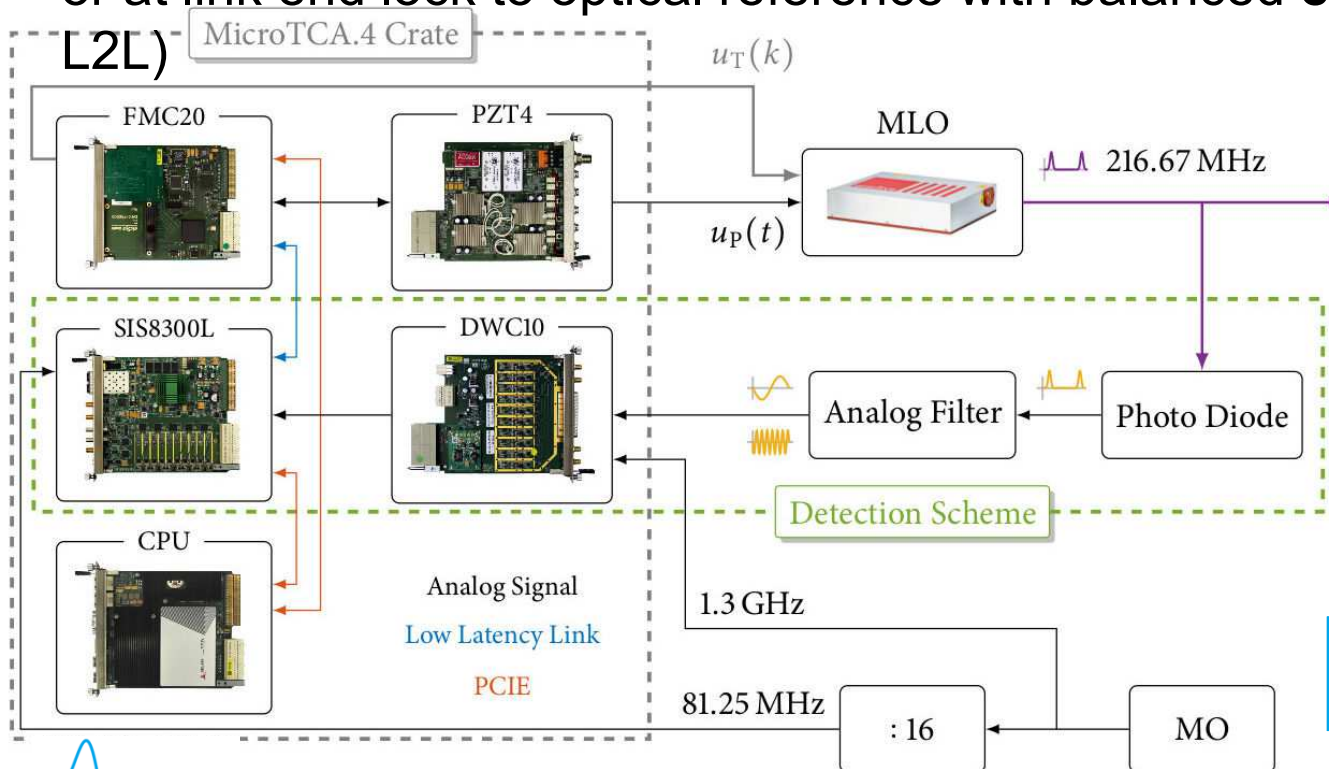
- Channels:
 - 4x no front panel
 - 2x with front panel
- Vita 57.1 compatible
- V_{adj} can vary from 3.3 V down to 1.5 V
- I2C-controlled oscillator (10-280 MHz)



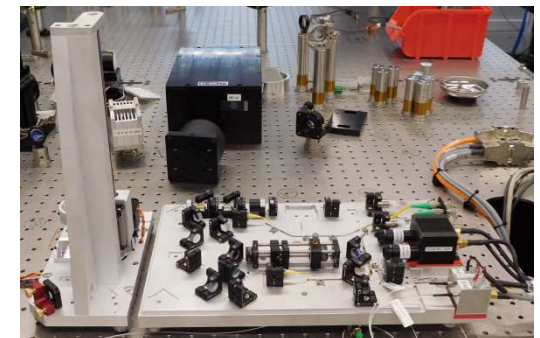
Available at CAENels

Laser Synchronization Setup

- **RF-lock** to fundamental rep. rate and higher harmonic at 1.3 GHz (+ rep. rate)
 - Downconversion (like LLRF) with non-IQ sampling and digital IQ extraction -> phase calculation
 - Problem of AM/PM effect in photo diode
- Low-noise and virtually drift-free lock to RF reference with **MZI Setup** (L2RF) or at link end lock to optical reference with balanced **cross correlator** (OXC-L2L)

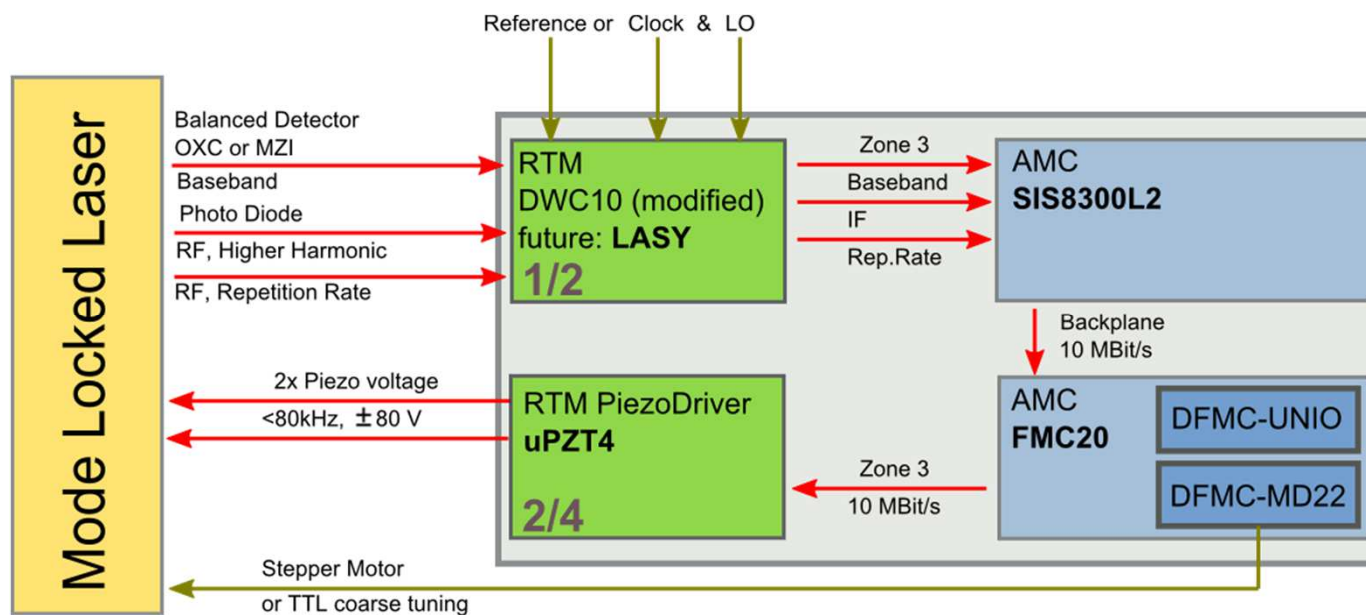


OXC Setup for pure optical lock to reference from link:



Courtesy: J. Mueller
Picture by M. Heuer

MTCA Setups for Sync – Laser Synchronization

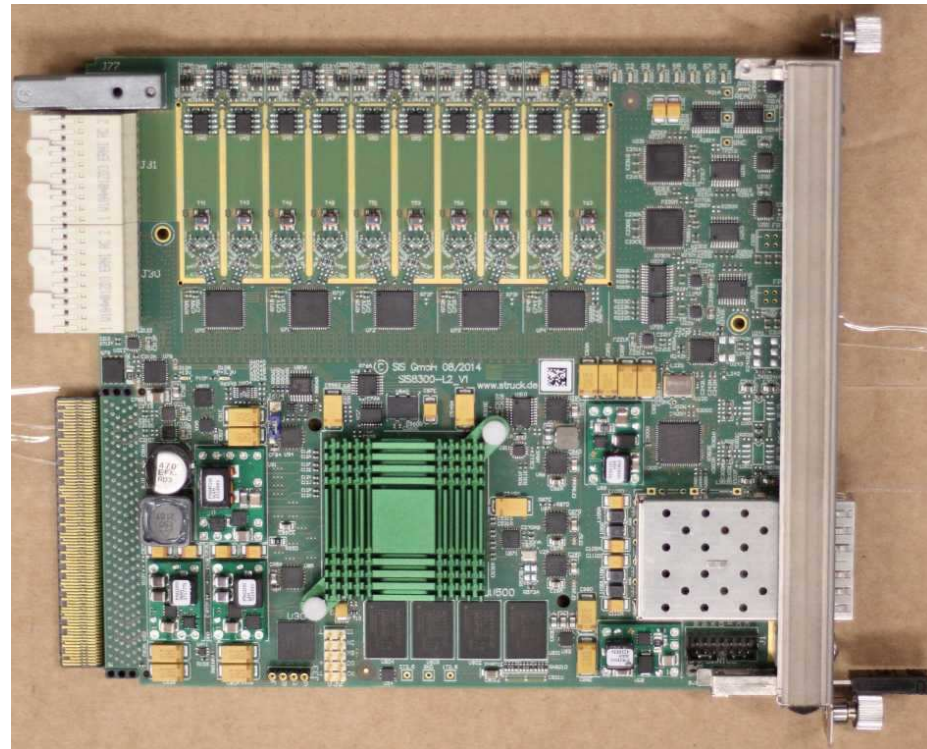


MTCA Setups for Sync – Laser Synchronization: Building Blocks

Digitizer and Processing AMC

“SIS8300L2”

- 10 x ADC
 - 16 bit
 - 125 MSPS
 - DC or AC coupled
 - Assembly variants for BW (up to 340 MHz)
- 2 x DAC
 - 16 bit
- FPGA: Virtex 6
- Zone 3: A1.0, A1.0C or A1.1CO



from Struck GmbH
(developed and improved in collaboration with DESY)

MTCA Setups for Sync – Laser Synchronization: Building Blocks

GPIO-FMC

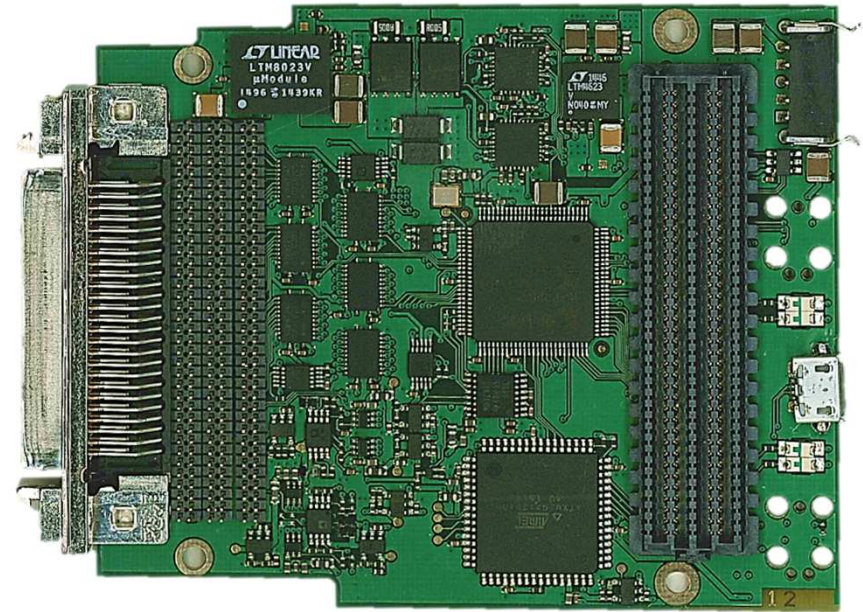
“DFMC-UNIO”

Applications

- General-Purpose IO Interfaces
- Laser and Shutter controls
- Industrial process control
- Manufacturing automation

Features

- Low-Pin-Count FMC Module
- Up to 48 general-purpose digital IO pins.
- 2 pins useable as 12-Bit DAC (0-5V, 50 mA drive)
- 2 pins useable as 12-Bit ADC
- 2 x 2 pins useable as two independent pwr ch.
- Hardware current limit: 2 x 1A with soft-start
- 4 pins useable as standard UART (12V)



MTCA integrates many components in a compact form factor

Electronic Infrastructure for Opt. Sync at FLASH (2 MLOs, 16 LSUs)



- 4 x 42 HE Racks
- 5 x VME Crates
- 6 x PLCs
- 18 x Piezo-Driver
- 6 x Vector Modulators

MicroTCA for Opt. Sync at XFEL (2 MLOs, up to 32 LSUs)



- 2 x 42 HE Racks
- 3 x MicroTCA Crates
- 1 x PLCs
- Up to 32x LDD

Firmware and High-Level Software for Synchronization Applications



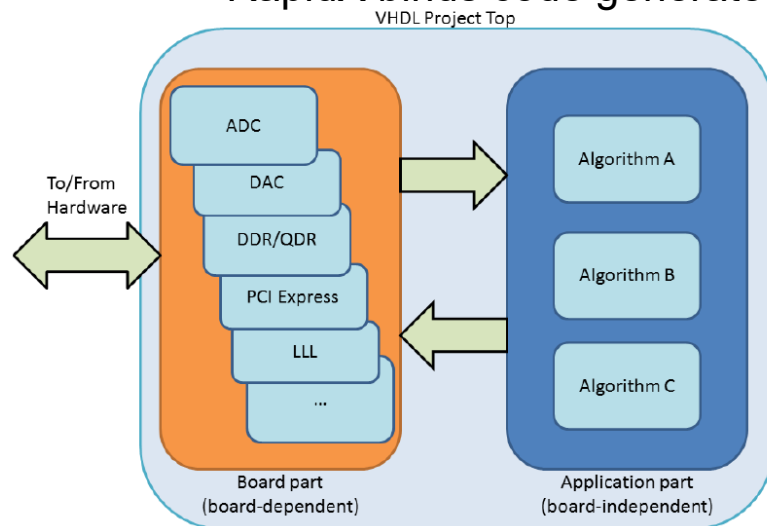
The firmware is always composed of two parts

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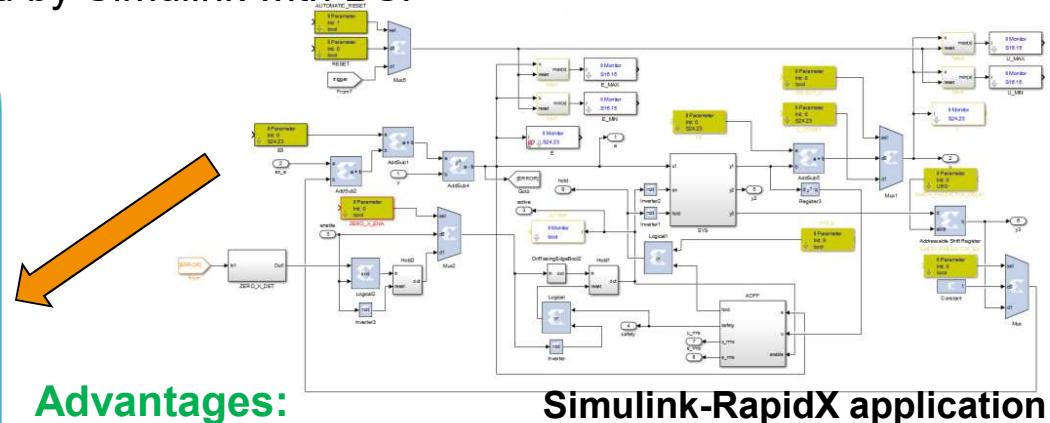
- **Board Support Package (BSP):** board dependent
 - Responsible for general PCB (AMC, FMC, RTM) functions support like clock distribution, communication (PCIe, LLL), support for on-board ADCs/DACs, memories (DDR2)
 - Prepared in VHDL

The firmware is always composed of two parts

- **Board Support Package (BSP):** board dependent
 - Responsible for general PCB (AMC, FMC, RTM) functions support like clock distribution, communication (PCIe, LLL), support for on-board ADCs/DACs, memories (DDR2)
 - Prepared in VHDL
- **Application:** board independent
 - FMC20 Laser & Link lock actuator application prepared in VHDL
 - SIS8300L2/FMC25 controller application prepared with Simulink-RapidX toolkit
 - RapidX binds code generated by Simulink with BSP



General firmware structure



Advantages:

- Reusable VHDL code - application can be reused on different hardware
- Much faster prototyping and development process

All core synchronization system software (laser and link locking servers) is based on two main libraries:

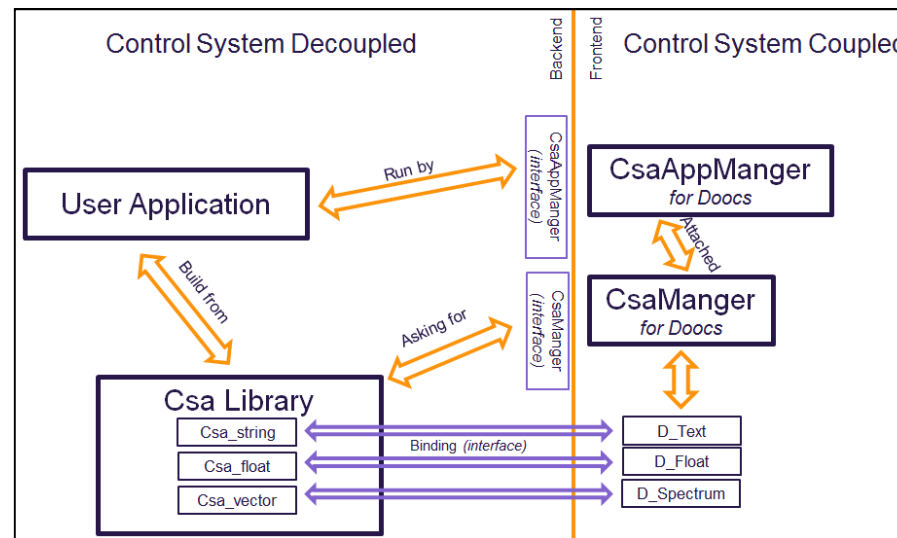
- Control System Attacher library - CsaLib
- Device Module library - DevModLib

All core synchronization system software (laser and link locking servers) is based on two main libraries:

- Control System Attacher library - CsaLib
- Device Module library - DevModLib

Control System Attacher library - CsaLib

- Decouples application core logic from control system, allowing to create independent reusable logic
- Some basic features need to be provided by control system dependent side (history, config files)



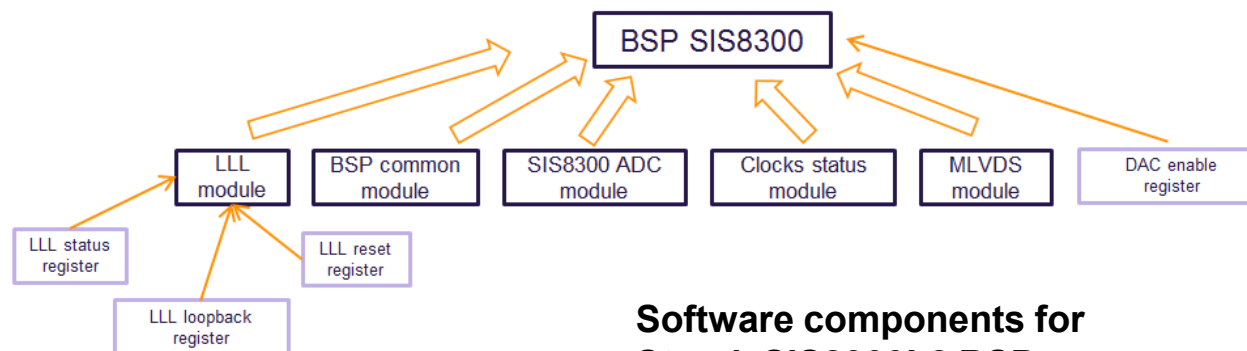
- 'Younger brother' of Control System Updater from ChimeraTK

Poster by
Martin Killenberg
TUPHA178

Device Modules library - DevModLib

- Based on CsaLib and device access library from ChimeraTK →
 - CsaLib provides data exchange with 'external world' – Control System
 - Device access (ChimeraTK) provides access to physical hardware
- Support for:
 - AMCs' BSPs - FMC20, FMC25, SIS8300, SIS8300L(2)
 - FMCs' and RTMs' BSPs – FMC-MD22, FMC-AD16, RTM-PZT4, RTM-AD84
 - Application logic - DAQ, Simulink-RapidX modules, higher level algorithm (e.g. coarse tuning)
- Modular structure (C++ Object Oriented code) allowing core reuse for fast application development
- Each module has a control system (jddd) panel

Poster by
Martin Killenberg
TUPHA178

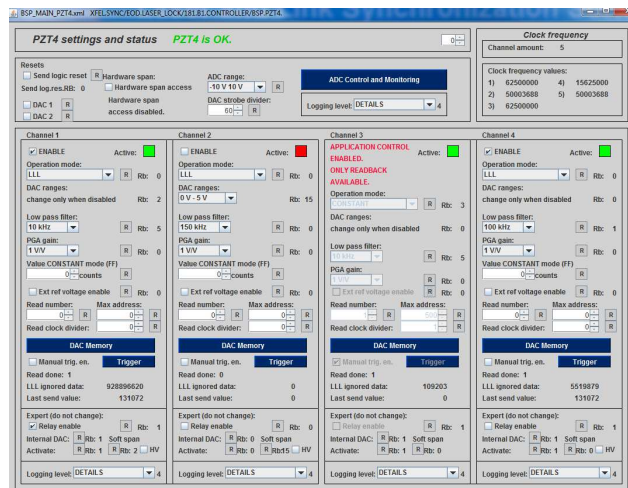


**Software components for
Struck SIS8300L2 BSP**

Laser and Link Synchronization Software

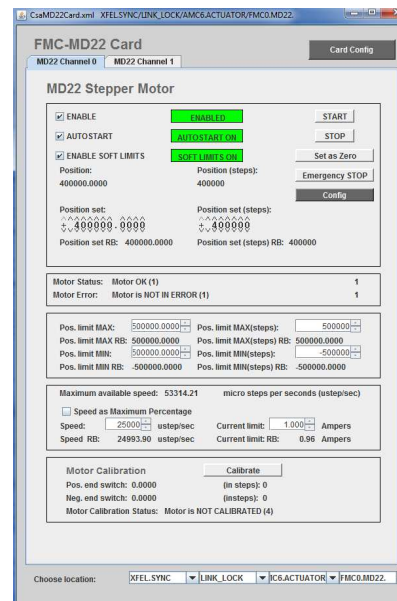
Courtesy: T. Kozak

DRTM – PZT4



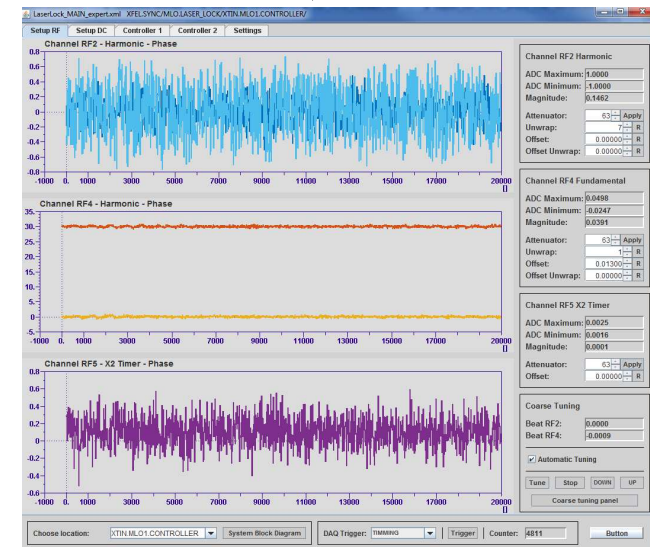
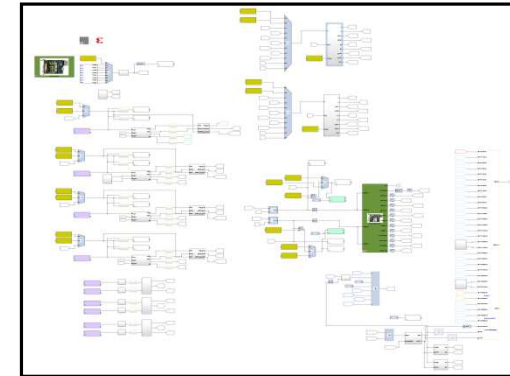
DRTM – PZT4 jddd panel

DFMC – MD22



DFMC – MD22 jddd panel

Laser Synchronization Controller



Laser synchronization jddd panel

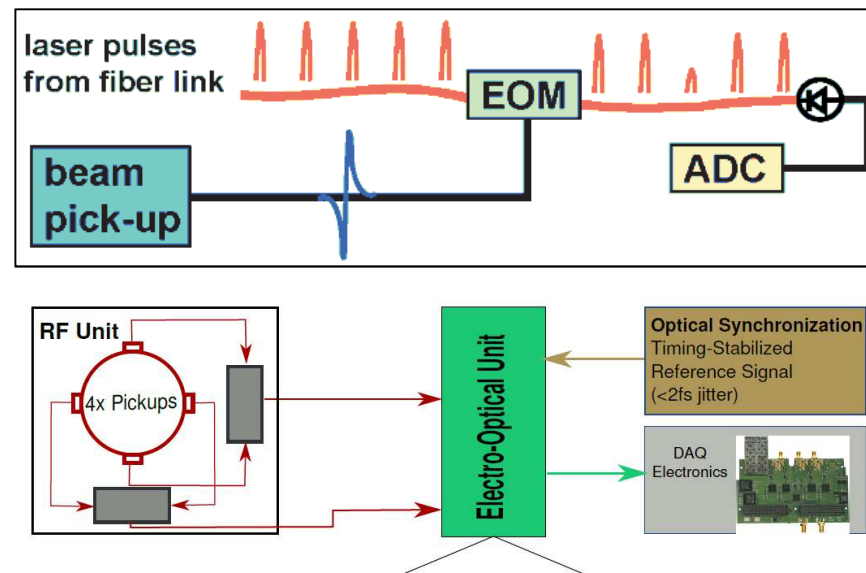


Diagnostics using MicroTCA

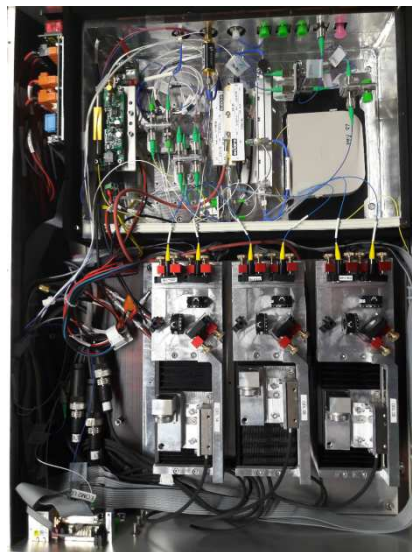
(incomplete selection)

Bunch Arrival Time Measurement (BAM)

Courtesy: M.K. Czwalinna



- > 40 GHz pickups: signals of 2 opposite pickups combined
- > Laser amplitude modulation in Mach-Zehnder Modulator depends on arrival time
- > 15 BAM stations in total (FLASH and XFEL)

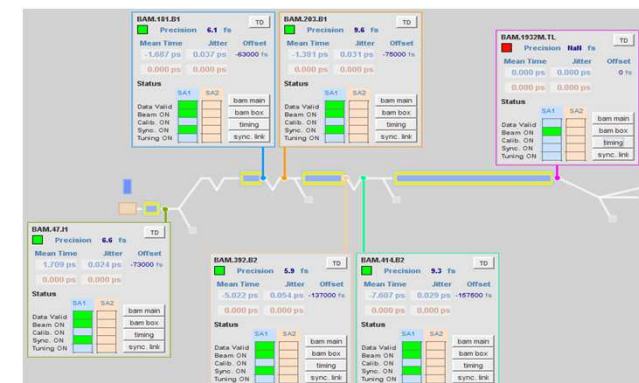
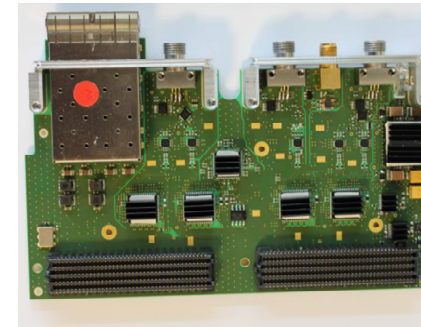


Charge (pC)	Sensitivity (fs/%)	Resolution (fs)
50	120	24.0
100	84	16.8
140	67	13.4
200	38	7.6
450	27.8	5.6

BAM – Data processing

Courtesy: M.K. Czwalinna

- Dedicated double FMC "DSBAM"
 - 3 photo diodes (Clk + 2 channels)
 - 4x ADCs for baseline and signal on each channel
 - 216 MSPS, 16 bit for each ADC
- AMC Carrier: FMC25
 - 1024 samples stored in RAM and filtered for bunch data
 - Uncalibrated arrival time sent to LLRF system via fast links for intra-train arrival time feedback (=stabilization)
- High Level Software
 - Calibration and parameter control
 - Operation relevant procedures (keeping working point)
 - Slow feedback (control system based)



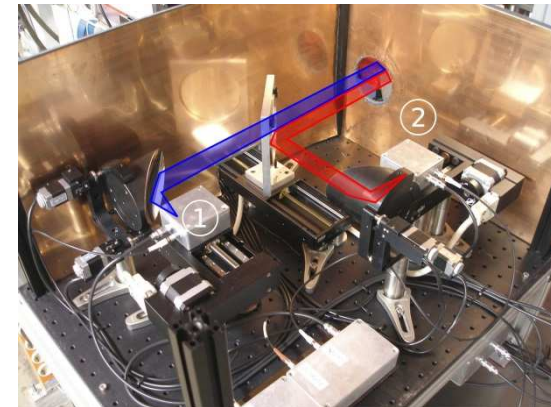
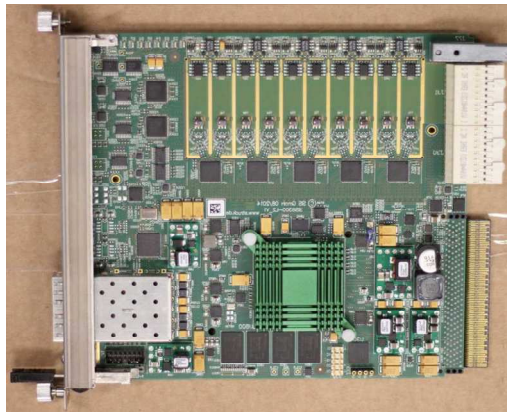
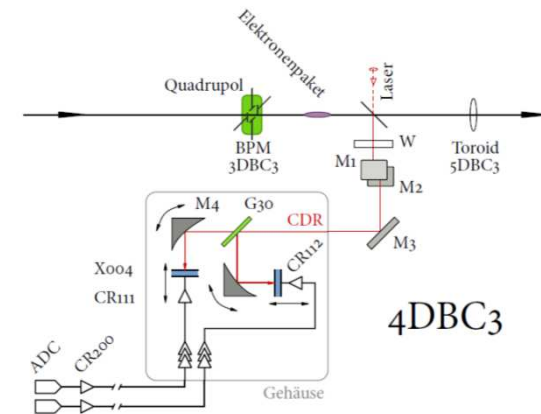
Poster by Michele Viti TUPHA125



Bunch Compression Monitor (BCM)

Courtesy: S. Wesch

- Coherent Diffraction / Transition Radiation (CDR or CTR) is guided to a pyro detector and an antenna
- Response signal is used to measure the bunch length
- Data acquisition with MTCA boards from 'Struck GmbH' ("SIS8300L2" + "SIS8900")

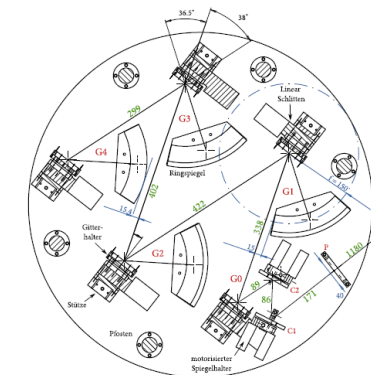
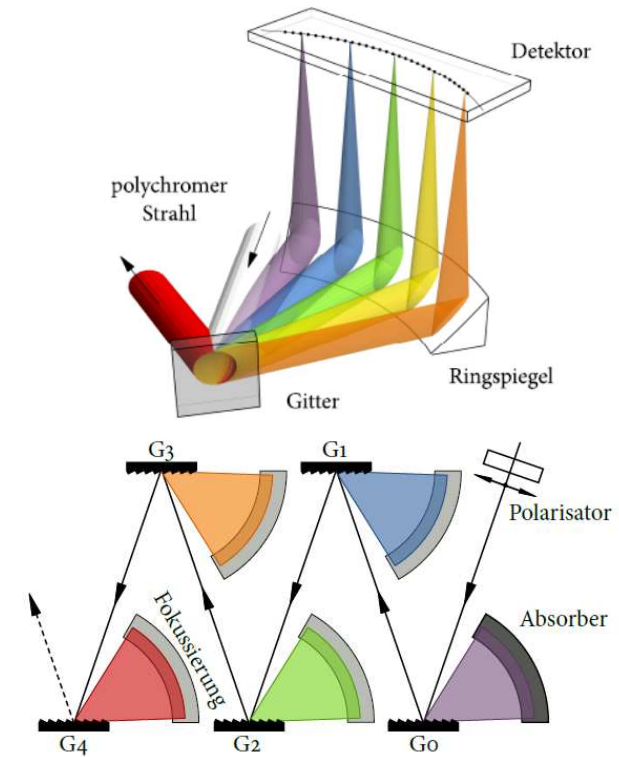
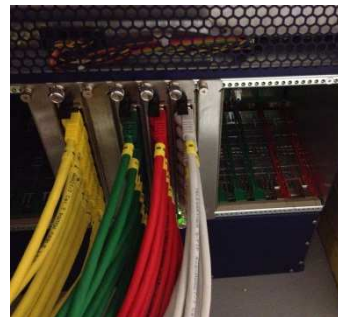
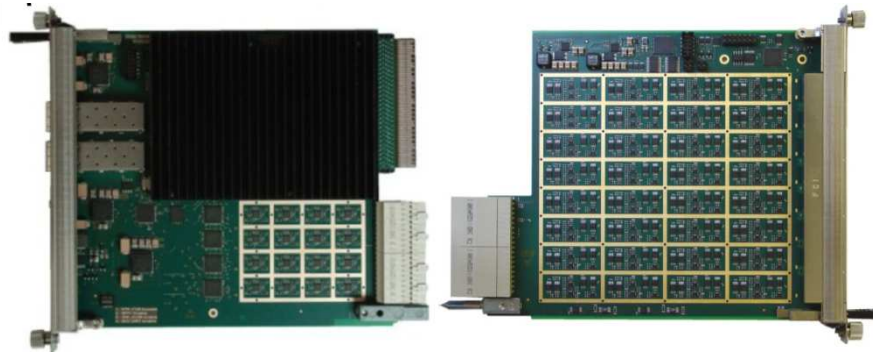


- Slow feedback (control system based)

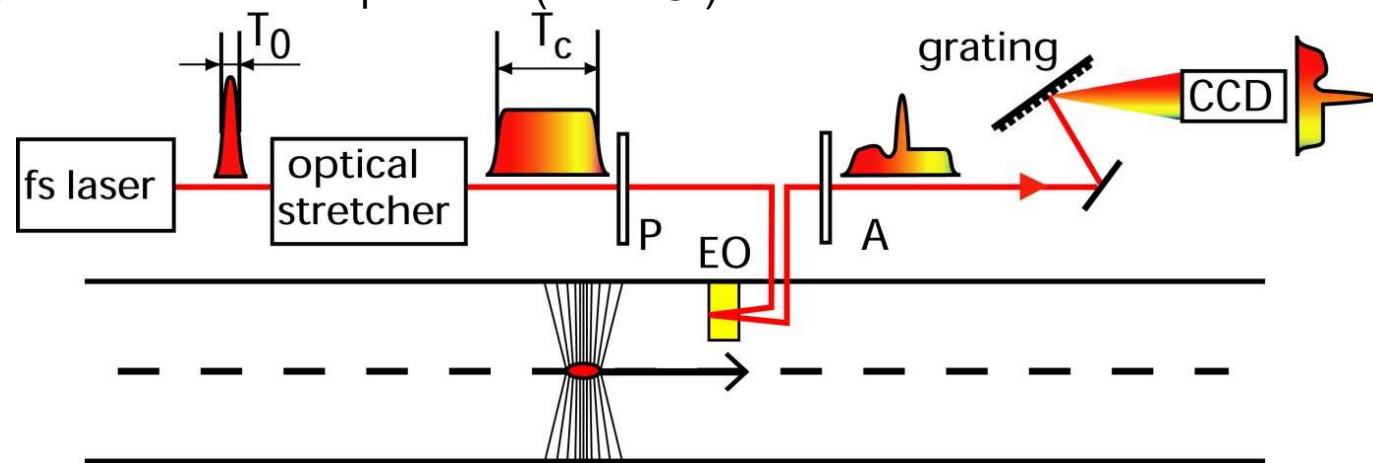
BCM (2) – Coherent Radiation Spectrometer

Courtesy: S. Wesch

- Measuring the spectrum (200 GHz – 100 THz) can reveal the longitudinal bunch shape via a sophisticated mathematical algorithm
- Needs about 120 ADC channels
- Data acquisition with MTCA boards from 'TEWS GmbH' ("TAMC532" + "TAMC532-TM")

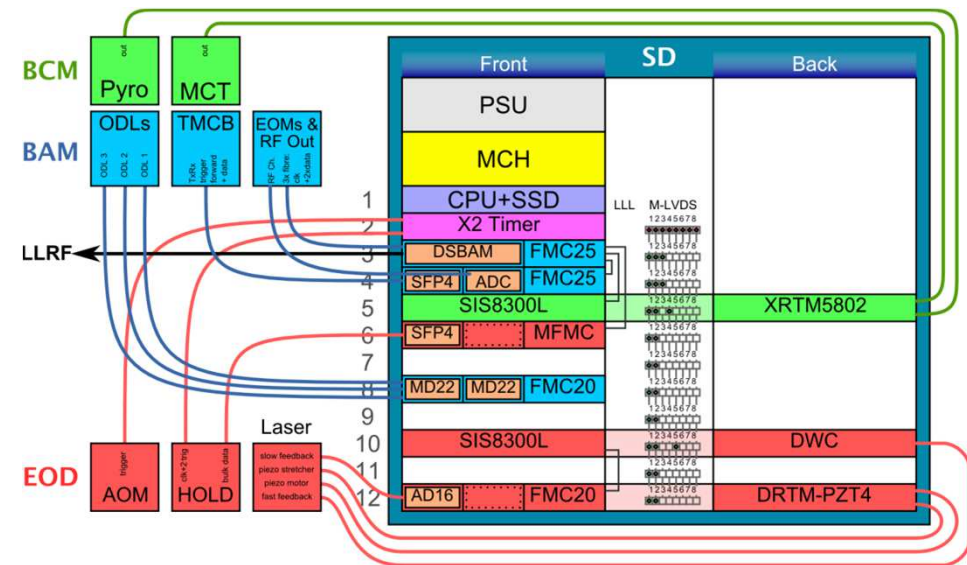
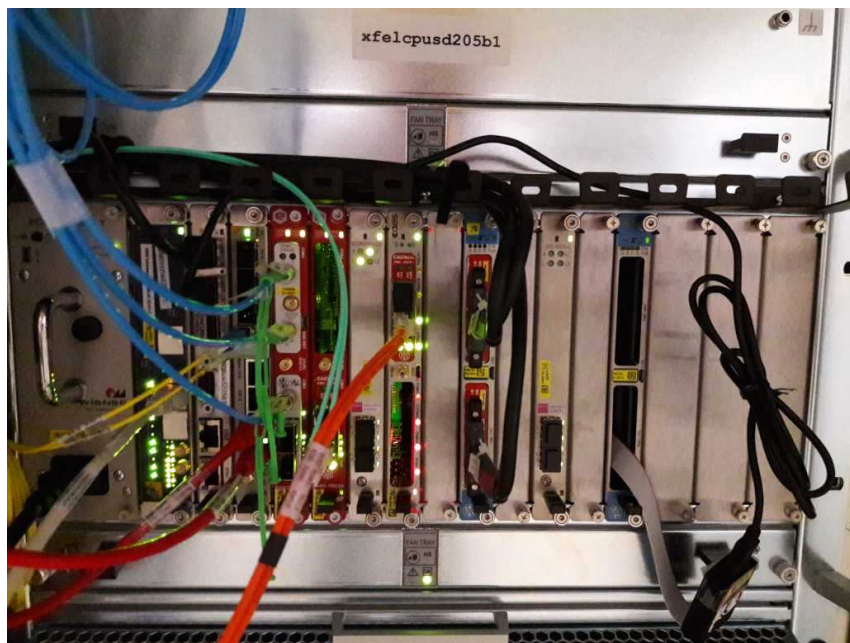


- > Electron bunch changes optical properties of EO-crystal
 - Sampling of bunch shape with consecutive pulses
 - Or measuring bunch shape with one stretched pulse (Electro-Optical Spectral Decoding)
- > Needs precise laser synchronization and fast image acquisition
 - Detector chip and dedicated carrier (-> “HOLD”, collaboration with KIT & PSI)
- > Fast (optical) communication to MTCA crate for real-time data in control system
 - SFP4 with FMC-Carrier from ‘AIES sp. z o.o.’ (“MFMC”)



BAM, BCM, EOD at one station (XFEL)

- At some diagnostic stations of the the European XFEL BAM, BCM, and EOD are combined in one MTCA crate



Courtesy: C. Gerth

> Cavity BPMs – highest resolution

- 101 at XFEL and about 20 at FLASH(2)
- Required single bunch resolution 1 μm for 0.1-1 nC and within ± 0.5 mm at 10 mm beam pipe -> achieved sub- μm resolution
- Readout electronics is in-kind contribution from PSI: Modular BPM Unit (MBU)
- Up to 4 MBUs connected to one MicroTCA DAMC2 board (interface to control system)

Cavity BPM



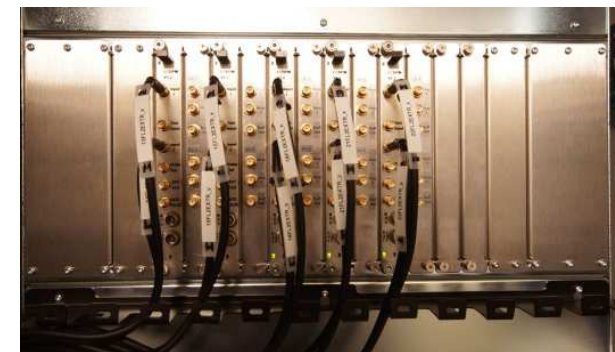
> Button & Stripline BPMs – low charge BPMs (LCBPM)

- > 300 at XFEL and currently about 20 at FLASH(2)
- Resolution: 50 μm (single), 10 μm (rms avg train) within ± 10 mm at 40.5 mm beam pipe
- MBUs at XFEL and MicroTCA LCBPM electronics at FLASH (will replace all electronics at FLASH)
- RF Front-end on LCBPM RTM / AMC: Struck “SIS8300L2”

LCBPM
RTM

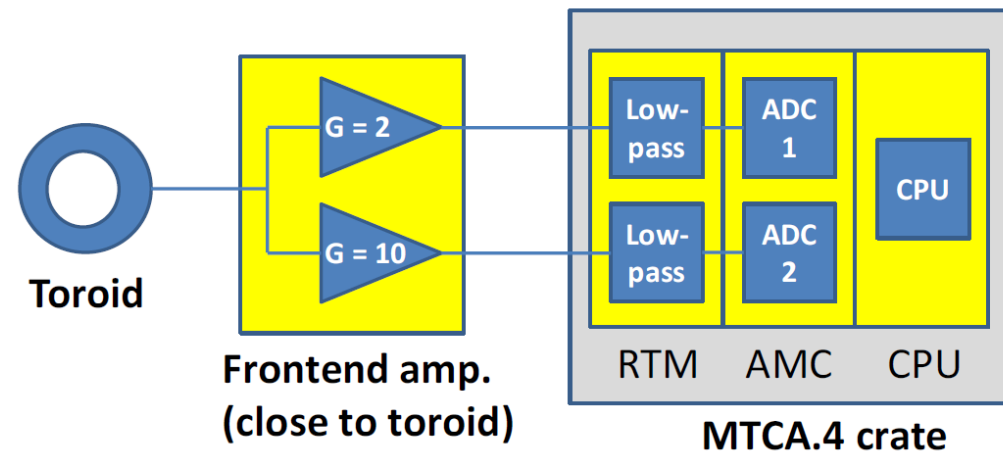
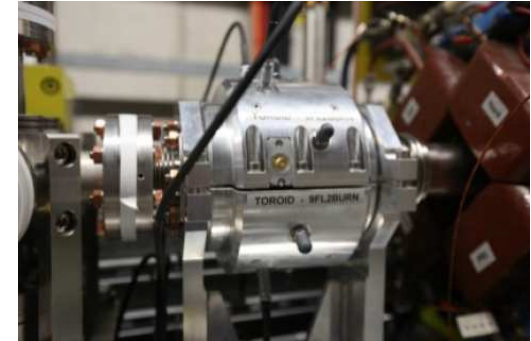


Crate rear side



Charge Measurement – Toroid Readout

- Machine Protection System needs to cut the bunch train if charge is lost
- 36 Toroids at XFEL, about 20 at FLASH(2)
- Achieved resolution ~ 0.2 pC at 2 nC dynamic range
- Dedicated conditioning “Toroid RTM” + “SIS8300L2”



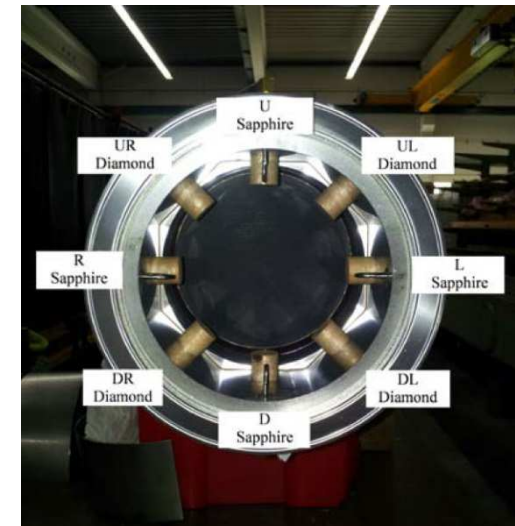
Courtesy: T. Lensch, M. Werner

Beam Loss Monitors (BLM) / Beam Halo Monitors (BHM)

- Based on scintillator or fused silica (rod or fiber)
- Signal detection with photo multiplier tubes (~500 V)
- >300 BLMs at XFEL + about 60 at FLASH2 with new MicroTCA electronics for readout and low latency interface to MPS
- 8 channel readout “BLM RTM” + “DAMC2”



Courtesy: T. Lensch, N. Baboi

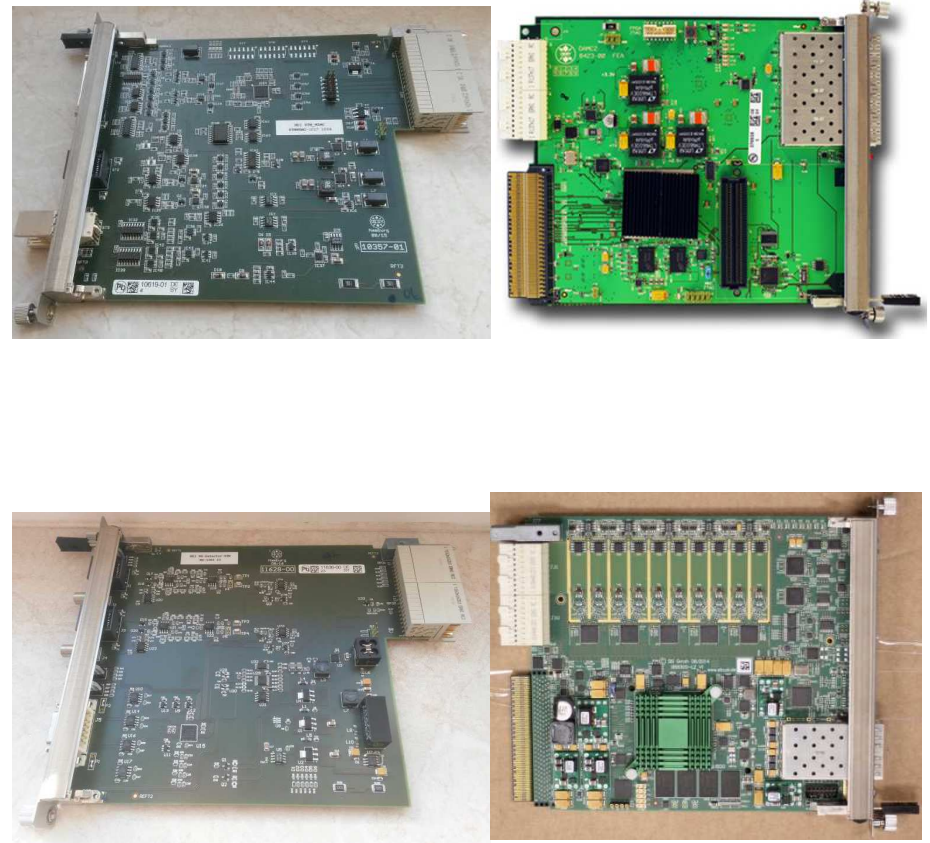


Dump loss monitors:
BHM: 8 sensors are read
Out in one MTCA slot

Wire Scanners

- 1) Wire moves through beam and scatters electrons
 - Speed is 1m/s meaning about 100 bunches are crossed → MPS must be deactivated
 - Dedicated RTM for motor control and position readout (0.5 μm resolution of wire position)
 - “WS-MC RTM” connected to “DAMC2” AMC

- 2) Signal detection with photo multiplier tubes
 - Dedicated RTM for readout of two PMTs
 - “WS-Detector RTM” + “SIS8300L2”



Courtesy: T. Lensch

Further Diagnostics using MTCA but not Covered in this Talk

- > Transverse Deflecting Structure (TDS)
- > Chicane BPM for energy measurement (EBPM & BPMS)
- > Dark Current Monitor (DCM)
- > Ionization Chambers
- > Synchrotron Radiation Monitor (SRM)
- > ...

Thank you for your attention!

> Synchronization Team

- C. Sydlo, J. Mueller, T. Lamb, E. Felber, F. Zummack, M. Titberidze, T. Kozak, M. Felber

> With help from

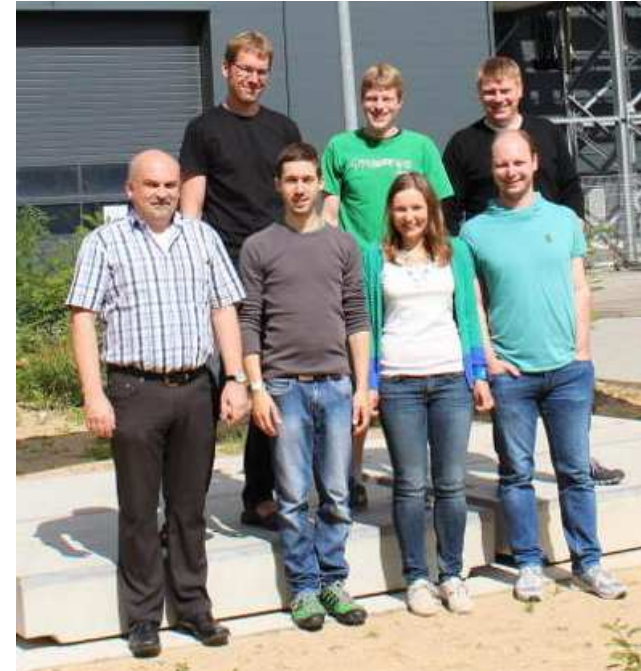
- M. Fenner, K. Przygoda, R. Wedel, M. Schaefer, B. Szczepanski, D. Kuehn, S. Chystiakov, P. Prędkie, S. Ruzin, M. Hoffmann, and many more....

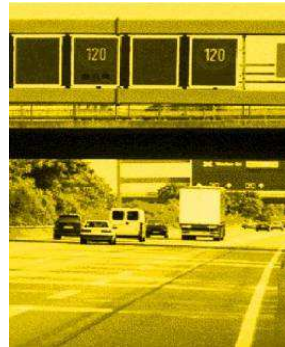
> Special Diagnostics

- C. Gerth, M.K. Czwalinna, B. Steffen, J. Roeber M. Viti, (S. Wesch)

> Standard Diagnostics

- N. Baboi, T. Lensch, M. Werner, B. Lorbeer, S. Vilcins, F. Schmidt-Foehre, D. Lipka, P. Smirnov, T. Wamsat, and many more...





Scaleability of MTCA...

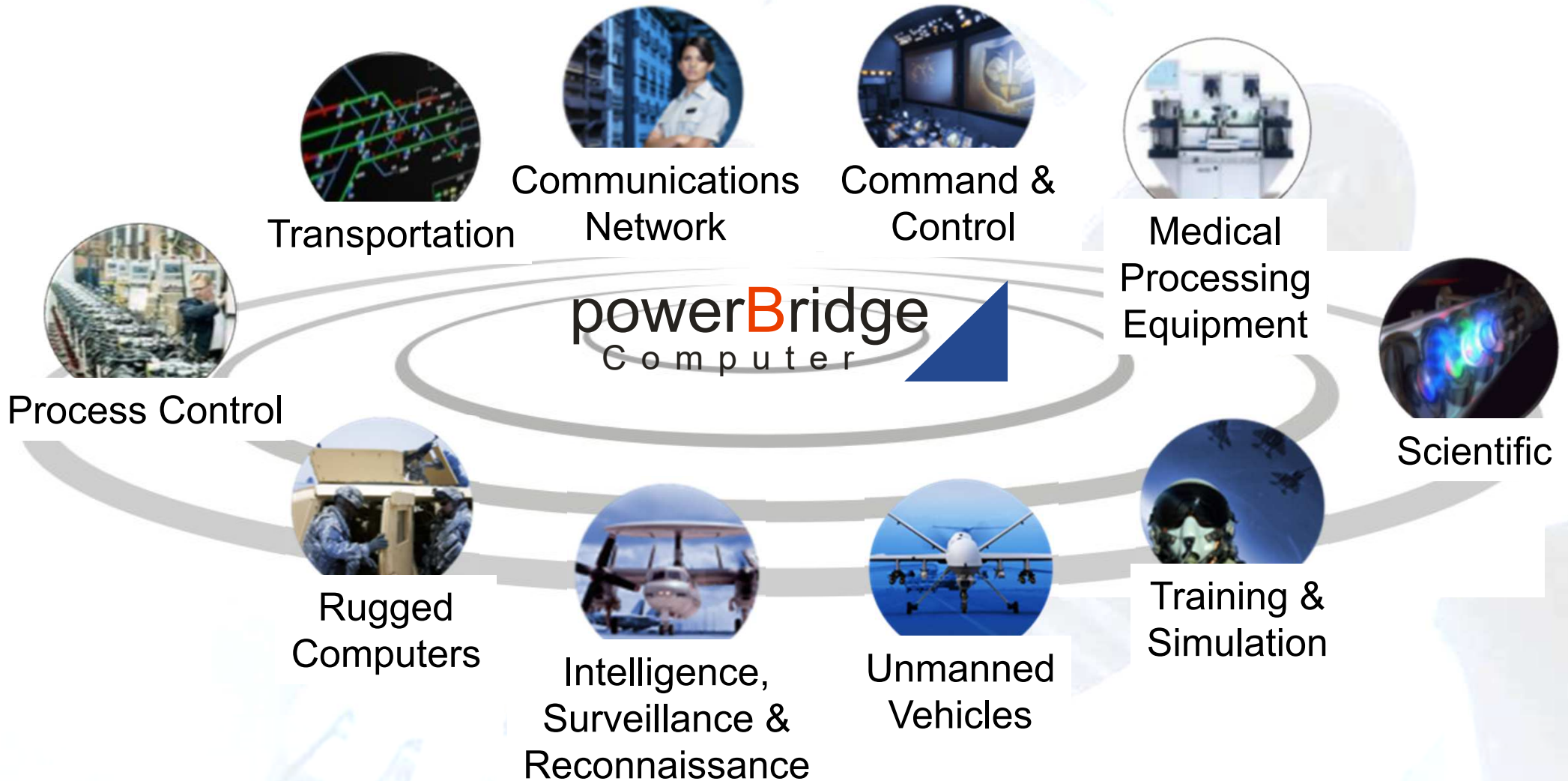
ICALEPS 2017
Workshop 9
User Experience in MTCA

- Over 20 years in the market
- Privately owned
- Over 25 years VME experience
- Own Lab and integration facilities
- powerBridge has delivered over 27.000 VME boards and 5.500 systems
- Active PICMG member
- ISO 9001:2008 and 14001:2009 approved





*Medical. Transportation.
Communication. Automation.*

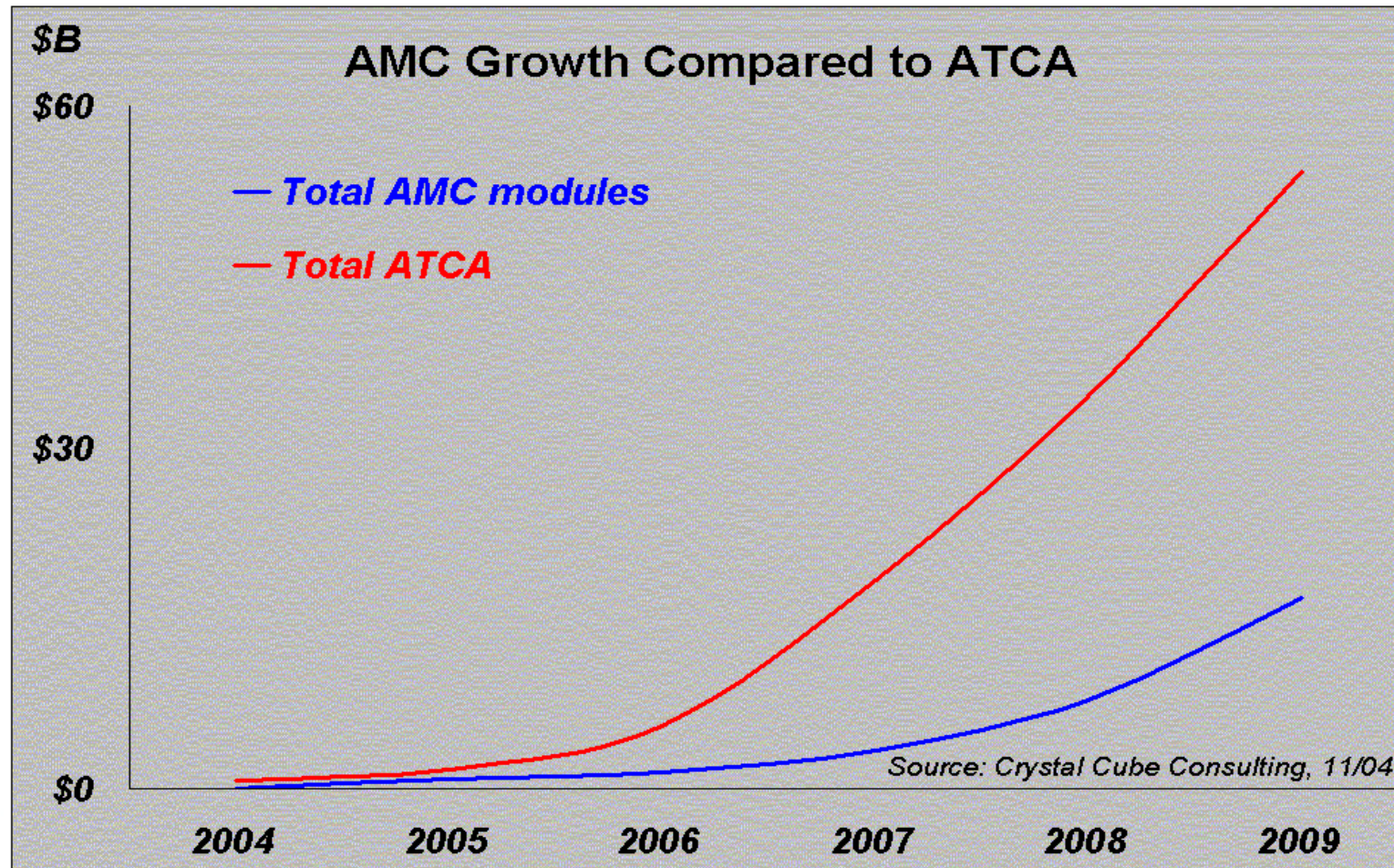


powerBridge has the right solution ... From building blocks to systems

2004. Outlook.

Prognosis of Open industry standards.

“More telecom equipment manufacturers are taking advantage of the cost savings that they and their customers can achieve from using open industry standards such as AdvancedTCA and SA Forum,” said Lee Doyle, Group Vice President, Network Infrastructure, International Data Corp., a leading industry analyst firm. “ATCA enables telecom equipment manufacturers to get to market faster so that service providers can benefit from open standards much sooner than was possible using the traditional building block approach to communications computing platform integration.”



Markets

Our diverse membership allows PICMG to develop compelling specifications in multiple markets. PICMG technologies are widely used in a broad swath of industries including industrial automation, military/aerospace, transportation, communications, test/measurement, physics/research, energy, medical, and more!

	COM Express	AdvancedTCA	CompactPCI	CompactPCI Serial	HPM	MicroTCA / AMC	SHB
Industrial Automation	X		X	X		X	X
Gaming	X						
Telecommunications	X	X			X	X	
Aerospace	X		X	X	X	X	
Defense	X	X	X	X	X	X	X
Railway	X		X	X	X	X	
Energy	X		X	X	X	X	X
Medical	X		X	X	X	X	
Test / Measurement	X	X	X	X	X	X	
Physics		X			X	X	X
Drones / UAV	X		X	X	X	X	



MTCA. Ecosystem. Chassis and AMC.

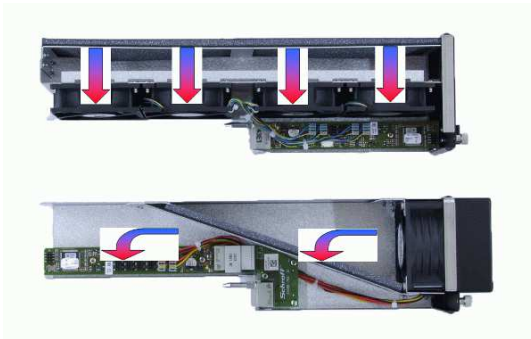


RackPak/M4-2.

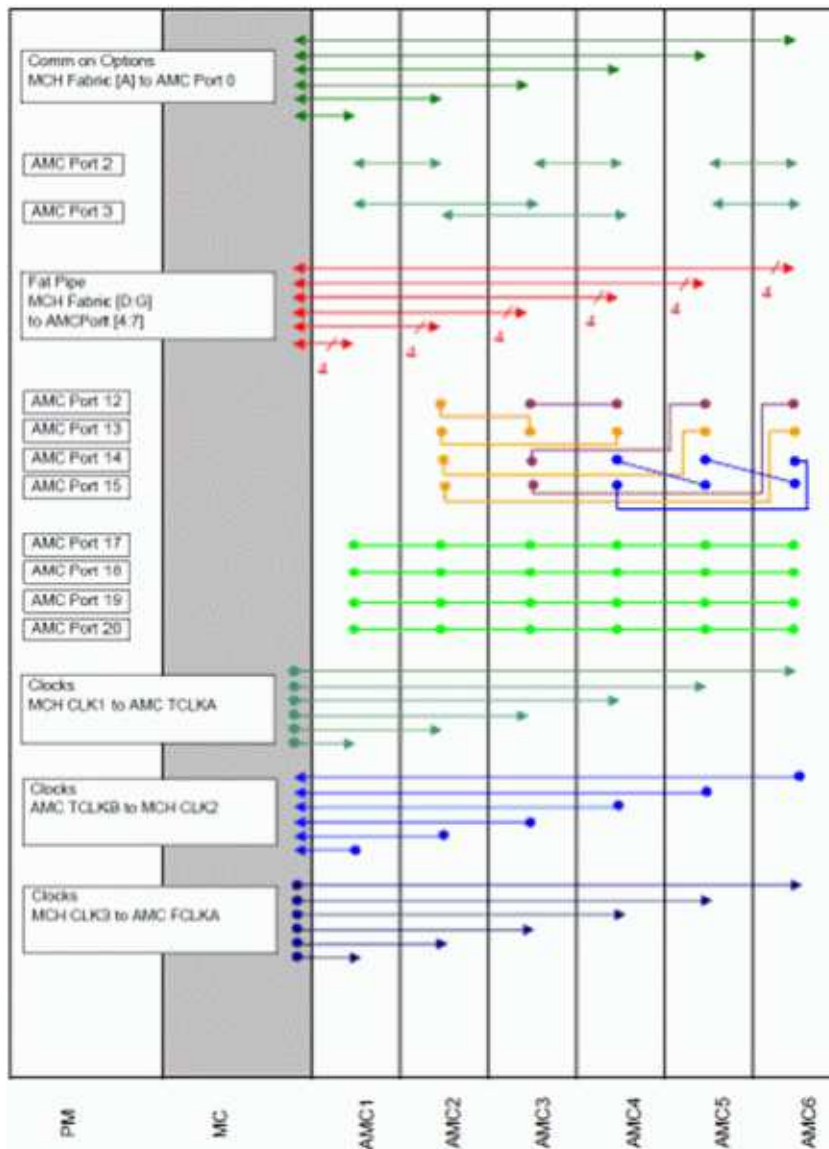
Small, dense MTCA.4.



- 2U 19" MTCA.4 crate, PICMG MTCA.4 R1.0
- 6 double mid-size AMC slots
- 4 double mid-size μ RTM slots
- Double full-size MCH slot
- Double full-size Power module slot
- Exchangeable cooling unit with front to left or right to left air flow
- Dust filter exchangeable



■ Backplane Topology

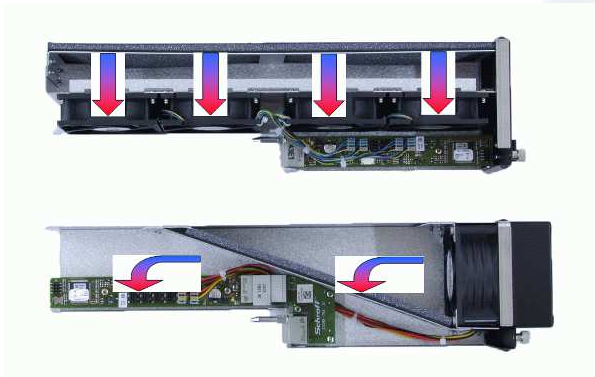
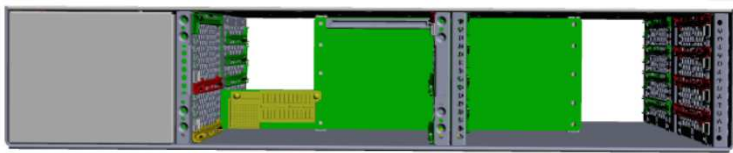
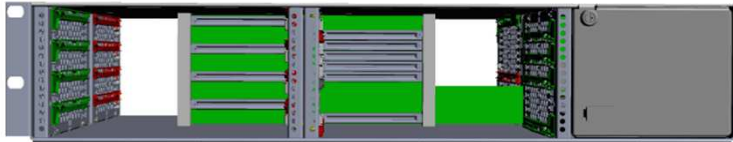


- Single Ethernet Link (Port 0) to every AMC
- Dedicated SATA Links on Ports 2&3
- PCIe x4 support on Ports 4-7
- Point to Point connections on Ports 12-15
- Daisy Chain on Ports 17-20
- TCLKA, TCLKB and FCLKA Clocks

RackPak/M5-1. *Smart, dense MTCA.4.*



Joint Development together with N.A.T. and Pentair

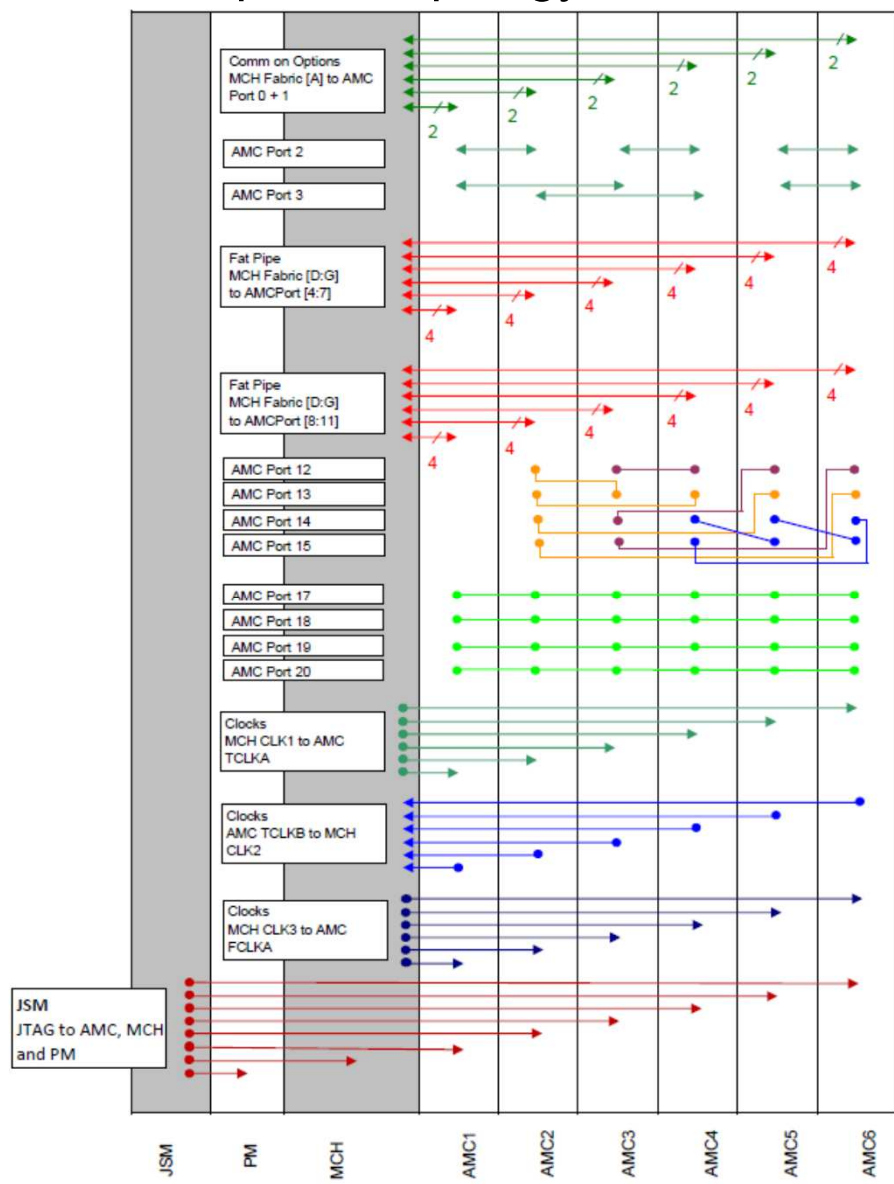


Available now!

- 2U 19" MTCA.4 crate, PICMG MTCA.4 R1.0
- 5 double mid-size AMC slots
- 1 double full-size AMC slot
- 5 double mid-size μ RTM slots
- Double full-size MCH slot with μ RTM Slot
- Double full-size Power module slot
- Exchangeable cooling unit with front to left or right to left air flow
- Dust filter exchangeable
- Order codes:
RackPak/M5-1R (right-to-left cooling)
RackPak/M5-1RS (right-to-left cooling)
or
RackPak/M5-1F (front-to-left cooling)

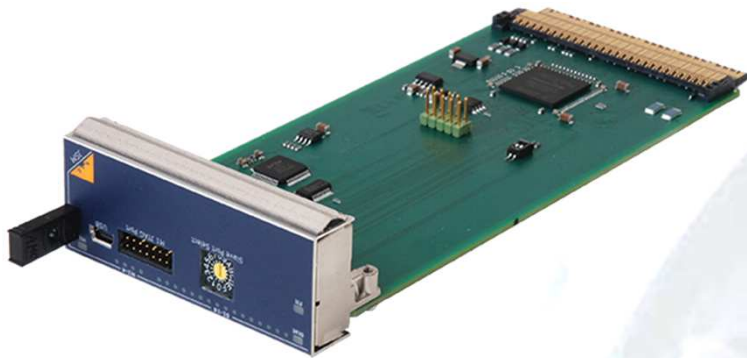


■ Backplane Topology



- **Dual** Ethernet Link (Port 0+1) to every AMC
- Dedicated SATA Links on Ports 2&3
- **PCIe x8** support on Ports 4-11
- Point to Point connections on Ports 12-15
- Daisy Chain on Ports 17-20
- TCLKA, TCLKB and FCLKA Clocks
- **JTAG Switch Module (JSM)** Slot
- Optional White Rabbit Support

JTAG adapter. *Ease of programming.*

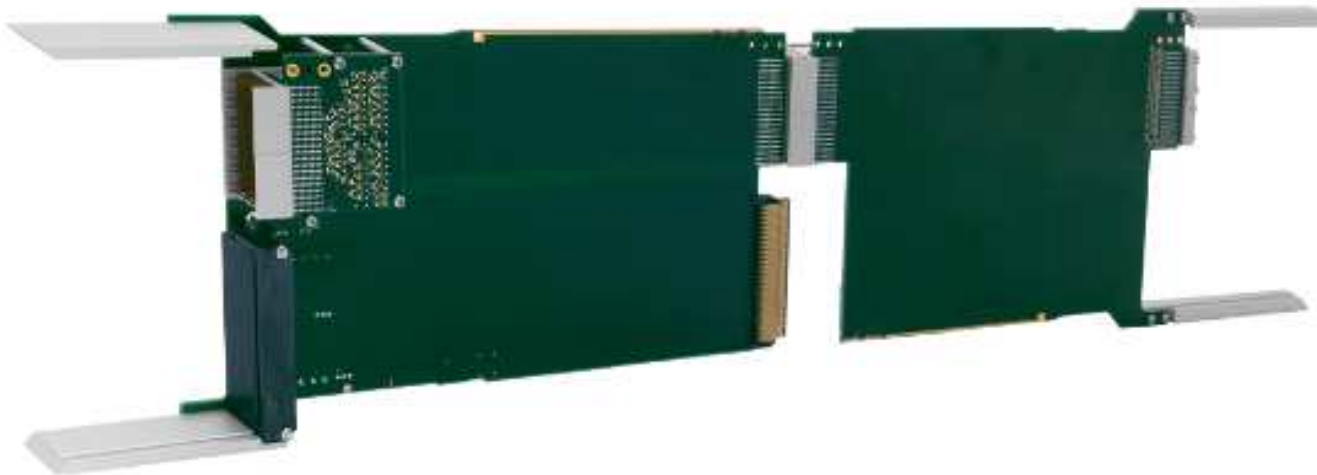


- JTAG Switch Module (JSM) in single mid/full size AMC form factor with onboard FPGA to adapt to any JSM pin-out at AMC type backplane connector (default N.A.T. pin out, others on request)
- JTAG download via MCH through Ethernet
- JTAG programming connector at front panel
- Automatic arbitration between JTAG Masters
- Target selection through JTAG information
- Overrule of automatic operation and dedicated selection of JTAG target by front panel elements
- Multiple JSM pinout configurations via FPGA

AMC extender. *Ease of development.*

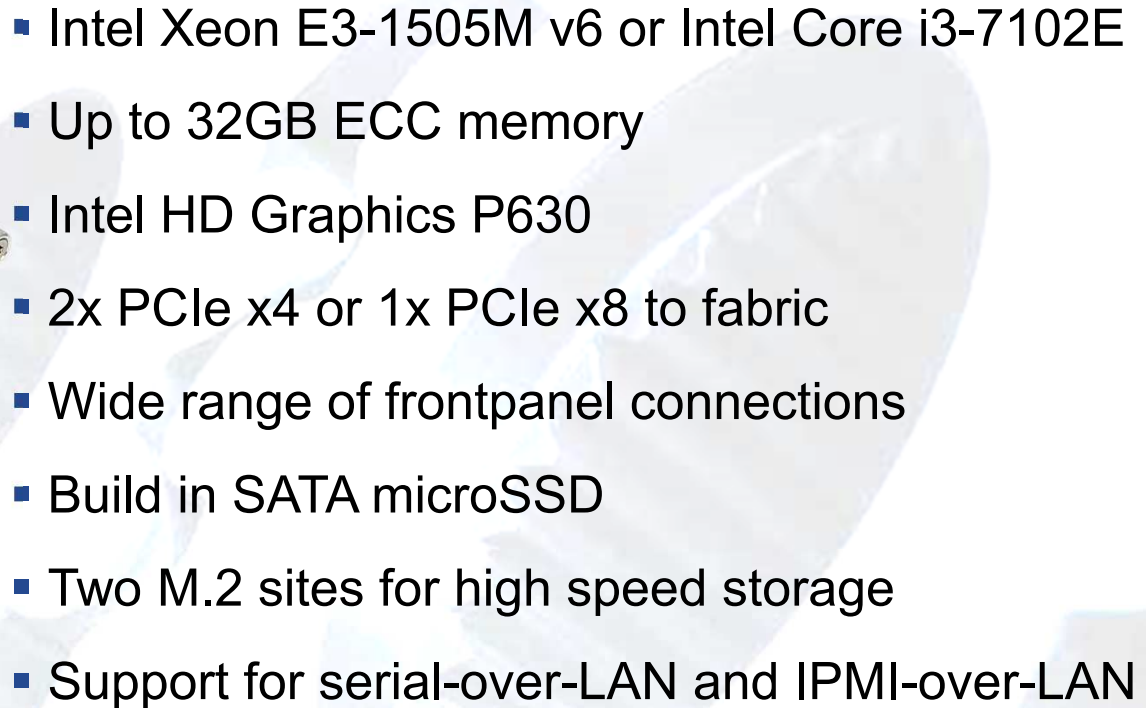
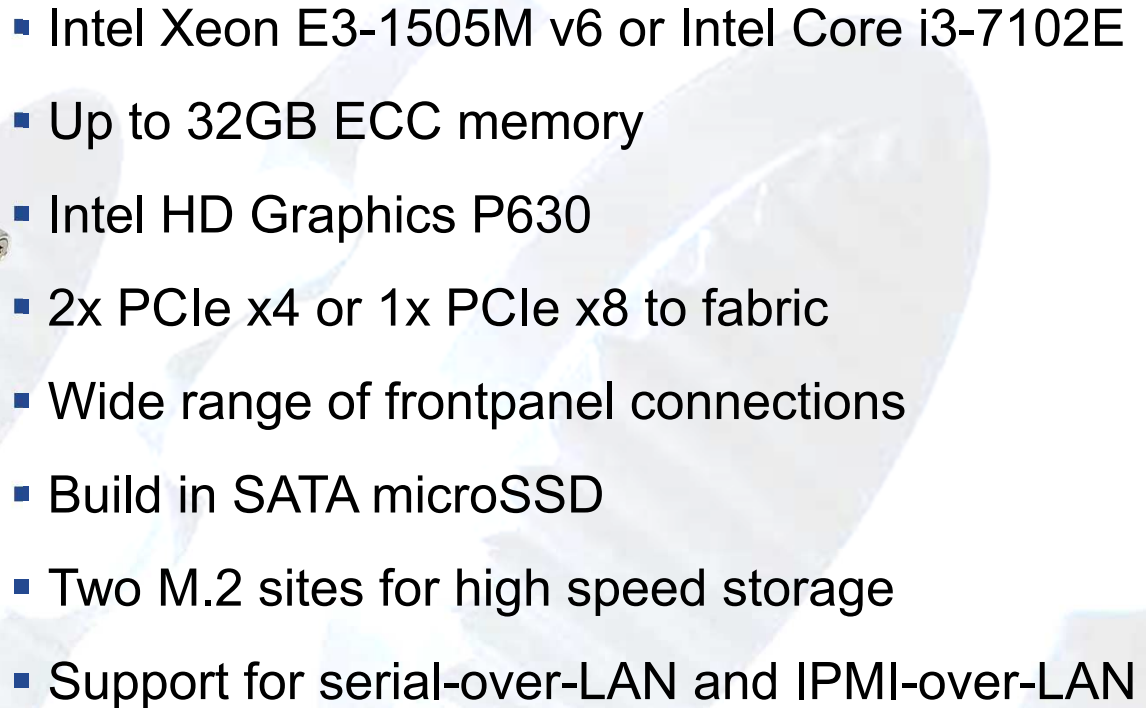


- AMC extender are passive extenders
- Front AMC extender module
- Rear μ RTM extender module
- Enables access to AMC modules and signals
- Supports all fabric connectors
- available with additional power supply for development

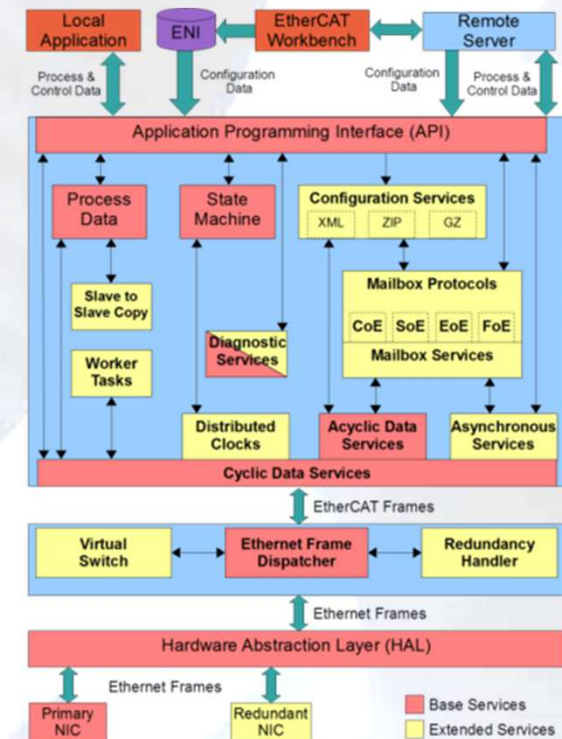


6x/msd.
computing power.

- Intel Xeon E3-1505M v6 or Intel Core i3-7102E
- up to 32GB ECC memory
- Intel HD Graphics P630
- 1x PCIe x4 or 1x PCIe x8 to fabric
- Wide range of frontpanel connections
- Build in SATA microSSD
- Two M.2 sites for high speed storage
- Support for serial-over-LAN and IPMI-over-LAN



- MTCA System can act as EtherCAT Master
 - Configuration and management of EtherCAT networks
 - Cyclic exchange of process data
 - Sophisticated API common to all implementations as interface between the application and the EtherCAT master stack
 - Mailbox based communication with:
 - CAN application protocol over EtherCAT (CoE)
 - Ethernet over EtherCAT (EoE)
 - File over EtherCAT (FoE)
 - Servo Drive over EtherCAT (SoE)
 - Built-in detailed diagnostics and profiling functions
 - Written in ANSI-C designed with high performance, small resource usage and scalability in mind
 - The core components are operating system (OS) and CPU architecture independent
 - Adaption to many prevalent (real-time) operating systems available from stock
 - EtherCAT Master Class A according to ETG.1500

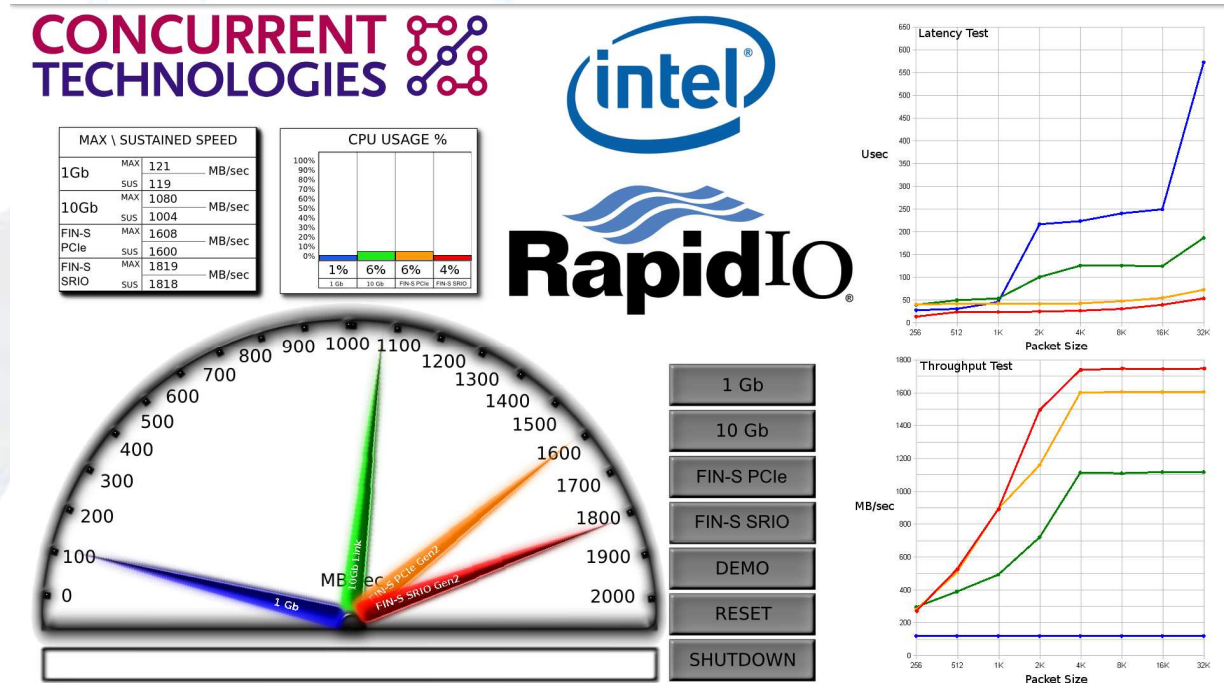


EtherCAT Slave modules

- EPS-6000 EtherCAT bus coupler
- EPS-1132 digital input 32 channel with SPI interface (sinking type)
- EPS-2032 digital output 32 channel with SPI interface (sourcing type)
- EPS-2308 relay output 8 channel and 8 digital input with SPI interface
- EPS-3032 analogue input 32 channel ($\pm 10V$) with SPI interface
- EPS-3216 analogue input 16 channel (0~20mA) with SPI interface
- EPS-3504 RTD input thermal 4 channel with SPI interface
- EPS-4008 analogue output 8 channel with SPI interface
- EPS-7002 pulse output motion controller 2 channel with SPI interface



FIN-S. High Speed Data Transfer.



Fabric Interconnect Networking Software FIN-S

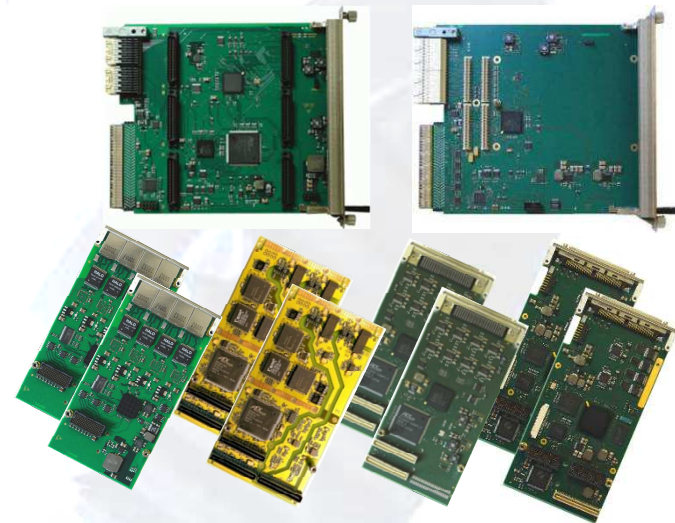
- IP based socket communication
- Direct Inter-Process Communication Interface
- Support for Linux, Windows, VxWorks
- VPX, VXS, AMC
- High Performance, Low latency comms
- PCI Express, Serial Rapid-IO, 10GbE

MTCA Toolbox. *Starterkits and components.*

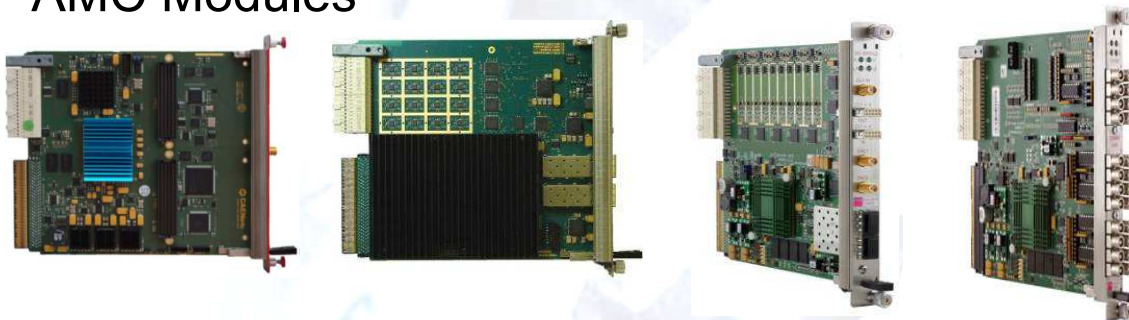
- MTCA.4 Starter Kits, including MCH, CPU & PM



- Carrier + Mezzanines (IP, PMC, XMC, FMC)



- AMC Modules



- Spare parts, like filler modules, adapter cables, program and debug tools, test adapter

- SW & FW Support including BSP, source code drivers, sample applications, FPGA framework

- Components quality
- System construction
- Quality of manufacturing and assembly instructions
- Functional tests, final test, safety test
- Quality of test instructions
- Device History Record

Installationshinweise VP717.pdf - Adobe Acrobat

ge Fenster Hilfe

Seite entnehmen Werkzeuge Kommentar Freige

2014-12-02 Mtg- Installationshinweise VP717.doc

powerBridge
Computer

VX838/011-74
Montage- und Installationshinweise Rev.1.2
Materialnummer: 83220224
Dokumentnummer: 54.1155.157.02

1. Vorbereitungen

- Die Seriennummern von CPU Board und TR Modul in das Prüfprotokoll übertragen.
- Die Firmware/Bios Revision (Label Board-Rückseite) mit Angaben auf dem Karton vergleichen.
- Im PP die Abruf- Bestell- Nr. und alle Angaben in der Artikeltable anpassen.
- Im Begleitschein ebenfalls die Auftragsnummer anpassen. Dateinamen unten im Begleitschein anpassen. Begleitschein für Kartonbeilage drucken und bereitlegen.
- Eine EU Konformitätserklärung 2011/65/EU für jedes Lieferlos beilegen. Datum anpassen!
- Ein COC VP717xx von pBC für jedes einzelne Produkt erstellen. SN, AU und Datum anpassen!
- Auf dem CPU-Karton das Label "Caution! Lithium Metal Battery" entfernen.
- Auf der Karton Stirnseite vom links ein Typenschild „VP717/083-43-K1“ anbringen

VP717/083-43-K1
SN: M
powerBridge
Computer

CONCURRENT
VP717/083-43-K1
SN: M170454
Modul: 717/083-43-K1
Board: 717/083-43-K1
Rev: 1.0
Date: 2014-12-02

i) Auf der Karton Stirnseite unten mittig ein Label 45,5mm x 16,9mm mit der Beschriftung „With ME Firmware Update, B541Axxx, BIOS V3.xx“ anbringen.

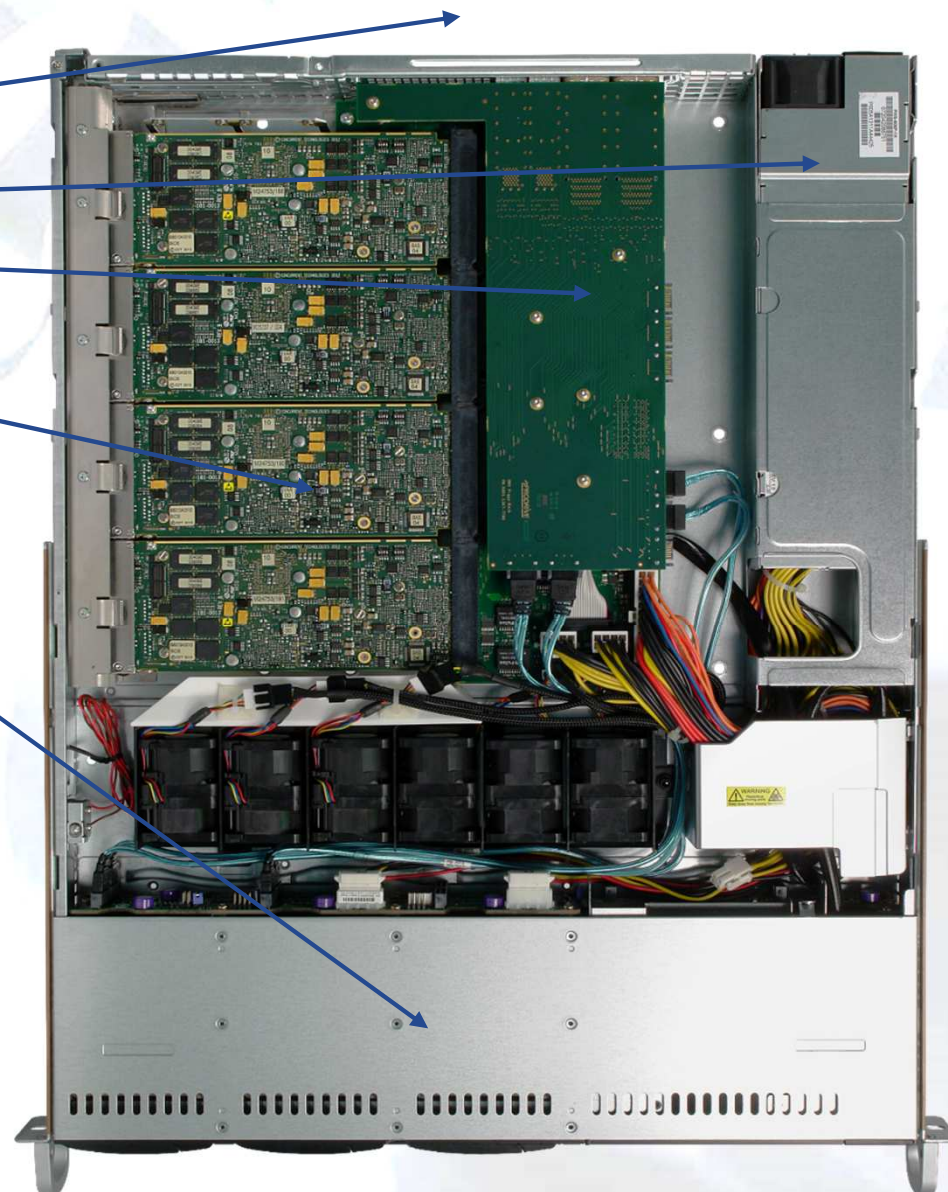
With ME Firmware Update
B541A3L1



- Manufacturing quality is determined by staff training and experience, work place quality and infrastructure, regular inspections of measuring devices,
- ESD protection and checking electrical fields,
- employee quality awareness and motivation
- Assembly and test instructions quality
- Managing of exact reproducibility



- Data Center Compute and Network
- 3rd Party 19" 1U rack
 - 10G Ethernet connectivity
 - PSU
 - Fabric switch board
- 4 AMC Module sites
 - Fitted with any combination of CPU/GPU
- Up to 8 spaces for 2.5" removable drives
 - 2 SATA connections to each Module
- Open HPC (high performance compute) Platform
 - Blade server concept based upon AMC



MTCA. HPC Traffic control.

High Density. Maximum Flexibility.

- COTS components
- Small system footprint
- Fully redundancy for system!
- No NRE or additional development costs



- NATIVE C-2 Chassis
- NAT-MCH Systemcontroller, LAN infrastructure 1/10GbE
- 12 CPU cards per system: NAMC-2041 Quad-Core QorIQ P2014, IEEE-754 Double precision, e500mc Core ->MPC603 compliant, Encryption and secure boot

- Application-Ready-Platform
- Latest DSP technology
- Latest audio and video codecs supported
 - Includes HD audio and video codecs (OPUS, SILK, WebRTC,...)
- Legacy interfaces supported (E1/T1/J1)

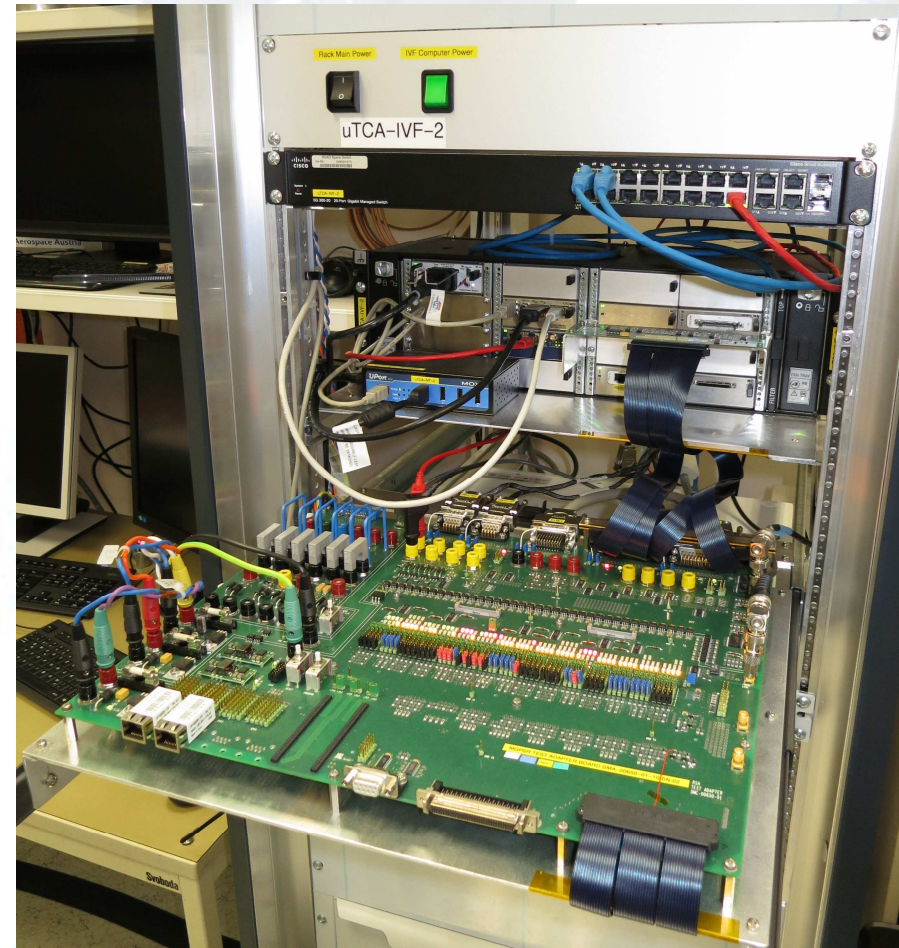


- Former Test-Equipment concept and architecture
 - standard PC or IPC systems and Microsoft Windows only
 - Legacy hardware based Device-Under-Test (DUT) interface implementation (e.g. SpaceWire, UART, Mil1553, proprietary Multi-Wire Communication-link, ...)
 - Legacy hardware driven SW functions to operate these interfaces, no universal approach
- Consequence and Short-Comings
 - High effort to handle and maintain multiple Interface-Device Vendors, their Libraries and drivers
 - High development effort to realize an appropriate Test-Equipment capable of meeting DUT Verification requirements
 - Limitations in performance and reliability

MTCA. SAT Testbed.

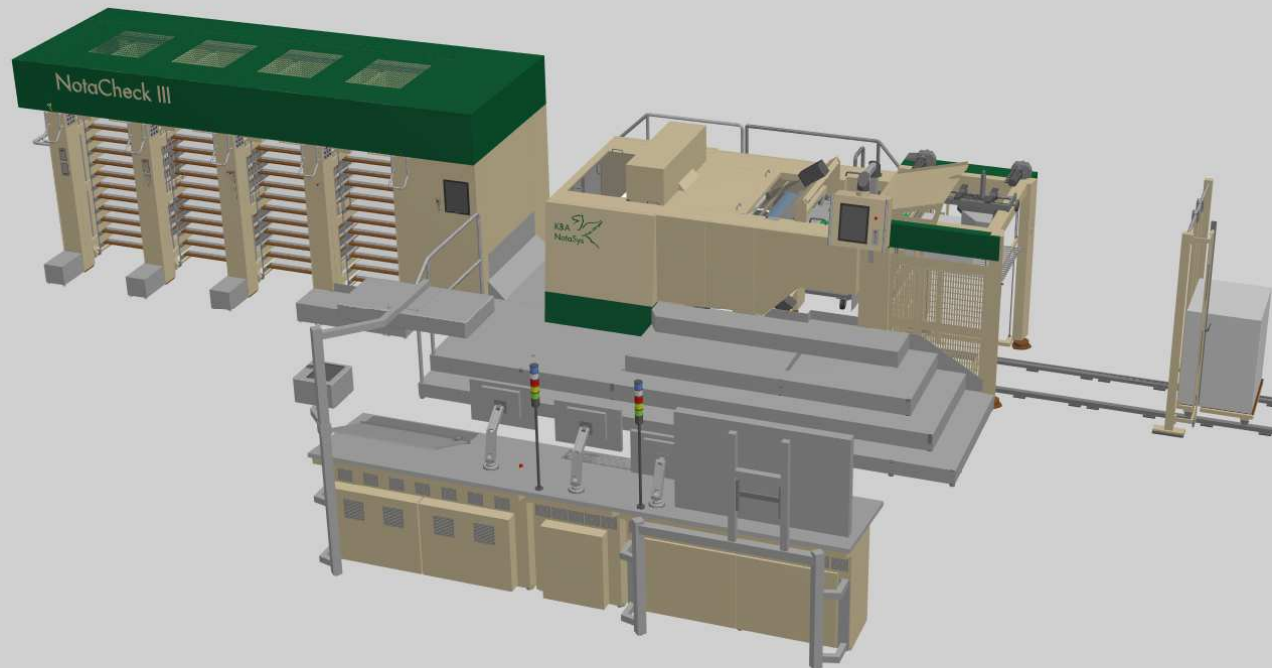
High Density. Maximum Flexibility.

- Decision for MTCA due to:
 - Open industry standard
 - Matured Ecosystem
 - Fast datapaths available (SATA 3, PCIe (Gen.2) and GbE)
 - Scaleable architecture
 - Independant PCIe Root complexes
 - Legacy IO could be re-used
 - SW support (Windows 7 and VxWorks)



MTCA. Banknote Inspection. *High Density. High Speed.*

- Inspection and sorting
- Inline inspection of all sheets
- 12.000 sheets per hour



MTCA. Banknote Inspection. *High Density. High Speed.*

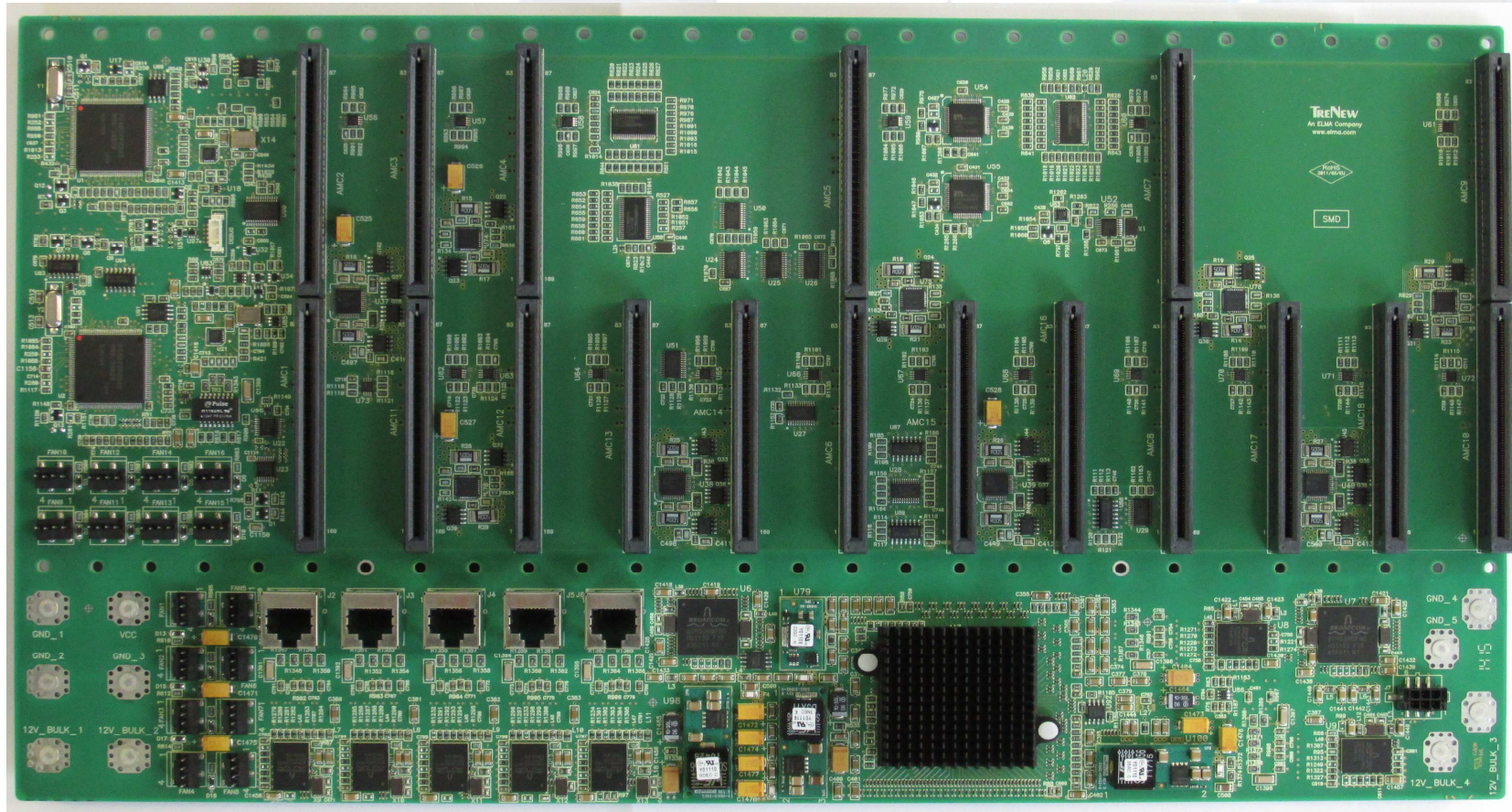
- Up to 18 slots, active backplane
- High bandwidth, PCIe links



Only 1 board per inspection pipeline

MTCA. Banknote Inspection. *High Density. High Speed.*

- Custom backplane with integrated MCHx2, PCIe switch and GIGE switch
- Heterogeneous computing approach
- Up to 7 CPUs
- Split configuration: 2 virtual systems!!!
- Custom port configurations between AMC slots (local connections)



test and measurement

- testbeds for avionics
- high speed visual inspection
- Non destructive Testing (NDT)
- spectral analysis
- Hardware-in-the-loop (HIL)

communication

- PABX
- gateways
- 5G/LTE basestation (CPRI, OBSAI) Testsystems
- conferencing platforms
- Software defined radio (SDR)

medical has adopted MTCA for

- high speed data acquisition
- image processing

others

- Broadcast
- homeland security and defence

And many, many more....

- It is an open, matured, robust Standard
- It is extremely scaleable
- The Ecosystem is intact
- Big variety of different processor boards
 - X86, Freescale, ARM
 - GPGPU, FPGA, DSP
- Big variety of I/O-functions available
 - Either as dedicated AMC module
 - Or
 - Via carrier cards (IP, PMC, XMC, FMC)
- Variety of chassis
 - From small to big
- Highspeed interfaces
 - Up to PCIe x8, Gen.3
 - Ethernet 1,10,40GbE
 - SRIO Gen.2
 - 2018 upcoming SRIO Gen.3 and PCIe Gen.4



- Powerbridge is a member of the MicroTCA Technology Lab
- Hub for research, development and testing
- Advanced measurements and compliancy testing
- MicroTCA Trainings
- Loaner pool of pre-configured MicroTCA systems
- Custom MicroTCA development
- Licensing of DESY designs





The network for your success.





Let's discuss your requirements and test our performance!

- Thomas Holzapfel
- Email: thomas.holzapfel@powerbridge.de
- Tel: +49-5139-9980-21

powerBridge Computer Vertriebs GmbH,
Ehlbeek 15a, 30938 Burgwedel, Germany
<http://www.powerbridge.de>

MicroTCA in Real Life



Let Your **Application** benefit

www.nateurope.com

MicroTCA.4

Configuration and Maintenance



- Motivation
- Configuration Tools
 - Command Line Interface
 - Java-App
 - Web interface
- Examples of Configurations
 - Ethernet and PCIexpress Configurations
 - Emergency Configuration
- Maintenance Tools
 - Analysis locally: LEDs
 - Analysis remotely: inventory, current, revision
 - Firmware update

About N.A.T.

Network and Automation Technology



- Founded in 1990, privately owned
- Hard- and Software design and manufacturing
- Focus on **innovation in communication**
- international and worldwide operations
- Headquarters

Konrad-Zuse-Platz 9

53227 Bonn

Germany

- Presenter:
 - Thomas Holzapfel, thomas.holzapfel@powerbridge.de
 - on behalf of Vollrath Dirksen, vollrath@nateurope.com



About N.A.T.

Network and Automation Technology



Innovation in Communication

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The brain of your MTCA.4 system

Higher bandwidth for Physics: the new NAT MCH PHYS80

Key features

- x16 PCIe Gen3 uplink at front panel
- 128Gbps link to local CPU/IOCT complex
- special low latency and low jitter CLK module
- fully user accessible quad core Intel (R) Core i7
- new RTM for LPRF backplane
- complete product line

Let Your **Application** benefit



The brain of your MTCA system [read more ...](#)



**Accelerate
Media
Processing**
[read more ...](#)



**The brain of
your MTCA
system**
[read more ...](#)



**The QorIQ-
Family**
[read more ...](#)

Board Level Products



System Solutions



Upcoming Events

- ▶ **MTCA Workshop at DESY**
Dec 9th-10th, 2015, Hamburg
- ▶ **IBIC 2015**
Sept. 13-17th, Melbourne,
Australia
- ▶ **Mobile World Congress**
Mar 2nd-5th, 2015, booth 6B40

Latest News

- ▶ **New product NAT-JSM**
Open JTAG switch module in
AMC form factor
- ▶ **NAT-MCH firmware v2.17
and NATview v2.18**
New versions of firmware and
GUI available
- ▶ **AMC module NANC-ODSP**
New Media Acceleration Engine
based on 8x OCT2224M DSPs
- ▶ **MicroTCA Concept**
Version IV now available

N.A.T. at and in DESY XFEL



MicroTCA.4

Configuration and Maintenance



- About N.A.T.
- Comparison of Standards
- Configuration Tools
 - Command Line Interface
 - NATView
 - Web interface
- Examples of Configurations
 - Ethernet and PCIexpress Configurations
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 - LEDs
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AMC

Pluggable in ATCA and MTCA Shelf



- The basic idea of MTCA is to have a shelf that contains just AMC modules
- Backplane directly accepts AMC modules
- AMCs are interchangeable between ATCA and MTCA
- The infrastructure of a ATCA Carrier was adapted into the MTCA shelf (power, management, switching)
- No rear I/O
- power input and all outputs to the front



Comparison of Standards

Differences in latest specs



	VPX	ATCA	MTCA
Common size	3U, 6U	2U, 3U, 12U	1U, 2U, 3U, 5U, 9U
Backplane	passive, switched	passive, switched	passive, switched
topologies	<i>single star, dual star (1/2 switch), full mesh, daisy-chain, ring</i>	<i>dual star, dual-dual star, full meshed</i>	<i>single star, dual star</i>
profiles	yes	no	no
Voltages	MP: 3.3V PP: 3.3V, 5.0V, 12.0V optional: ±3.0V, ±12.0V	MP: 3.3V PP: 48.0V	MP: 3.3V PP: 12.0V
Slot budget (PP)	115W@5V, 384W@12V 768W@48V	400W@48V	80W@12V
Pins per slot	728 (6U), 168 (3U)	234/414	170 (AMC) 260(AMC+RTM)
Link speed (Gbaud)	1.25, 2.5, 5, 6.25, 8.0	1.25, 2.5, 5, 6.25, 8.0	1.25, 2.5, 5, 6.25, 8.0
Link width	x1, x2, x4, x8	x1, x2, x4, x8	x1, x2, x4, x8
Fabrics	GbE, XAUI, PCIe, SRIO	GbE, XAUI , PCIe, SRIO	GbE, XAUI, PCIe, SRIO
Markets	Mil, Aerospace	Mil, Aerospace, core Net	all

Open Modular Computing Specifications
PICMG is the leading specification development
organization in the embedded computer market.



Markets

Our diverse membership allows PICMG to develop compelling specifications in multiple markets. PICMG technologies are widely used in a broad swath of industries including industrial automation, military/aerospace, transportation, communications, test/measurement, physics/research, energy, medical, and more!

	COM Express	AdvancedTCA	CompactPCI	CompactPCI Serial	HPM	MicroTCA / AMC	SHB
Industrial Automation	X		X	X		X	X
Gaming	X						
Telecommunications	X	X			X	X	
Aerospace	X		X	X	X	X	
Defense	X	X	X	X	X	X	X
Railway	X		X	X	X	X	
Energy	X		X	X	X	X	X
Medical	X		X	X	X	X	
Test / Measurement	X	X	X	X	X	X	
Physics		X			X	X	X
Drones / UAV	X		X	X	X	X	

Comparison of Standards Results



- Results:
 - VPX targeting at one vertical market
 - ➔ limited volumes
 - ➔ industry develops for this market only
 - ATCA has its strength in bandwidth
 - ➔ limited use cases due to cost/function
- ➔ MTCA combines strengths and flexibility



- simple backplane architecture
 - ✓ reduces costs and risks, is re-useable in future
- all signals at same signal level (MLVDS)
 - ✓ no electrical clash
- switched connections
 - ✓ no blocking transfer
 - ✓ type of backplane connection depends on kind of switch
- all slots managed and controlled
 - ✓ detection of incompatibilities and faults
 - ✓ health management and fault isolation
 - ✓ hot-swap and hot-plug



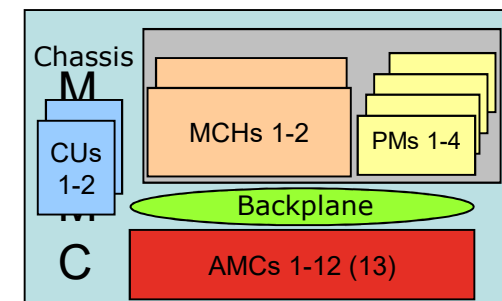
- all data transfer are
 - independent
 - simultaneous
 - bidirectional
- data connections determined by one switch card:
 - **base/common options** fabric: GbE
 - **storage** fabric: SATA
 - **fat pipe** fabric: PCIe or XAUI or SRIO
 - **extended fat pipe** fabric: XAUI or SRIO

MicroTCA Architecture

Advanced Mezzanine Cards (AMCs)



- AMC eco system
 - single and multi-core CPUs (Intel, Freescale, ARM, etc.)
 - single and multi-core GPP, NPU, GPGPU
 - communication line interfaces (E1/T1, SDH, ATM, 3G/4G/5G)
 - antenna interfaces (CPRI, OBSAI)
 - FPGAs (Xilinx, Intel-Altera, etc.)
 - DSPs (TI, Freescale, Octasic, etc.)
 - analogue and digital IO (ADCs, DACs, TTLs, etc)
 - industrial busses (EtherCAT, Profibus, CANbus etc.)
 - SSD and HDD storage
 - Carrier Boards (FMC, XMC, PMC, IP)
 - Cross-Link (cPCI, PCIe, PCI)
 - Reference MMC, EMMC, AMC, RTM system
 - Timing Modules



MicroTCA.4

Configuration and Maintenance



- About N.A.T.
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Safari Ablage Bearbeiten Darstellung Verlauf Lesezeichen Entwickler Fenster Hilfe 192.168.178.67 Fr. 12:55 Vollrath Dirksen

NAT-MCH by N.A.T.

Setup

- Base Configuration
- Switch BASE 1GbE
- Port on/off
- Port VLAN
- 802.1Q VLAN
- 802.1X
- 802.1p
- Port Mirroring
- Jumbo Frame
- Link Aggregation
- Rapid Spanning Tree
- Link Status
- PCME2006 counters
- Configure PCIe Virtual Switches

Maintenance

- Board Information
- System Information
- Reboot NAT-MCH
- Update MCH
- Change Password
- N.A.T. Webpage
- Home

Welcome to the HTML based NAT-MCH configuration tool.

Setup Functions:

Base Configuration:	- Changes Base Configuration.
Age Time:	- MAC Table setup: set the aging of the MAC Table Entries.
Port VLAN:	- Port based VLAN setup and port enable/disable.
802.1Q VLAN:	- 802.1Q VLAN setup.
802.1X:	- 802.1X security setup.
802.1p:	- 802.1p Quality of Service setup.
Port Mirroring:	- Mirroring of the inbound and outbound traffic on a port
Jumbo frames:	- Support of the Jumbo frames on a port
Link Aggregation:	- Support of up to four the Link Aggregation groups
Rapid Spanning	- Support of the Rapid Spanning Tree by 1GbE-Switch
IGMP Snooping	- Support of the IGMP Snooping by 10GbE-Switch (FM4000 only)
Link Status:	- Show the current status of the Ethernet links
Counter Statistic:	- Show the counter statistic of the Ethernet switch

Maintenance Functions:

Script Management:	- Backup/Restore settings to/from flash memory or file.
Board Information:	- Provides hardware information of this NAT-MCH.
System Information:	- Collect hardware information of this system.
Reboot NAT-MCH:	- Allows rebooting over the Web-Interface.
Update MCH:	- Allows updating several components over the Web-Interface.
Change/Reset Password:	- Allows changing or resetting of the MCH Password over the Web-Interface.
N.A.T. Webpage:	- Opens the N.A.T. webpage in a new browser window.
Home:	- Shows this page.

Web Interface Release: V1.30 Final (11:35:34 Nov 26 2014)

goahead
WEB SERVER
powered by GoAhead Webserver

JAVA Tool

OS independent



The image shows the NATview 2.25 software interface. On the left, a blue sidebar contains a magnifying glass icon and a list of licensed options. Two orange arrows point from the sidebar to the main window. The main window displays a hardware rack view at the top, a resource tree on the left, and a detailed sensor view on the right.

Licensed options:

- FRU Editor
- Backplane View
- HPM Update
- MCH Scanner
- System Dump
- Event Log

Resources of system 192.168.137.185:

- [003] N.A.T. GmbH - Germany NAT
- [005] N.A.T. GmbH - Germany NAM
- [006] N.A.T. GmbH - Germany NAM
- [007] N.A.T. GmbH - Germany NAM
- [203] Temp CPU
- [202] Temp CPU max
- [201] Temp PCB
- [200] Temp PCB max
- [199] 1.0V
- [198] 1.2V
- [197] 1.5V
- [196] 1.8V
- [195] 2.5V
- [194] Current
- [193] HotSwap
- [192] HS 007 AMC3
- [008] N.A.T. GmbH - Germany NAM
- [009] N.A.T. GmbH - Germany NAM
- [010] N.A.T. GmbH - Germany NAM
- [011] N.A.T. GmbH - Germany NAM
- [012] N.A.T. GmbH - Germany NAM

Sensor # 203 / LUN 0: Temp CPU = 40.0 degree Celsius (n/a -- n/a)

Temperature (deg C) 40,00

	MIN	MAX
non-critical	8.0	75.0
critical	4.0	80.0
non-recoverable	2.0	110.0

Buttons: Edit thresholds, Cancel, Update

Your Maintenance Tools

Examples of command line interface (CLI)



- `sdrrep_info` - SDR repository information
- `sel_info` - System Event Log information
- `show_ekey` - **Show all activated connections**
- `show_fru` - **Show all FRUs**
- `show_fruinfo` - `fru_id` FRU contents
- `show_cu` - Show cooling unit
- `show_pm` - Power Module Status
- `show_sensorinfo` - **Show sensors for FRU**
- `version` - Print firmware version information
- `ni` - Print network configuration
- `nlstory`

MicroTCA.4

Configuration and Maintenance



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Web Interface

Source of IP address



Change MCH Configuration

MCH global parameter	Configuration
remote interfaces:	
Management interface at GbE port	disabled
RMCP access	enabled
telnet access	enabled
WEB access	
IP address source for management port	no IP address board configuration ✓ DHCP ShM IP link record CM IP link record
IP address source for GbE port	
RMCP session activity timeout minutes	0 min
RMCP session activity timeout seconds	60 sec
default fan level	30 percent
MCH configuration flags:	
enable backward compatibility V2.4	no
Enable alternative cooling scheme	no
Control rear transition module fans	yes
PM Assignment strategy	strict

Emergency Shutdown

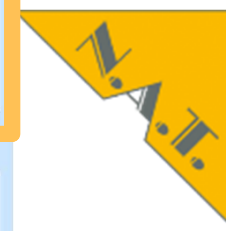
Only switch of the faulty FRU



Shelf manager parameter	Configuration
configuration flags:	
allow shelf FRU invalid	yes
temperature management	disabled FRU on critical event ✓ FRU on non recoverable event SYSTEM on critical event SYSTEM on non recoverable event
emergency shutdown	
Send SEND_MSG confirmation to SMS	
use external shelf manager	
	no

[illegible]

Ethernet switch parameter	Configuration
configuration source	✓ no configuration load from FLASH
Ignore Backplane FRU Info	no



Clock module parameter	Configuration
configuration source	no configuration

PCIe parameter	Current Configuration
configuration flags:	
upstream slot power up delay	15 sec
PCIe hot plug delay for AMCs	0 sec
hot plug support	enabled
PCIe early ekey (before payload)	disabled
Use PCIe on MCH-RTM(disable AMC12)	yes

Time Protocol/SNTP parameter	Current Configuration
Time server IP	195 . 145 . 119 . 188
'Check for Time' delay minutes	0 min
'Check for Time' delay hours	0 h
local time offset	1 h
configuration flags:	
SNTP or Time Protocol	Time Protocol
Time client	enabled

DHCP parameter	Current Configuration
Host name	MTCA4TRAINING

Configuration and Setting of Multiple MCHs

Backup Settings



Backup current configuration settings to the onboard FLASH or an external file, or load settings from the onboard FLASH or an external file.

- Save
- Restore
- Generate
- Upload
- Verify

Setup

- Show MCH Configuration
- Change MCH Configuration
- Switch BCM5396 1Gb
- General settings
- Port VLAN
- 802.1Q VLAN
- 802.1X
- 802.1P
- Port Mirroring
- Jumbo frame
- Link Aggregation
- Rapid Spanning Tree
- Link Status
- BCM5396 counters
- Configure PCIe Virtual Switches

Maintenance

- Backup Settings**
- Board Information
- System Information
- Reboot NAT-MCH
- Update MCH
- Change Password
- N.A.T. Webpage
- Home

NAT-MCH Configuration Backup

Running Configuration: [nat_mch_cfg.txt](#)

Restore the Running Configuration from the Startup Configuration

Save the Running Configuration

☒ to FLASH and load on Startup

☐ to FLASH only.

Upload configuration file:

Keine Datei ausgewählt

☒ load on startup

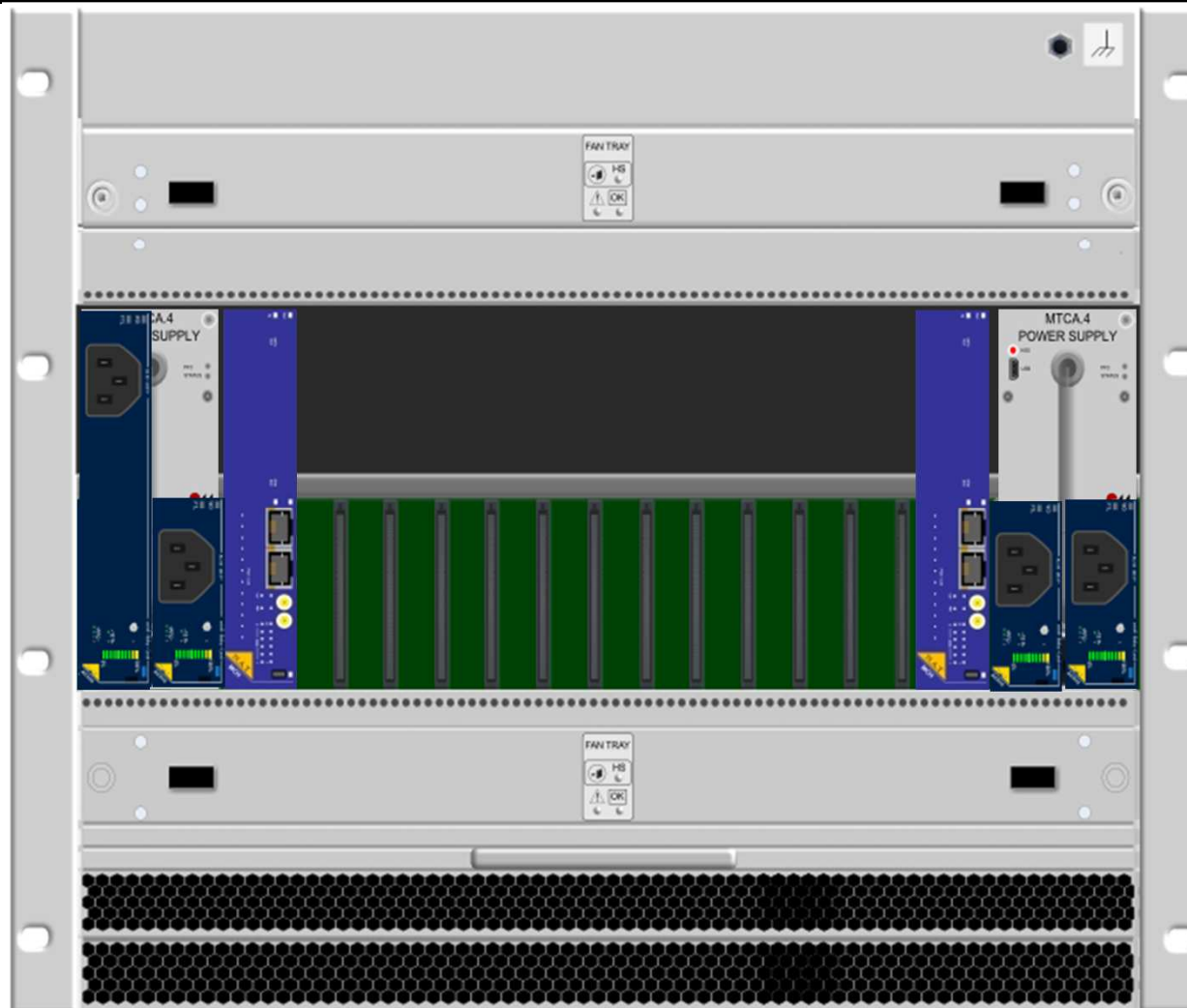
☒ save to FLASH

Verify configuration file with the Startup Configuration:

Select file: Keine Datei ausgewählt

Backplanes with 4 Power Module Sites

1, 2, 3, 4 PMs: Redundancy, Load Sharing



NATView Power Configuration Manager

Redundancy



Power Configuration Manager

Cancel Quit and Save

Status: **OK**

Power Channel:	1 MCH1	2 MCH2	3 CU1	4 CU2	5 AMC1	6 AMC2	7 AMC3	8 AMC4	9 AMC5	10 AMC6	11 AMC7
Max. Power Output (mA):	7000	7600	7600	7600	7200	7200	7200	7200	7200	7200	7200
Required Power (mA):	3500	n/a	7600	7600	n/a	7200	n/a	n/a	n/a	800	n/a

PM enable

PM1
sum : 116200 mA
max: mA
primary (0)

PM2
sum : 116200 mA
max: mA
secondary (1)

PM3
sum : 116200 mA
max: mA
undefined (ff)

PM4
sum : 116200 mA
max: mA
undefined (ff)

☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒
☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒	☒
☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐

NATView PCM

n+1 Redundancy



Power Configuration Manager

Cancel Quit and Save

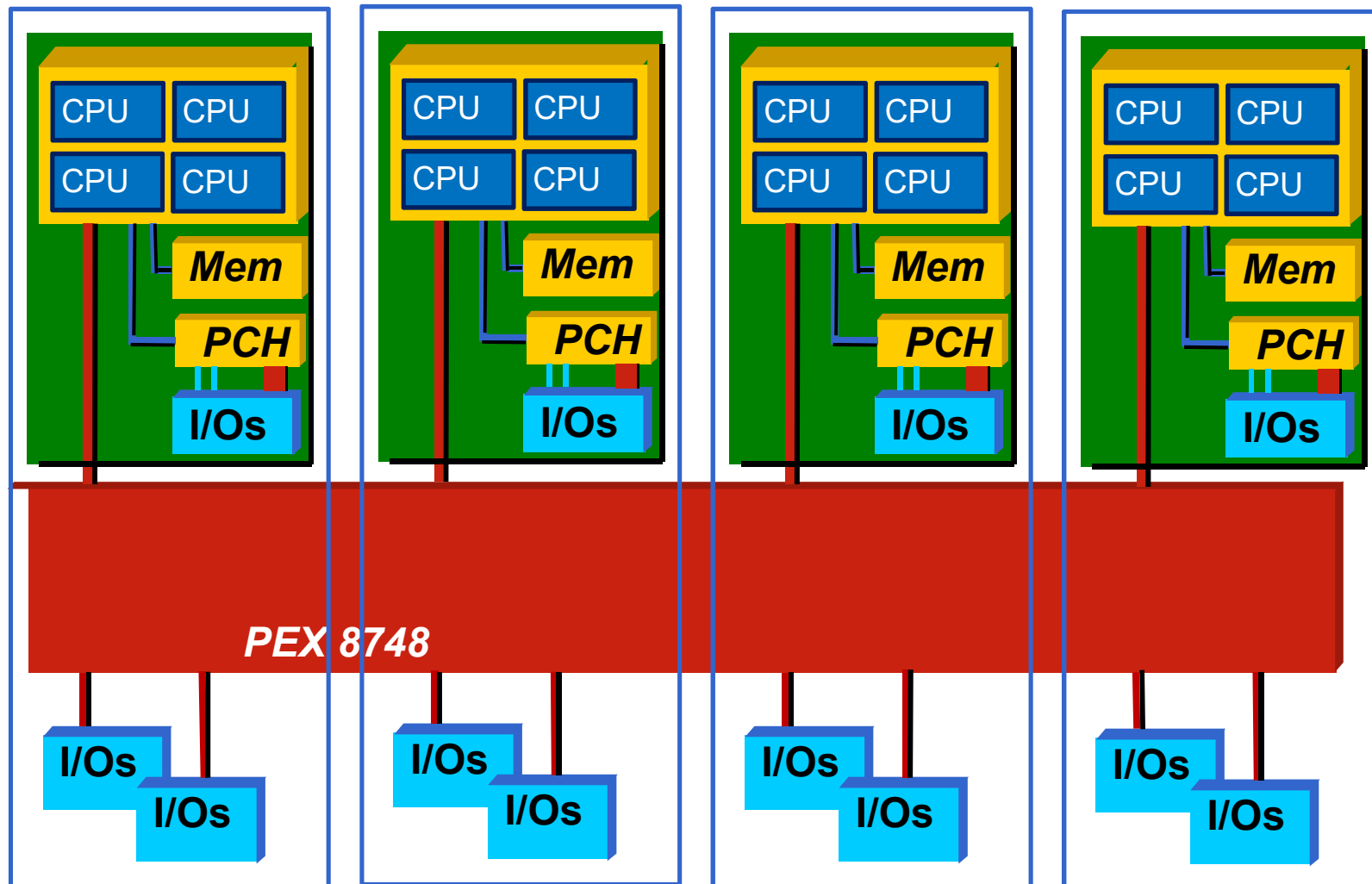
Status: **OK**

Power Channel:	1 MCH1	2 MCH2	3 CU1	4 CU2	5 AMC1	6 AMC2	7 AMC3	8 AMC4	9 AMC5	10 AMC6	11 AMC7
Max. Power Output (mA):	7000	7600	7600	7600	7200	7200	7200	7200	7200	7200	7200
Required Power (mA):	3500	n/a	7600	7600	n/a	7200	n/a	n/a	n/a	800	n/a

PM enable	PM1 sum : 116200 mA max: 50000 mA primary (0)	PM2 sum : 116200 mA max: 50000 mA primary (0)	PM3 sum : 116200 mA max: 50000 mA primary (0)	PM4 sum : 116200 mA max: 50000 mA secondary (1)
☒	☒	☐	☒	☐
☒	☐	☒	☒	☐
☒	☐	☐	☐	☐
☒	☒	☒	☒	☒

PEX8748

Multi-Host Configuration: up to 6 Cluster





NAT-MCH by N.A.T.

Setup

Base Configuration

Switch **BASE 1GbE**

Age Time

Port on/off

Port VLAN

802.1Q VLAN

802.1X

802.1p

Port Mirroring

Jumbo Frame

Link Aggregation

Rapid Spanning Tree

Link Status

BCM5396 counters

Configure PCIe Virtual

Switches

Maintenance

Board Information

System Information

Reboot NAT-MCH

Update MCH

Change Password

N.A.T. Webpage

Home

PCIe Virtual Switch configuration

Select Host AMC's (Upstream) for each virtual switch that shall be enabled first.

Select Host AMC's (Non-Transparent Upstream) for each virtual switch that shall be enabled afterwards.

Select which AMC's shall be connected to each virtual switch as downstream in the end.

Virtual Switch	Upstream AMC	NT- Upstream AMC	A M C 1 4..7	A M C 2 4..7	A M C 3 4..7	A M C 4 4..7	A M C 5 4..7	A M C 6 4..7	A M C 7 4..7
none			☐	☐	☐	☐	☐	☐	☐
Virtual Switch 0	RTM	- none -	☒	☒	☒	☒	☒	☐	☒
Virtual Switch 1	AMC 6_4		☐	☐	☐	☐	☐	☒	☐
Virtual Switch 2	- none -		☐	☐	☐	☐	☐	☐	☐
Virtual Switch 3	- none -		☐	☐	☐	☐	☐	☐	☐
Virtual Switch 4	- none -		☐	☐	☐	☐	☐	☐	☐
Virtual Switch 5	- none -		☐	☐	☐	☐	☐	☐	☐
Max. Link Speed			8.0 GT/s	8.0 GT/s	8.0 GT/s	8.0 GT/s	8.0 GT/s	8.0 GT/s	8.0 GT/s

Apply

Note: You need to click apply before you can save your changes to EEPROM.

PCIexpress Configuration Command Line Interface



```
nat> mchcfg
MCH CFG: configuration modes
  [ 2] reset to defaults
  [ 9] modify PCIe configuration
Enter configuration mode (RET=0/0x0): 9
PCIe parameter:
-----
PCIe Virtual Switch configuration
change via web-interface
VS # | Host      | NT-Host | Members
  0   | RTM       | none    | AMC01_4 AMC02_4 AMC03_4 AMC04_4 AMC05_4 AMC07_4 AMC12_4
  1   | AMC06_4   |         | AMC06_4
Upstream slot power up delay:      15 sec
PCIe hot plug delay for AMCs:      0 sec
PCIe configuration flags:
hot plug support:                  enabled
PCIe early ekey (before payload):  disabled
'no ekey' for PCIe:                disabled
PCIe clustering:                   enabled
```

MicroTCA.4

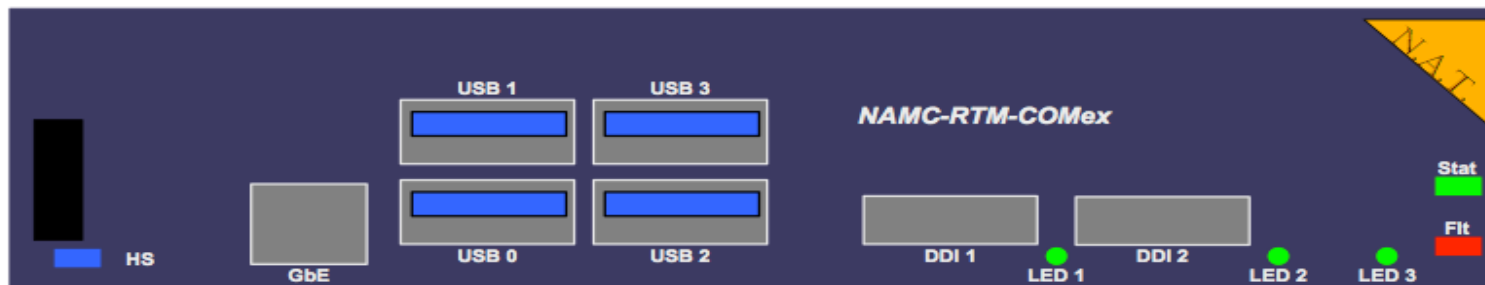
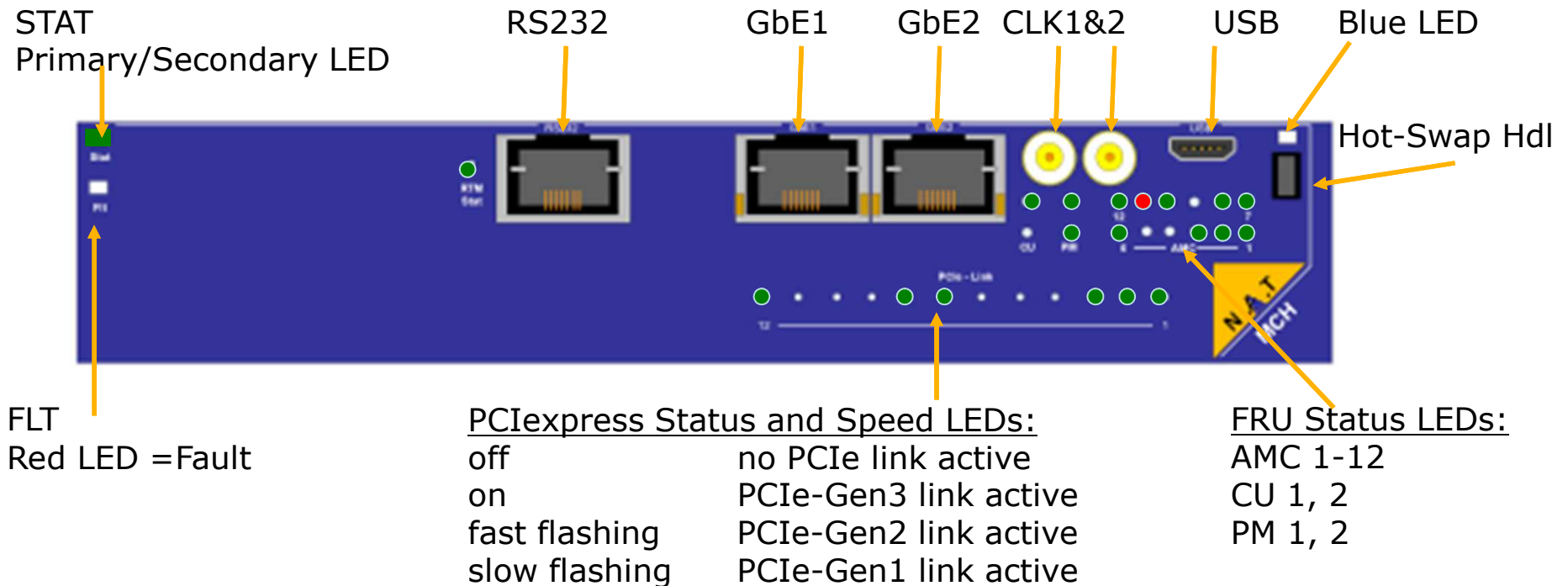
Configuration and Maintenance



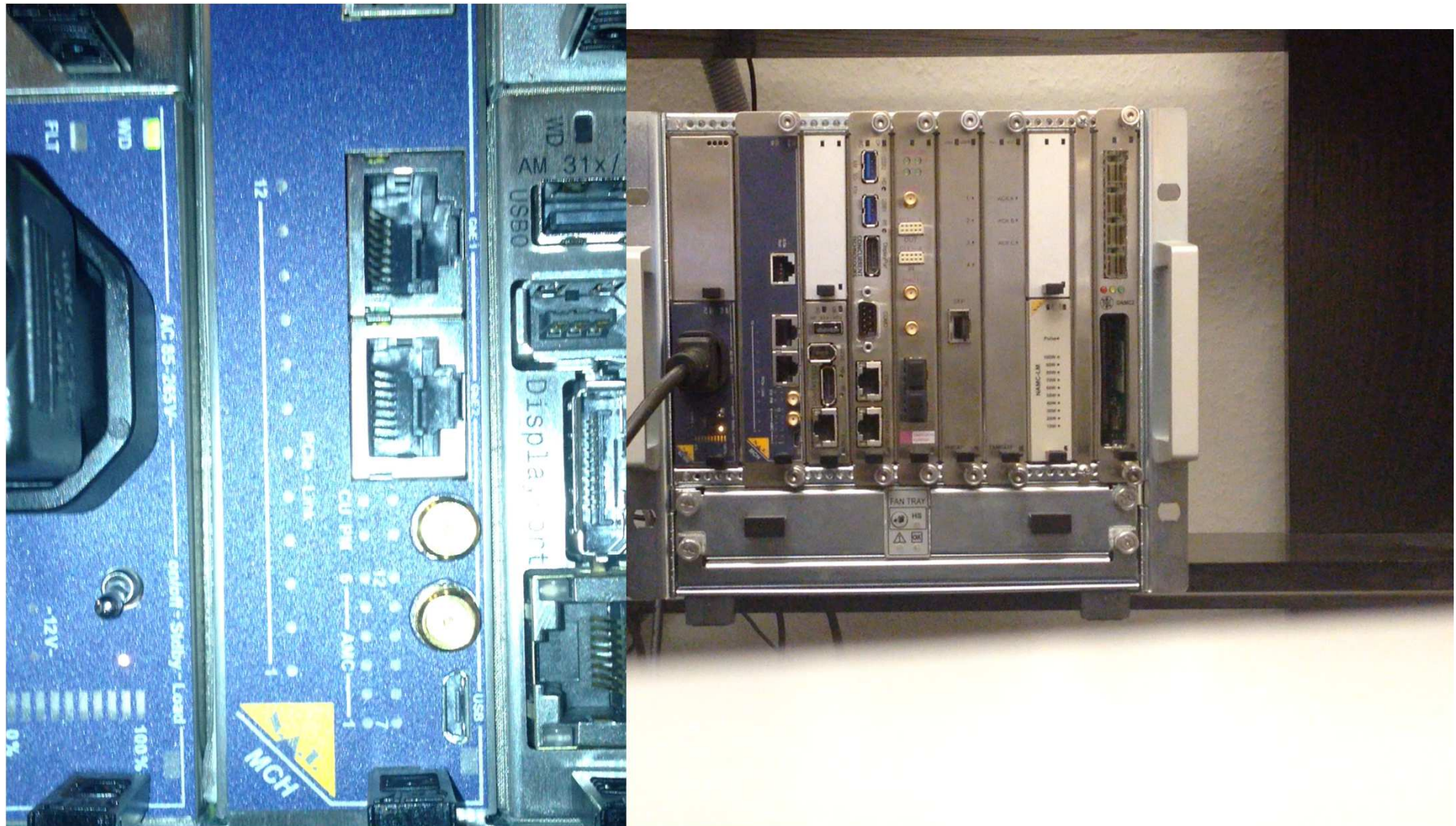
- About N.A.T.
- Comparison of Standards
- Configuration Tools
 - Command Line Interface
 - Java-App
 - Web interface
- Examples of Configurations
 - Ethernet and PCIexpress Configurations
 - Emergency Configuration
- Maintenance Tools
 - Analysis locally: LEDs
 - Analysis remotely: inventory, current, revision
 - Firmware update

Analysis locally

LEDs



Analysis locally LEDs



Analysis remotely: Webinterface

Complete Systeminformation in seconds



- Complete System Information output of the following commands collected in text file:
 - history, version, bi, mch, show_pm, show_sensor_info for all FRU-IDs
 - show_fruinfo 253 (backplane)
 - show_ekey, show_link_state,

Setup
[Show MCH Configuration](#)
[Change MCH Configuration](#)
Switch
[General settings](#)
[Port VLAN](#)
[802.1Q VLAN](#)
[802.1X](#)
[802.1P](#)
[Port Mirroring](#)
[Jumbo frame](#)
[Link Aggregation](#)
[Rapid Spanning Tree](#)
[Link Status](#)
[BCM5396 counters](#)
[Configure PCIe Virtual Switches](#)

Maintenance
[Backup Settings](#)
[Board Information](#)
[System Information](#)
[Reboot NAT-MCH](#)
[Update MCH](#)
[Change Password](#)
[N.A.T. Webpage](#)
[Home](#)

NAT-MCH System Information

collecting information about your system
please wait ...

Please download file(s) below and attach them to your support request

[nat_mch_sysinfo.txt](#)

Web Interface Release: V1.27 Final (12:41:58 Jun 26 2014)

```
***** End of History Buffer *****

***** Version Information *****
*****
** MCH CM/ShM Firmware V2.15 Final (12:36:15 Jun 26 2014) **
*****

NAT-MCH-PHYS HW: M4 PCB V1.3 Rev 130927  FPGA V1.9  AVR 1.2 - sn: 113513-0109 - Re
AOPT: 0x3d - SMA CLK, SRAM, HS Ctrl, 2nd FRT ETH, LED MOD
SATA 0 attached
CLK MOD: for Physics PCB V1.0  MC V1.3  FPGA V1.15 assembly option: HCSSL buffer
HUB MOD: PCB PCIe-x48 V2.3  MC V1.6  FPGA V1.4 (assembly option -X48 L0SC) - sn: 1
ATM MOD: ComExpress PCB V1.1  MC V1.0  FPGA V1.1 - sn: 0015 - Rel:121102 - ComEx N

OSP V1.15 Final (12:41:13 Jun 26 2014)
CM/ShM interface
Diagnose software
TCP/IP V1.1 Engineering (12:40:01 Jun 26 2014)
Telnet daemon support
compiled with GCC 2.95
Instruction cache enabled
Data cache enabled

CPU: Coldfire MCF 54450
DRAM size: 32 MB

***** Board Information *****
```


Analysis remotely

Ethernet Link Status



Setup

Base Configuration

Switch **BASE 1GbE**

Age Time
Port on/off
Port VLAN
802.1Q VLAN
802.1X
802.1p
Port Mirroring
Jumbo Frame
Link Aggregation
Rapid Spanning Tree
Link Status
BCM5396 counters
Configure PCIe Virtual
Switches

Maintenance

Board Information
System Information
Reboot NAT-MCH
Update MCH
Change Password
N.A.T. Webpage
Home

Link States of Ethernet Connections

Slot	A M C 1	A M C 2	A M C 2	A M C 3	A M C 3	A M C 4	A M C 4	A M C 5	A M C 5	A M C 6	A M C 7	A M C 7	F R T 1	F R T 2	U P D B	R T M B	C P U 1
Port	0	0	1	0	1	0	1	0	1	0	0	1	-	-	-	-	-
Links	EN	EN	EN	EN	EN	EN	EN	EN	EN	EN	EN	EN	EN	DIS	EN	EN	EN

	- Link is up
	- Link is down
"EN"	- Interface is enabled
"DIS"	- Interface is disabled

Web Interface Release: V1.30 Final (11:35:34 Nov 26 2014)

Ethernet Analysis with Wireshark

Mirroring inside GbE Port to Front GbE



NAT-MCH by N.A.T.

Setup

Base Configuration

Switch **BASE 1GbE**

Age Time

Port on/off

Port VLAN

802.1Q VLAN

802.1X

802.1p

Port Mirroring

Jumbo Frame

Link Aggregation

Rapid Spanning Tree

Link Status

BCM5396 counters

Configure PCIe Virtual Switches

Maintenance

Board Information

System Information

Reboot NAT-MCH

Update MCH

Change Password

N.A.T. Webpage

Home

Port Mirroring Configuration

FRT_1 Capture port

Slot	A M C 1	A M C 2	A M C 2	A M C 3	A M C 3	A M C 4	A M C 4	A M C 5	A M C 5	A M C 6	A M C 7	A M C 7	F R T 1	F R T 2	U P D B	R T M B	C P U 1
Port	0	0	1	0	1	0	1	0	1	0	0	1	-	-	-	-	-
Ingress	☐	☐	☐	☐	☐	☒	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐
Egress	☐	☐	☐	☒	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐	☐

Apply Discard

Deactivate

Web Interface Release: V1.30 Final (11:35:34 Nov 26 2014)

Ethernet Analysis with Wireshark

Mirroring IPMI Traffic



MCH Configuration - Chromium

MCH Configuration x

192.168.100.119/index.asp

Thorsten

NAT-MCH by N.A.T.

Setup

- Base Configuration
- JSM
- Switch BASE 1GbE
- Age Time
- Port on/off
- Port VLAN
- 802.1Q VLAN
- 802.1X
- 802.1p
- Port Mirroring
- Jumbo Frame
- Link Aggregation
- Rapid Spanning Tree
- Serdes/SGMII
- Link Status
- BCM5396 counters

Maintenance

- Script Management
- Board Information
- System Information
- Reboot NAT-MCH
- Update MCH
- Change Password
- N.A.T. Webpage
- Home

DHCP parameter	Current Configuration
Host name	

SNMP parameter	Current Configuration
SNMP server	disabled
Destination IP for SNMP Traps	0 . 0 . 0 . 0

Xilinx Virtual Cable parameter	Current Configuration
Xilinx Virtual Cable Server	disabled
Base TCP Port	2542
Maximal User defined JTAC Frequency	1.01MHz

IPMI monitor over ethernet	Current Configuration
IPMI Monitor	enabled
Target IP Address	192 . 168 . 100 . 58
Target UDP Port	623

Save Discard Changes

Reset Configuration

*eth2(noticmp) [Wireshark 1.10.6 (v1.10.6 from master-1.10)]

File Edit View Go Capture Analyze Statistics Telephony Tools Internals Help

Filter: Expression... Clear Apply Save

No.	Time	Source	Destination	Protocol	Length	Info
4	0.008755300	192.168.100.119	192.168.100.58	IPMI/A^C	77	Rsp, [uTCA] Get Power Channel Status, seq 0x29
5	1.000041000	192.168.100.119	192.168.100.58	IPMI/A^C	66	Req, [uTCA] PM Heartbeat, seq 0x2a
6	1.003404000	192.168.100.119	192.168.100.58	IPMI/A^C	65	Rsp, [uTCA] PM Heartbeat, seq 0x2a
7	1.003901000	192.168.100.119	192.168.100.58	IPMI/A^C	66	Req, [uTCA] Get Power Channel Status, seq 0x2b
8	1.008938000	192.168.100.119	192.168.100.58	IPMI/A^C	77	Rsp, [uTCA] Get Power Channel Status, seq 0x2b
9	1.405981000	192.168.100.119	192.168.100.58	IPMI/A^C	63	Req, Get Device ID, seq 0x2c
10	1.414250000	192.168.100.119	192.168.100.58	IPMI/A^C	75	Rsp, Get Device ID, seq 0x2c
11	1.990204000	192.168.100.119	192.168.100.58	IPMI/A^C	65	Req, [ATCA] Get Fan Level, seq 0x2d
12	1.993773000	192.168.100.119	192.168.100.58	IPMI/A^C	68	Rsp, [ATCA] Get Fan Level, seq 0x2d
13	2.000650000	192.168.100.119	192.168.100.58	IPMI/A^C	66	Req, [uTCA] PM Heartbeat, seq 0x2e
14	2.004040000	192.168.100.119	192.168.100.58	IPMI/A^C	65	Rsp, [uTCA] PM Heartbeat, seq 0x2e
15	2.004433000	192.168.100.119	192.168.100.58	IPMI/A^C	66	Req, [uTCA] Get Power Channel Status, seq 0x2f

Frame 12: 68 bytes on wire (544 bits), 68 bytes captured (544 bits) on interface 0

Ethernet II, Src: NAT_0b:0c:51:00:42:2b:0c:51, Dst: minimalp_3f:68:96:00:11:6b:3f:68:96

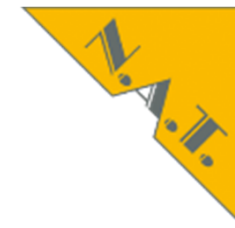
Internet Protocol Version 4, Src: 192.168.100.119 (192.168.100.119), Dst: 192.168.100.58 (192.168.100.58)

User Datagram Protocol, Src Port: 49154 (49154), Dst Port: asf-rmcp (623)

Remote Management Control Protocol, Class: IPMI

- Version: 0x06
- Sequence: 0xf
- Type: Normal RMCP, Class: IPMI
- IPMI v1.5 Session Wrapper, session ID 0x0
- Authentication Type: NONE (0x00)
- Session Sequence Number: 0x00000000
- Session ID: 0x00000000
- Message Length: 12
- Intelligent Platform Management Interface
 - [Response to: 11]
 - [Responded in: 0.003513000 seconds]
 - Header: [ATCA] Get Fan Level (Response) from 0xa8 to 0x20
 - Target Address: 0x20
 - Target_LUN: 0x00, NetFN: PICMG (Group) Response (0x2d)
 - Header checksum: 0x29 (correct)
 - Source Address: 0xa8
 - Source_LUN: 0x00, SeqNo: 0x2c
 - Command: [ATCA] Get Fan Level (0x16)
 - Completion code: Command Completed Normally (0x00)
 - Signature: 00 (PICMG (Group))
 - Data
 - Override Fan Level: 5
 - Local Control Fan Level: 15
 - Local Control Enable State: Disabled (0x00)
 - Data checksum: 0x7a (correct)

Frame (Frame), 63 bytes Packets: 16 · Displayed: 16 (100.0%) Profile: Default



More Debug Information

E-keying-debug Flag AMC in Slot 2 (FRU-ID 6)



Carrier manager parameter	Configuration
carrier number default	0
quiesced event timeout	10 sec
configuration flags:	
allow carrier FRU invalid	yes
override carrier FRU	no
shutdown system if MCH goes down	no
enable Clock E-keying	no
debug flags:	
IPMI	disabled
FRU	disabled
E-keying	disabled
sensor	disabled
event	disabled
power module	disabled
cooling unit	disabled
CM/ShM interface	disabled
FRU communication to debug (0=all)	6

Analysis Remotely: CLI

inventory, max. current, actual power consumption



- **show_fru**

FRU Information:

FRU	Device	State	Name
-----	--------	-------	------

=====

0	MCH	M4	NMCH-CM
---	-----	----	---------

3	mcmc1	M4	NAT-MCH-MCMC
---	-------	----	--------------

6	AMC2	M4	SIS8300
----------	-------------	-----------	----------------

7	AMC3	M1	NAMC-LM
---	------	----	---------

8	AMC4	M4	TAMC220-10
---	------	----	------------

9	AMC5	M4	TAMC651
---	------	----	---------

10	AMC6	M1	CCT AM 310/302
----	------	----	----------------

40	CU1	M4	Schroff uTCA CU
----	-----	----	-----------------

50	PM1	M4	NAT-PM-AC600
----	-----	----	--------------

60	Clk1	M4	MCH-Clock
----	------	----	-----------

61	Hub1	M4	MCH-PCIE
----	------	----	----------

64	RTM1	M4	MCH-RTM-ComEx
----	------	----	---------------

93	RTM4	M1	TAMC220-RTM
----	------	----	-------------

=====

- **show_pm**

- **show_sensorinfo 50**

MTCA.4 Debugging Inventory



- `show_fru`

FRU	Device	State	Name
=====			
0	MCH	M4	NMCH-CM
3	mcmc1	M4	NAT-MCH-MCMC
5	AMC1	M4	SIS8300
6	AMC2	M4	SIS8300
7	AMC3	M4	SIS8300
8	AMC4	M4	TAMC900-10
40	CU1	M4	Cooling Unit
50	PM1	M4	PDM
60	Clk1	M4	MCH-Clock
61	Hub1	M4	MCH-PCIE
64	RTM1	M4	MCH-RTM-ComEx


```
nat> show_pm
```

```
-----  
PM1: - online, primary(fru 50)      : budget 50.0 A (alloc 23.5 A  
avail 26.5 A)
```

```
PM2: - unknown
```

```
PM3: - unknown
```

```
PM4: - unknown
```

chan	FRU	FruId	primPM	secPM	PS1	POn	ENA	MP	PP	Amps

1	MCH1	3	1	-	Y	Y	Y	Y	Y	5.5
2	MCH2	4	-	-						
3	CU1	40	1	-	Y	-	Y	Y	Y	4.5
4	CU2	41	-	-						
5	AMC1	5	1	-	-	-	-	-	-	
6	AMC2	6	1	-	Y	-	Y	Y	Y	5.0
7	AMC3	7	1	-	Y	-	Y	Y	-	(overcurrent)
8	AMC4	8	1	-	Y	-	Y	Y	Y	4.0
9	AMC5	9	1	-	Y	-	Y	Y	Y	4.5
10	AMC6	10	1	-	Y	-	Y	Y	-	
11	AMC7	11	-	-						
12	AMC8	12	-	-						
13	AMC9	13	-	-						
14	AMC10	14	-	-						
15	AMC11	15	-	-						
16	AMC12	16	-	-						

```
nat> show_sensorinfo 50
```

```
Sensor Information for FRU 50 / PM1
```

=====							
#	SDRType	Sensor	Entity	Inst	Value	State	Name

30	MDevLoc		0x0a	0x61			NAT-PM-AC600
1	Full	Temp	0x0a	0x61	33 C	ok	T_CPU
2	Full	Temp	0x0a	0x61	48 C	ok	T_XFrm
3	Full	Temp	0x0a	0x61	35 C	ok	T-PSB
4	Full	Temp	0x0a	0x61	54 C	ok	T-PFC1
5	Full	Temp	0x0a	0x61	49 C	ok	T-REC
6	Full	Voltage	0x0a	0x61	264 V	ok	VINAC
7	Full	Voltage	0x0a	0x61	444 V	ok	VINDC
8	Full	Voltage	0x0a	0x61	12.4 V	ok	12V
9	Full	Voltage	0x0a	0x61	3.4 V	ok	3.3V
10	Full	Current	0x0a	0x61	5.50 A	ok	I_Sum
11	Compact	Current	0x0a	0x61	2.20 A	ok	I_CH01
12	Compact	Current	0x0a	0x61	0.00 A	ok	I_CH02
13	Compact	Current	0x0a	0x61	0.50 A	ok	I_CH03
14	Compact	Current	0x0a	0x61	0.00 A	ok	I_CH04
15	Compact	Current	0x0a	0x61	0.00 A	ok	I_CH05
16	Compact	Current	0x0a	0x61	2.20 A	ok	I_CH06
17	Compact	Current	0x0a	0x61	0.00 A	ok	I_CH07
18	Compact	Current	0x0a	0x61	0.30 A	ok	I_CH08
19	Compact	Current	0x0a	0x61	0.30 A	ok	I_CH09
20	Compact	Current	0x0a	0x61	0.00 A	ok	I_CH10
21	Compact	Current	0x0a	0x61	0.00 A	ok	I_CH11
22	Compact	Current	0x0a	0x61	0.00 A	ok	I_CH12

MTCA.4 Debugging

E-Keying



- `show_ekey`

EKeying information - activated Links:

```
-----  
  AMC FRU State Channel Type Port  
=====
```

AMC1	5	M4	0	PCie	4 <-> MCH1 Fabric D downstream Gen 1, no SSC
					5 <-> MCH1 Fabric E downstream Gen 1, no SSC
					6 <-> MCH1 Fabric F downstream Gen 1, no SSC
					7 <-> MCH1 Fabric G downstream Gen 1, no SSC
AMC2	6	M4	0	PCie	4 <-> MCH1 Fabric D downstream Gen 1, no SSC
					5 <-> MCH1 Fabric E downstream Gen 1, no SSC
					6 <-> MCH1 Fabric F downstream Gen 1, no SSC
					7 <-> MCH1 Fabric G downstream Gen 1, no SSC
AMC3	7	M4	0	PCie	4 <-> MCH1 Fabric D downstream Gen 1, no SSC
					5 <-> MCH1 Fabric E downstream Gen 1, no SSC
					6 <-> MCH1 Fabric F downstream Gen 1, no SSC
					7 <-> MCH1 Fabric G downstream Gen 1, no SSC

.....

MTCA.4 Debugging

Result of PCIexpress Training



- `show_link_state`

```
AMC 1 Port 4 is PCIe - x4 - 2,5 GT/s
AMC 1 Port 5 is PCIe - x4 - 2,5 GT/s
AMC 1 Port 6 is PCIe - x4 - 2,5 GT/s
AMC 1 Port 7 is PCIe - x4 - 2,5 GT/s
AMC 2 Port 4 is PCIe - x4 - 2,5 GT/s
AMC 2 Port 5 is PCIe - x4 - 2,5 GT/s
AMC 2 Port 6 is PCIe - x4 - 2,5 GT/s
AMC 2 Port 7 is PCIe - x4 - 2,5 GT/s
AMC 3 Port 4 is PCIe - x4 - 2,5 GT/s
AMC 3 Port 5 is PCIe - x4 - 2,5 GT/s
AMC 3 Port 6 is PCIe - x4 - 2,5 GT/s
AMC 3 Port 7 is PCIe - x4 - 2,5 GT/s
AMC 4 Port 4 is PCIe - x4 - 2,5 GT/s
AMC 4 Port 5 is PCIe - x4 - 2,5 GT/s
AMC 4 Port 6 is PCIe - x4 - 2,5 GT/s
AMC 4 Port 7 is PCIe - x4 - 2,5 GT/s
local RTM link status:
  Ethernet - 1000Base-BX
  PCIe - x16 - 8 GT/s
```

NATView

Find MTCA Systems in the Network



MCH Scanner

IP Address Range

Start address:

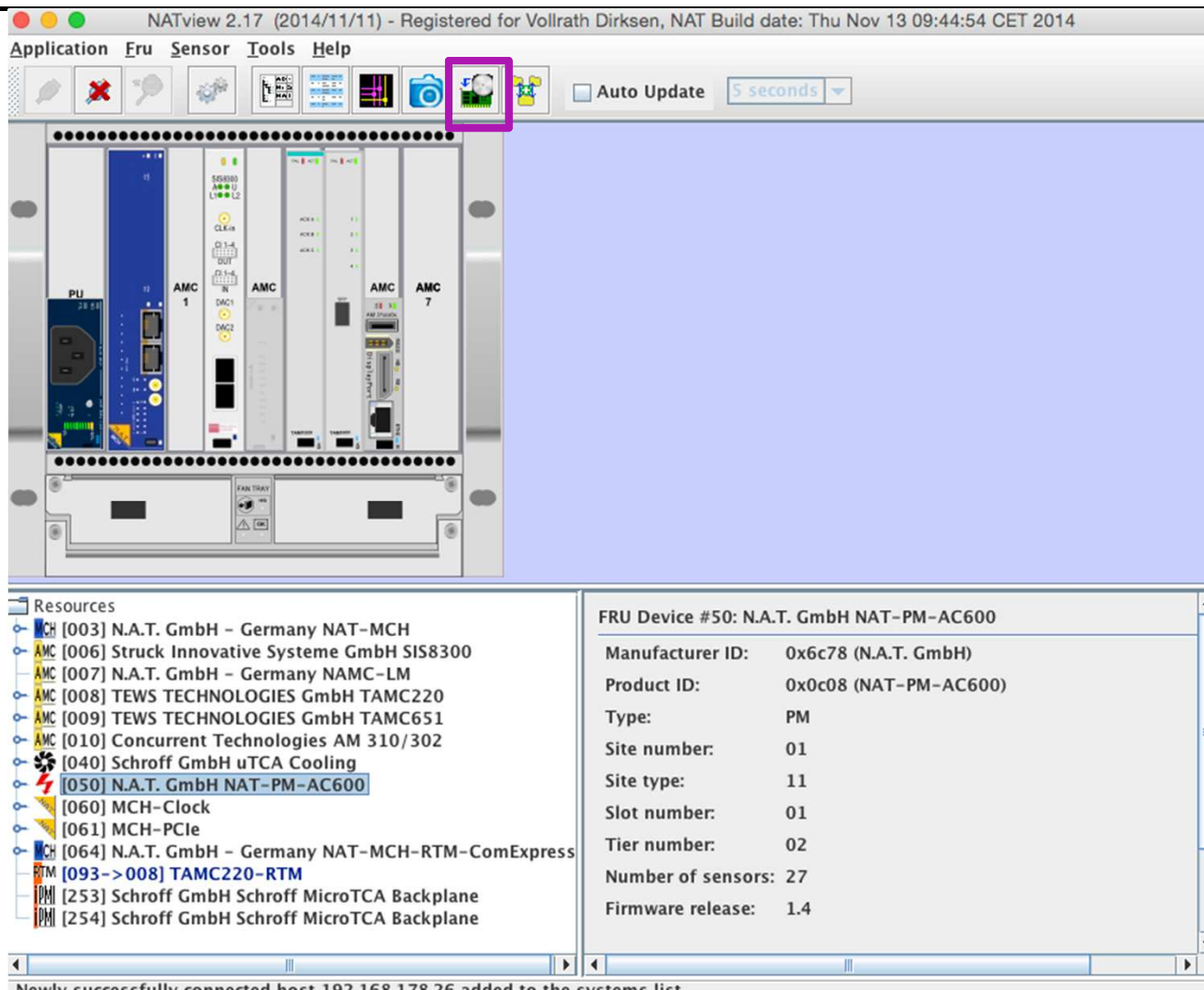
End address:

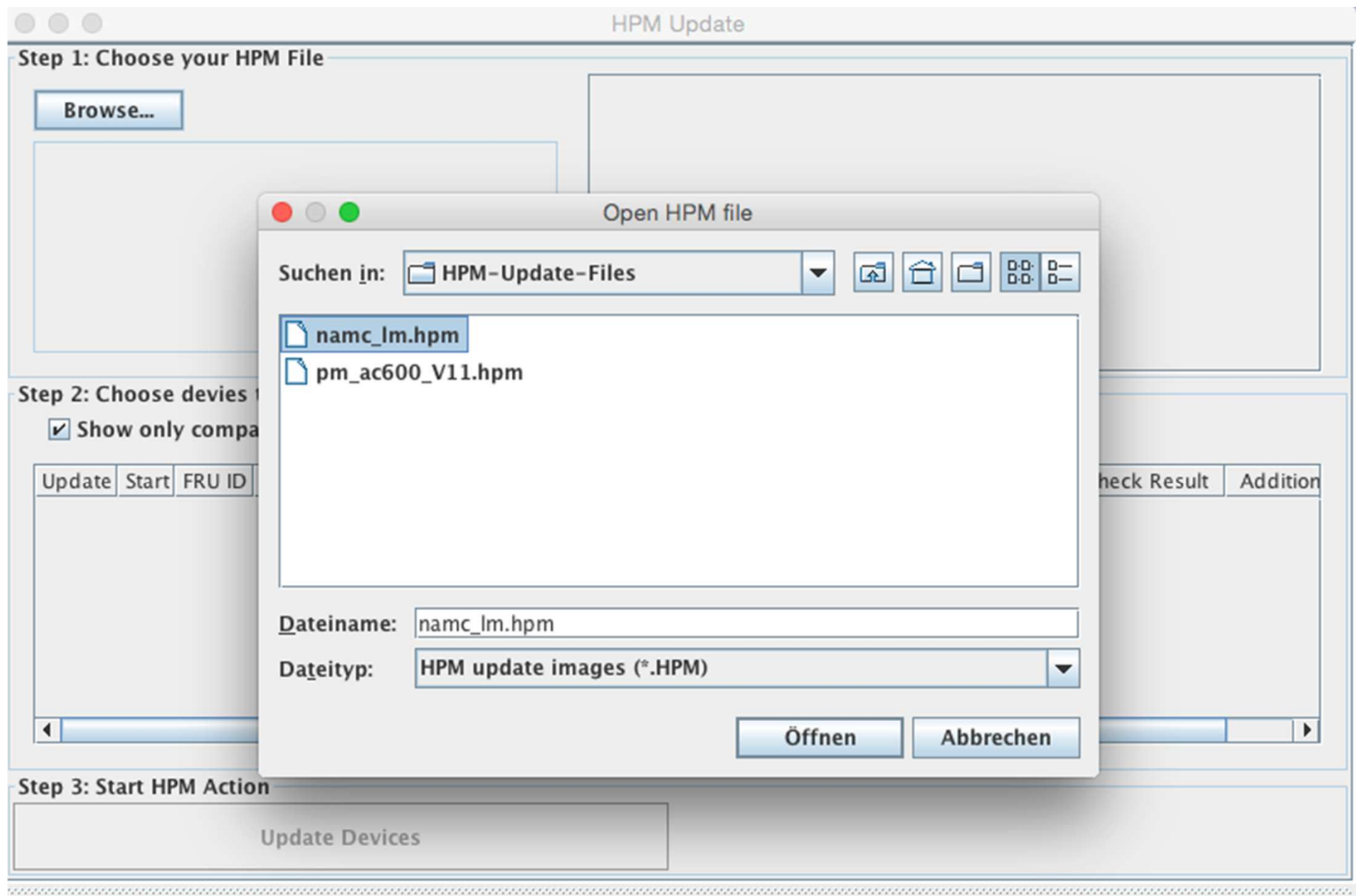
 **Start detection**

Detected systems

Select	IP Address	Carrier Manager...	Firmware Version	MCH	Chassis
☒	192.168.178.26	0x6c78/0x0b23	2.16	N.A.T. GmbH - ...	Schroff GmbH-...

Firmware Update of all System Components Easy with NATview Firmware-Update- Function





Step 1: Choose your HPM File

Browse...

/Users/vd/Documents/NAT/NAT Präsentationen/NAT-Schulungen/HPM-Update-Files/namc_lm.hpm

GENERAL	
Creation date/time:	Thu Jan 01 01:00:00 CET 1970
Image file valid?	yes
Read MD5 digest	69bbba87d97d1f17df68201a96ccfa3e
Signature valid?	yes
Device ID	0x0
Manufacturer ID	0x6c78
Product ID	0xc07
Earliest comp. revision	0.1
Firmware revision	1.0
OEM data length	0

Step 2: Choose devies to update

☒ Show only compatible FRUs

Update	Start	FRU ID	Manufacturer/Product	Status	Last Compl. Code	Firmware Rel.	Compatibility Check Result	Additional Info
☐	☒	7	N.A.T. GmbH - Germany/NAMC-LM	●	undefined (0)	-	1.5	-ok-

Step 3: Start HPM Action

Update Devices

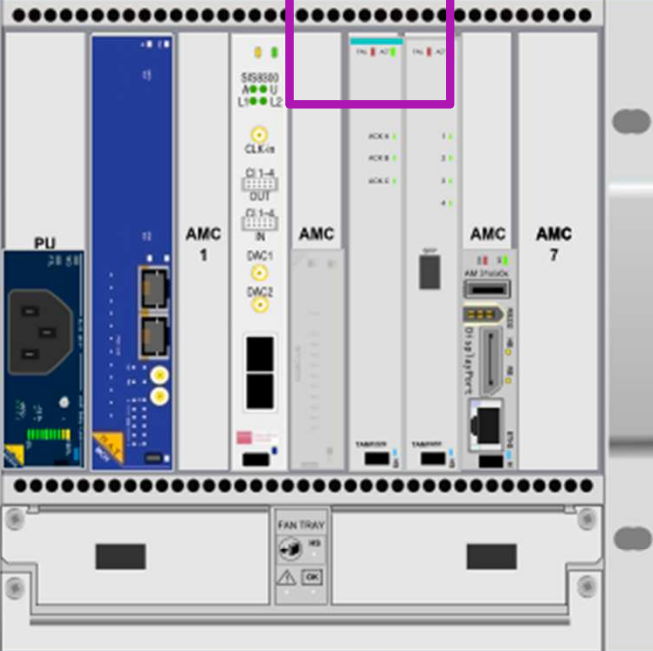
Scan for devices that are potential update candiates:

```
>> [007] N.A.T. GmbH - Germany NAMC-LM
checkCompatibleComponents: FRU #7 seems to have all necessary capabilities
Scan done.
```

NATview 2.17 (2014/11/11) - Registered for Vollrath Dirksen, NAT Build date: Thu Nov 13 09:44:54 CET 2014

Application Fru Sensor Tools Help

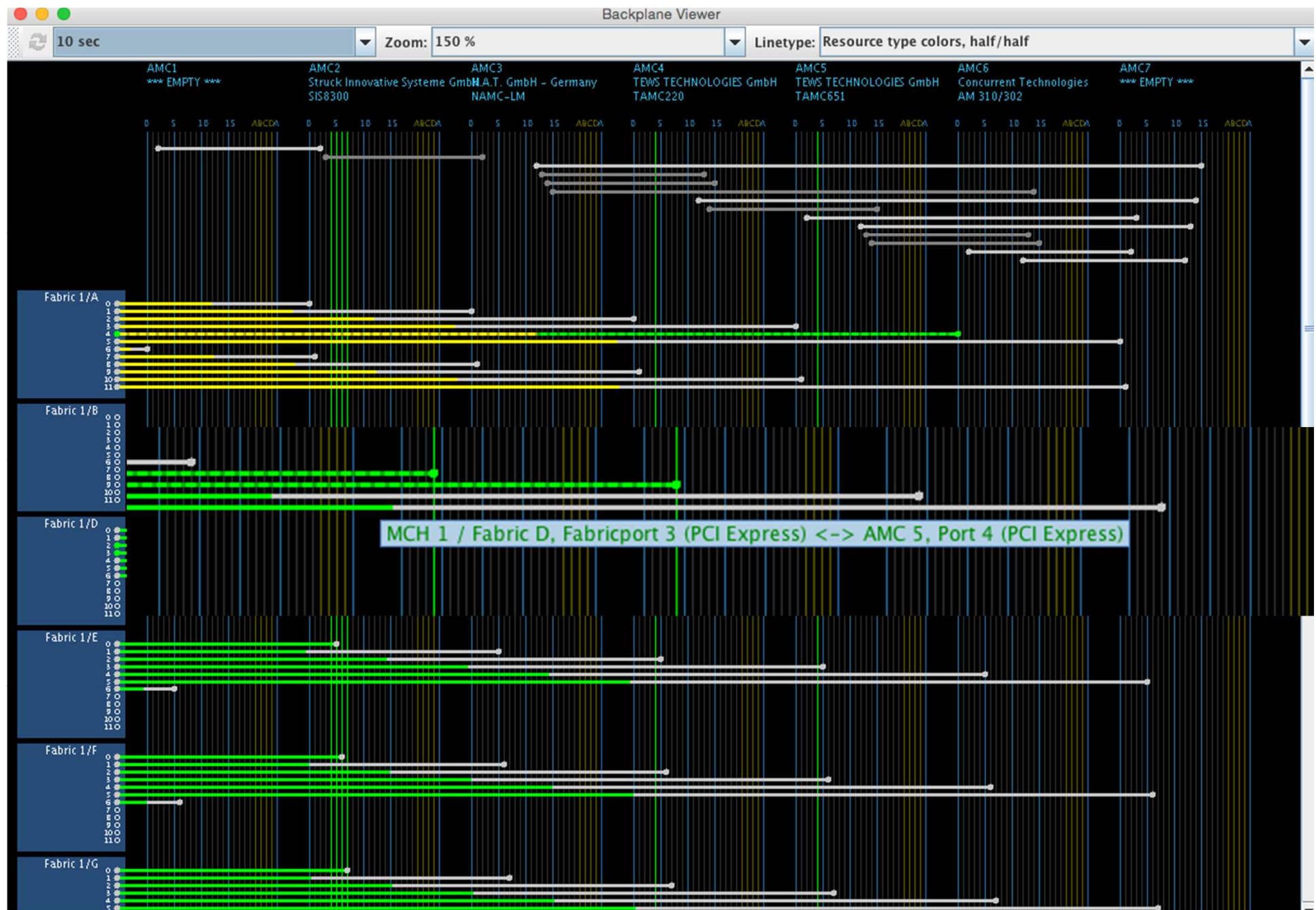
Auto Update 5 seconds



Resources

- MCH [003] N.A.T. GmbH - Germany NAT-MCH
- AMC [006] Struck Innovative Systeme GmbH SIS8300
- AMC [007] N.A.T. GmbH - Germany NAMC-LM
- AMC [008] TEWS TECHNOLOGIES GmbH TAMC220
- AMC [009] TEWS TECHNOLOGIES GmbH TAMC651
- AMC [010] Concurrent Technologies AM 310/302
- [040] Schroff GmbH uTCA Cooling
- [050] N.A.T. GmbH NAT-PM-AC600
- [060] MCH-Clock
- [061] MCH-PCIe
- MCH [064] N.A.T. GmbH - Germany NAT-MCH-RTM-ComExpress
- RTM [093->008] TAMC220-RTM**
- PMI [253] Schroff GmbH Schroff MicroTCA Backplane
- PMI [254] Schroff GmbH Schroff MicroTCA Backplane

Newly successfully connected host 192.168.178.26 added to the systems list.



NATView

Set Event Filter



Set Event Filter

Fru Filter

☐ FRU 3 ☐ FRU 4 ☐ FRU 5 ☐ FRU 6 ☒ FRU 7 ☐ FRU 8
☐ FRU 9 ☐ FRU 10 ☐ FRU 11 ☐ FRU 12 ☐ FRU 13 ☐ FRU 14
☐ FRU 40 ☐ FRU 41 ☐ FRU 42 ☐ FRU 43 ☐ FRU 50 ☐ FRU 51 ☐ FRU 60 ☐ FRU 61

Sensor Filter (as read by N.A.T. MCH)

Select	FRU ID	Sensor LUN	Sensor Nr.	Sensor Name
☐	3	0	162	Temp CPU
☐	3	0	161	Temp I/O
☐	3	0	160	HotSwap
☐	3	0	159	Version Change
☐	3	0	158	Base 1.2V
☐	3	0	157	Base 1.5V
☐	3	0	156	Base 1.8V
☐	3	0	155	Base 2.5V
☐	2	0	154	Base 3.3V

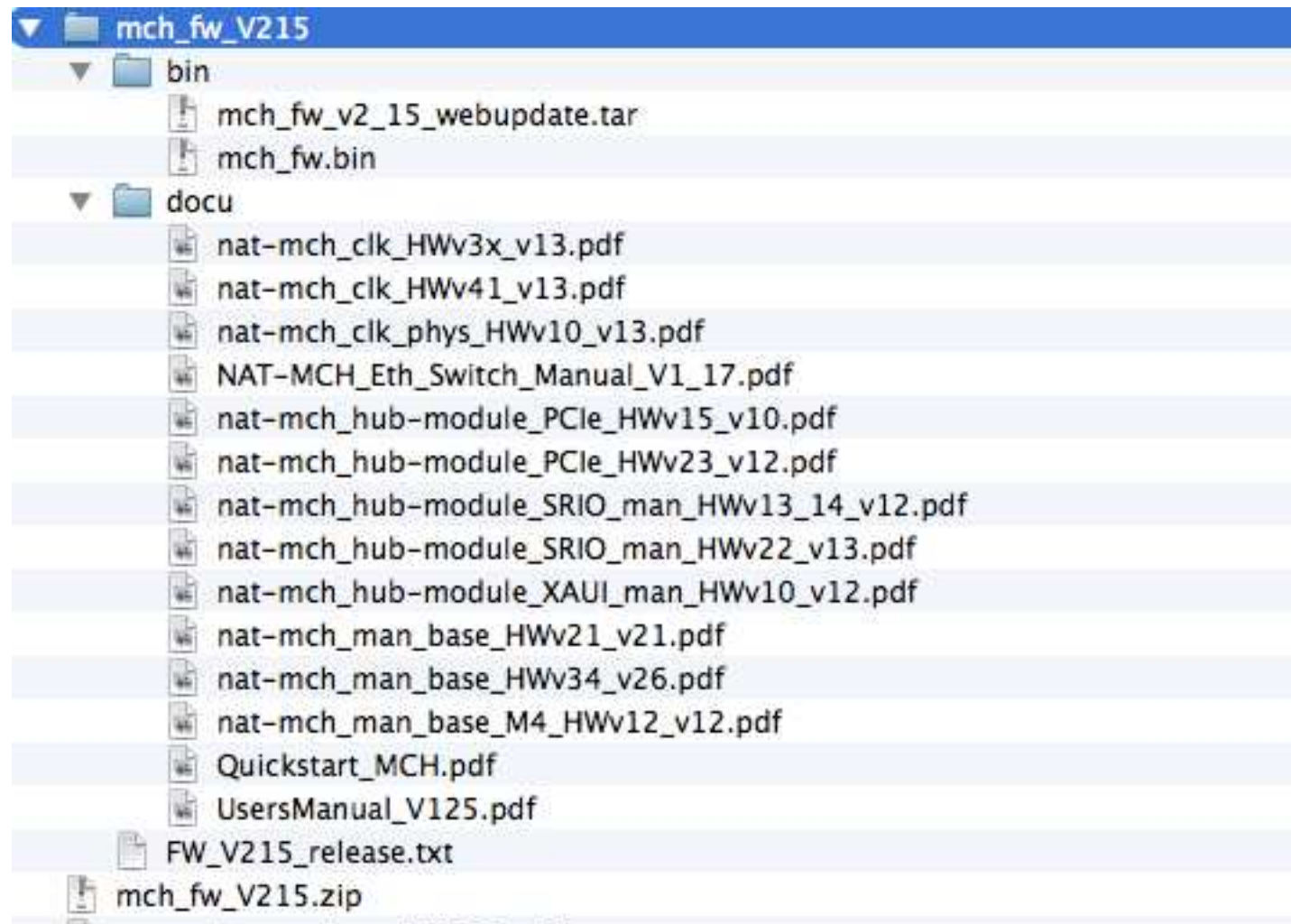
Event Category Filter

☒ Non-recoverable ☒ Critical ☒ Warning ☒ Informational

Clear all filters OK Cancel

Firmware Update

NAT-MCH: Unzip firmware (Password!)



MCH Firmware Update

Web Interface



Setup
Base Configuration
Switch BASE 1GbE
Age Time
Port on/off
Port VLAN
802.1Q VLAN
802.1X
802.1p
Port Mirroring
Jumbo Frame
Link Aggregation
Rapid Spanning Tree
Link Status
BCM5396 counters
Configure PCIe Virtual Switches

Maintenance
Board Information
System Information
Reboot NAT-MCH
Update MCH
Change Password
N.A.T. Webpage
Home

Firmware Update for NAT-MCH

• Upload TAR archive for NAT-MCH:

Select file: Datei auswählen mch_fw_...date.tar
Upload Cancel

Notes:
Select only a .tar-file here, do not select a .zip or .bin file.
After clicking Upload you can select the components to be updated.

MCH Firmware Update

Web Interface



Device	Current FW version	Update FW version	Update this device?
Base board			
Firmware	V2.15	V2.16	☒
Clock module			
Hub module			
PCIe Atmel	V1.9	V1.9	☐
PCIe HUB Module FPGA	V1.5	V1.5	☐

MicroTCA.4

Configuration and Maintenance



- About N.A.T.
- **Comparison of Standards**
- **Configuration Tools**
 - Command Line Interface
 - Java-App
 - Web interface
- **Examples of Configurations**
 - Ethernet and PCIexpress Configurations
 - Emergency Configuration
- **Maintenance Tools**
 - Analysis locally: LEDs
 - Analysis remotely: inventory, current, revision
 - Firmware update

It is time ... to change your Computing Platform!



Thank you very much!

Questions?



Thomas Holzapfel
thomas.holzapfel@powerbridge.de

Vollrath Dirksen
vollrath@nateurope.com



N.A.T. GmbH
Konrad-Zuse-Platz 9
53227 Bonn, Germany

www.nateurope.com

MTCA.4 Training:

mtca.desy.de/support/training

www.nateurope.com/services/support.html

www.powerbridge.de