Abstracted Hardware and Middleware Access in Control Applications

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Other DOOCS Server MicroTCA AMC TMCB2 **PCIe Backend DOOCS Backend ReboT Backend** Dummy Backend **Device Access Library** GUI: Register propertie Options Python Bindings Qt Hardware Monitor ontinuous read (250 r Register name AREA_DMAABLE_FIXEDPOINT16_3 Read after write Show plot window WORD_STATUS UMMY4 UMMY5 WORD_USER Operations **Matlab Bindings** Register bai WORD_CLK_CNT Read VORD_CLK_CNT_ Reaister widt Write egister addres WORD CLK CNT WORD CLK MUX Fractional bits VORD_CLK_MUX (Number of element Command Line Tools WORD_CLK_MUX_ WORD_CLK_MUX Sign bit WORD CLK MUX WORD_CLK_DUMM Device status WORD_CLK_RST evice is open. Close WORD_ADC_ENA raw (dec) ⊨ raw (hex) ⇒ double AREA DMAABLE Device properties ARFA DMA VIA DM 0.1250 REA_DMAABLE_FIXEDPOINT10_ AREA DMAABLE FIXEDPOINT1 0.5000 1.1250 evice file MOTOR 0x10 2.0000 WORD_SPI_WRITE 0x19 3.1250 WORD_SPI_READ 0x24 4.5000 DESY WORD SPI SYNC 6.1250 0x31 0x40 8.0000 Load Boards Autoselect previous regi

The task

- > Accelerator controls need complex devices servers
- > Requires communication to FPGAs, microcontrollers, frontend and middelware PCs with different protocols via PCIe, Ethernet, etc.
- > Devices should be used in various other facilities with different control systems
- XFEL and FLASH at DESY using DOOCS
- ELBE at HZDR using OPC UA
- FLUTE at KIT using EPICS 3
- TARLA in Ankara using EPICS 4

ChimeraTK

> Framework to abstract applications from the details

The DeviceAccess library

- > Access to register-based devices
- > Common interface to backends which implement different communication protocols
- > RegisterAccessor objects represent registers as process variables (common interface with ControlSystemAdapter)
- > Register name mapping: Identify registers by name instead of numerical address
- > Device name mapping: Identify devices by functional name (independent from backend)

Available backends

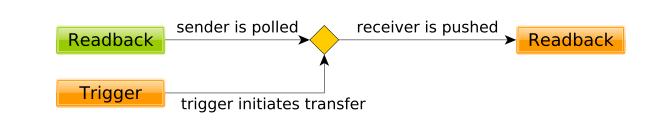
- > PCI Express
- of hardware and control system protocols
- >Write device servers which are intrinsically control system independent
- > Using modern C++11
- > Open source software, (L)GPL

ApplicationCore

- > Application modules implement the algorithms
- > Connection code combines modules and creates an application

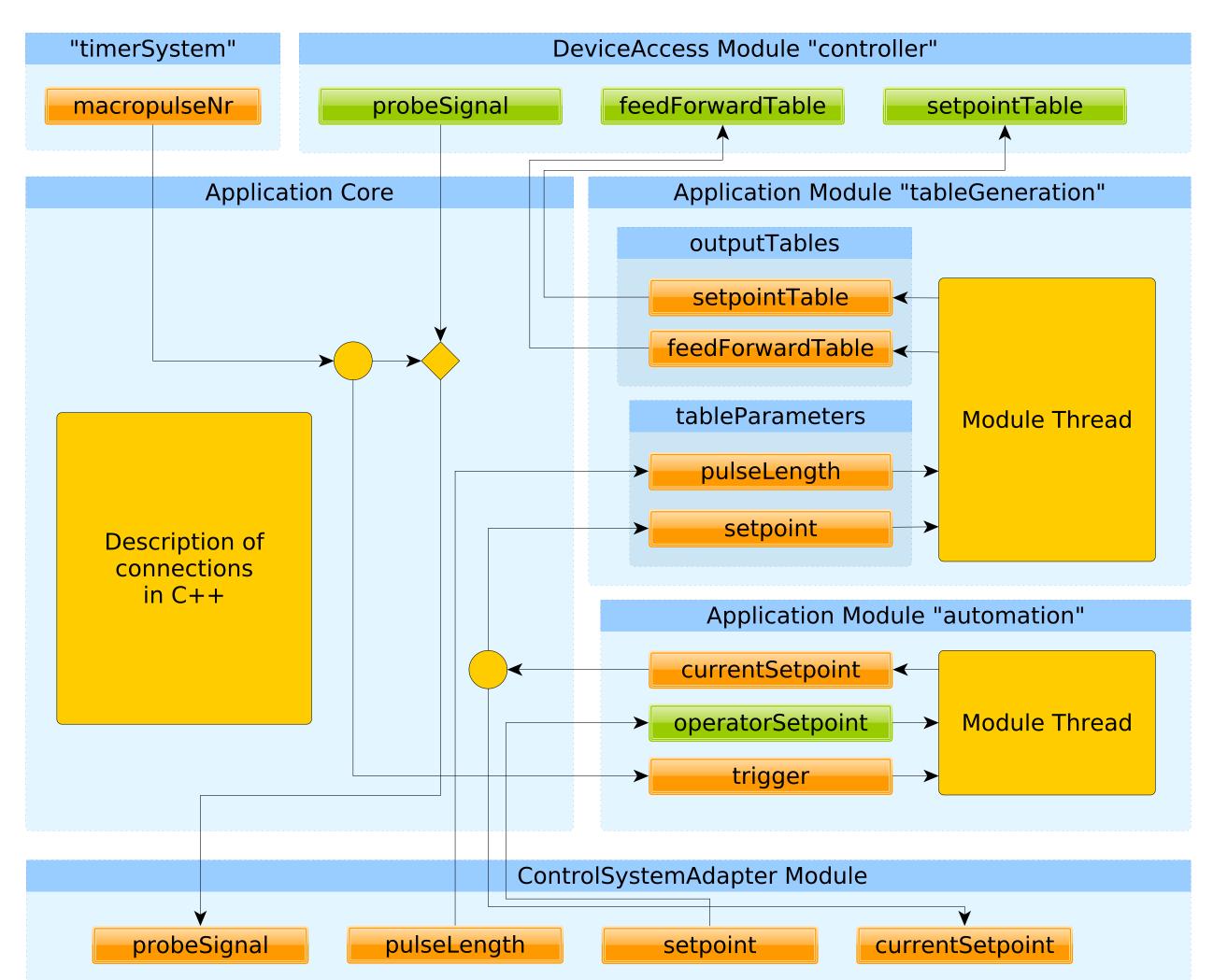
Connections

- Requirement: Intuitive syntax that minimises number of code lines
- > Use any pushing sender as trigger to connect a polled sender to a pushed receiver



> Simple network protocol for FPGAs: ReboT (Register-based over TCP)

- > DOOCS backend
- > Dummy backend / VirtualLab
- > LogicalNameMapping backend for more abstraction from implementation details of the firmware Custom backends can be loaded at run time.



Software for interactive access and scripting

- > Language bindings for Python and Matlab
- > Linux command line tool
- > Graphical user interface
- Convenient tools for firmware development: Direct hardware access without having to write code.

Application modules

Abstraction: If a module does not know if a process variable is coming from the hardware, the control system or another software module, it will not be sensitive to specifics of a particular middleware.

- > Interface consists of input and output variables
- > One thread per module
- > Two types of variables:
 - active sender pushes updates to passive receiver
 - passive sender is polled by active receiver

Readback	sender pushes	→ Readback
Readback	receiver polls	► Readback
Readback	sender pushes receiver "polls" latest update	→ Readback

> "Fan out" to distribute variables

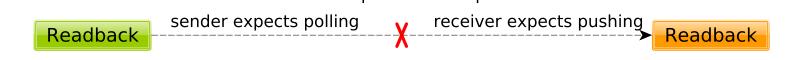


- > Connect all variables with the same name in a single command
- > Group variables and modules to structure the code
- > Plot tree with variable content of an application

ControlSystemAdapter library

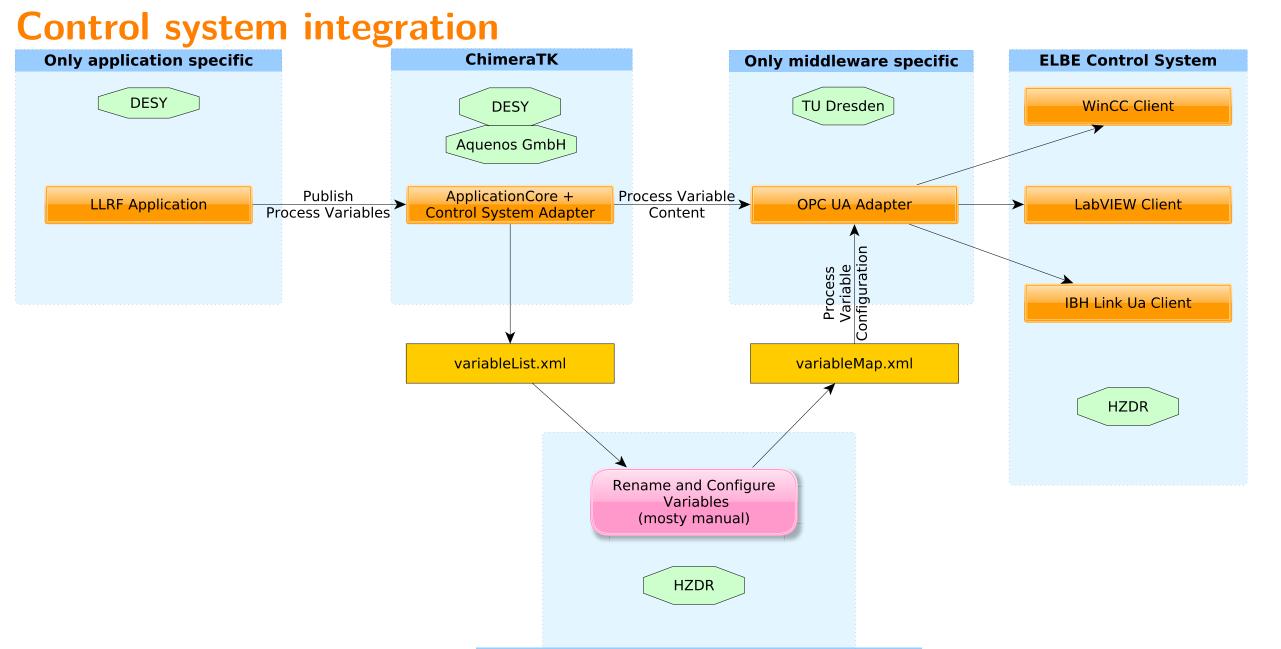
Process variables are implemented as lock-free sender/receiver pairs

- > Avoid locking problems with middleware
- > Lock-free queues allow different read-modes
- non-blocking read: return last received value if queue is empty
- read latest: empty the queue and return last received value
- blocking read: wait for new data if queue is empty
- > Basis for inter-thread communication, also in ApplicationCore



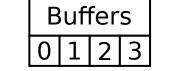
> Use *blocking read* to synchronise to other threads and to hardware

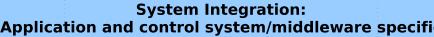
- on a single variable
- on *all* variables or *any* variable in a group
- > Hierarchical variable names
- > Advanced modelling with tags on variables

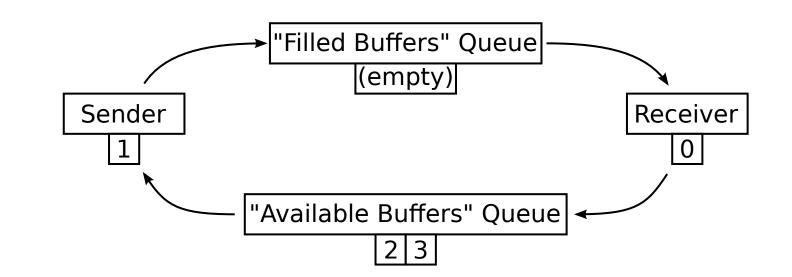


The ControlSystemAdapter ChimeraTK complemented by a middleware-specific 1S(DOOCS Adapter, OPC UA Adapter, part EPICS Adapter)

- > Publish process variables via middleware
- > Define variable name visible in control system
- > Define middleware dependent features/data types (server-side histories, display properties)
- > Application independent, configured via config file







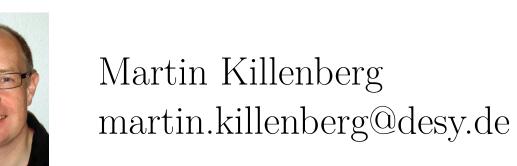
Software repositories

- > https://github.com/ChimeraTK/DeviceAccess > https://github.com/ChimeraTK/ControlSystemAdapter > https://github.com/ChimeraTK/ApplicationCore
- > https://github.com/ChimeraTK/ControlSystemAdapter-DoocsAdapter > https://github.com/ChimeraTK/ ControlSystemAdapter-OPC-UA-Adapter > http://oss.aquenos.com/svnroot/epics-mtca4u





Presenter



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