A MAJOR PERFORMANCE UPGRADE TO THE TRANSVERSE FEEDBACK SYSTEM AT THE ADVANCE PHOTON SOURCE*

TUPHA111

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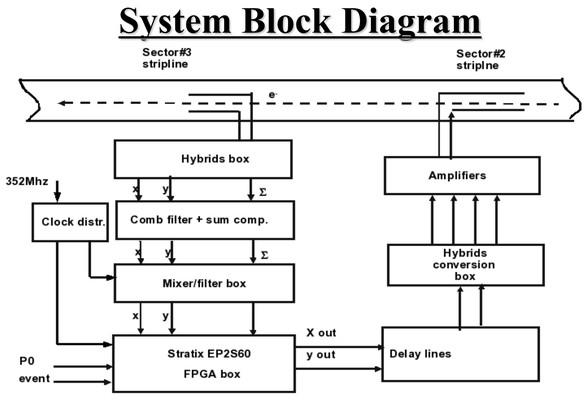
Abstract:

With the success and reliability of the transverse feedback system installed at the Advance Photon Source (APS), a major upgrade to expand the system is under way. The existing system is operating at a third of the storage ring bunch capacity, or 432 of the available 1296 bunches. This upgrade will allow the sampling of all 1296 bunches and make corrections for all selected bunches in a single storage ring turn. To facilitate this upgrade a new analog I/O board capable of 352 MHz operation was developed along with a revolution clock cleaning circuit. A 352MHz clock cleaning circuit was also required for the high-speed analog output circuit to maintain data integrity to the receiving DAC unit that is 61m away. This receiving DAC unit will have its transceiver data rate upgraded from 2.3Gbps to about 7Gbps transmitted over a fiber optic link. This paper discusses some of the challenges in reducing the clock jitter from both the system P0 bunch clock and the 352MHz clock along with the necessary FPGA hardware upgrades and algorithm changes, all of which is required for the success of this upgrade.

System Block Diagram



BlockDiagram of bunch-to-bunch feedback

The front-end input circuit was upgraded from the monopulse receiver to a 3-tap comb filter.

Single Mode Fiber connection, delay of 144ns.

Transverse Feedback – Main Box

Sec 35

Sec 02

Transverse Feedback – Remote DAC Box – Current location – About 188m

Beam direction

Transverse Feedback – Remote DAC Box – Future location – About 322m

Sec 30

Remote Fiber Optic link

Currently the remote DAC is connected via a 2.34 Gb/s fiber optic. The transmitter at the main box is in 16-bit mode while the receiver at the remote DAC box is in 8-bit mode. The 8-bit mode is used to solve two issues, 1) byte swapping that may occur at power-up or if fiber was disconnected and 2) the need to half step the delay value being sent to the remote DAC.

-- Transmitter using 117.333 MHz reference clock.
-- Receiver using 234.666 MHz reference clock.

The Upgrade will transmit 32-bits at 7.04 Gbps

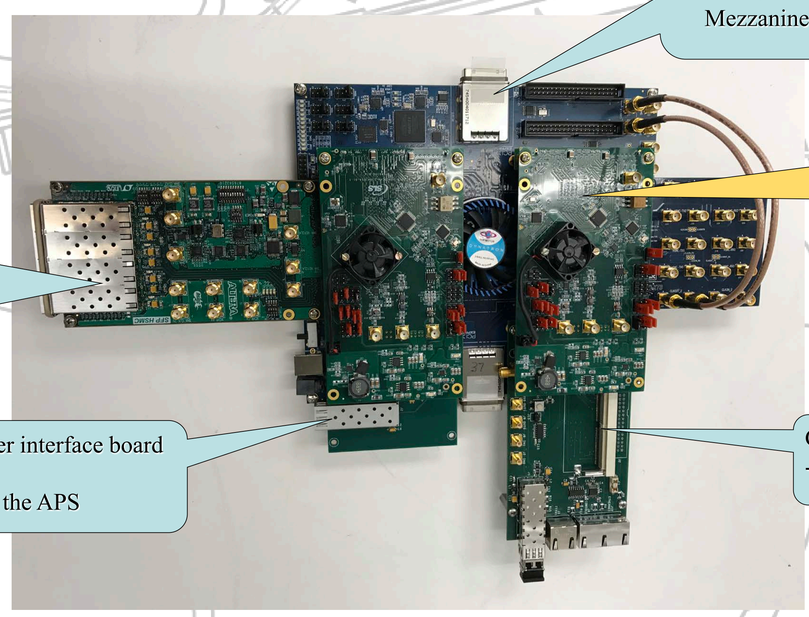
Terasic TR4 Development Kit Stratix IV GX with six HSMC (High Speed Mezzanine Card) connectors.

SFP Cage adapter board to Four SFP cages transceivers. Four SFP cages LVDS

Will be transmitting at 7.04 Gbps

This 400MSPS Data conversion board is capable of 400 MHz for the analog inputs and 400 MHz for the analog outputs. This board was developed at System Level Solutions (SLS).

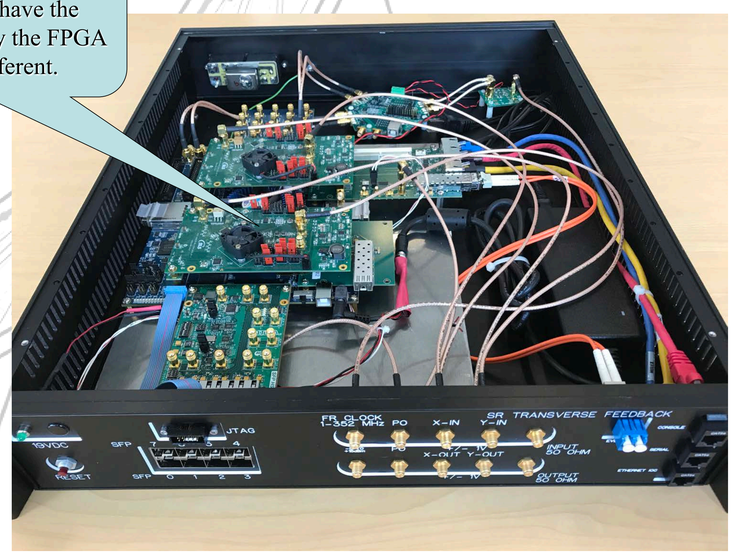
Note: two are installed.



Event Receiver interface board HSMC -developed at the APS

Coldfire daughter board HSMC -developed at the APS

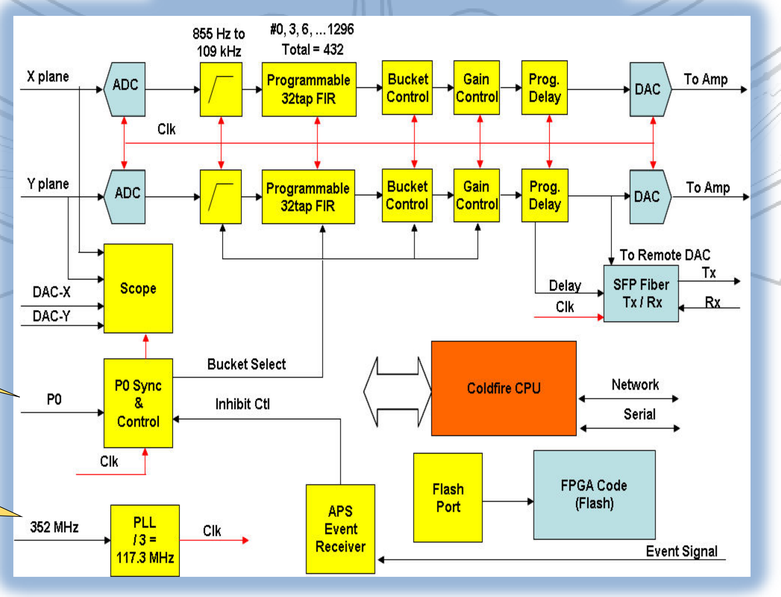
Completed chassis Both the master and the same hardware, only the FPGA firmware is different.



Transverse Feedback and Remote DAC Hardware

1) Terasic TR4 Development Kit Stratix IV GX
   a) Six HSMC (high speed mezzanine card) connectors
2) SLS 400MSPS Data Conversion HSMC (2 cards installed)
   a) One Analog to Digital converters, 14-bits
   b) One Digital to Analog converters, 14-bits
3) Coldfire CPU daughter board with HSMC connectors.
   a) Fiber optic transceiver used for the event timing system.
   b) Console, serial and Ethernet ports, RJ45
   c) Connector for an RF clock, connected to the FPGA.
   d) User defined SMB connector, 2 inputs and 2 outputs.
4) Transceiver by Finisar, model FTLF1428P2BTL
   a) A 8Gb RoHS Compliant Long-Wavelength SFP Transceiver

FPGA Main Block Diagram



New critical components needed for this enhancement

New P0 trigger input circuit needed to clean the jitter and to be synchronized to the 352 MHz source.

New input clock circuit needed to clean the jitter in the 352 MHz source.

Possible Bucket Modes

FPGA CLK	Number of buckets that can be sampled
88 MHz	Samples only 324 buckets 1) 324 mode 2) Hybrid mode 3) 648 FIR filters needed
117.3 MHz	Samples only 432 buckets 1) 24 singlet mode 2) Hybrid mode 3) 864 FIR filters needed
352 MHz	Samples all 1296 buckets 1) Any bucket configuration 2) 2392 FIR filters needed

The current configuration is 117.3 MHz.

1. Storage Ring @ 352MHz, (2.84ns)
2. Bunches/buckets = 1296
3. ADC sampling rate 352 MHz (2.84ns)
   a. Samples all of the buckets.
   b. 1296 buckets can be enabled.
4. Storage Ring turn rate = 271.6kHz (3.68μs)
5. Inputs use 14-bit A/D 400MSPS
6. Output uses 14-bit D/A 400MSPS

Conclusion

The P0 feedback system has proven to be very flexible in that it was easy to adapt when the need arose, e.g., increasing the number of buckets and adding a remote DAC function. However, the pervious configuration could not accommodate for all 1296 buckets limiting what bunch pattern could be used. The preliminary test data have shown some promise that this system can stabilize 1296 bunches in both the horizontal and vertical planes at the APS and possibly function as a bunch cleaner

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