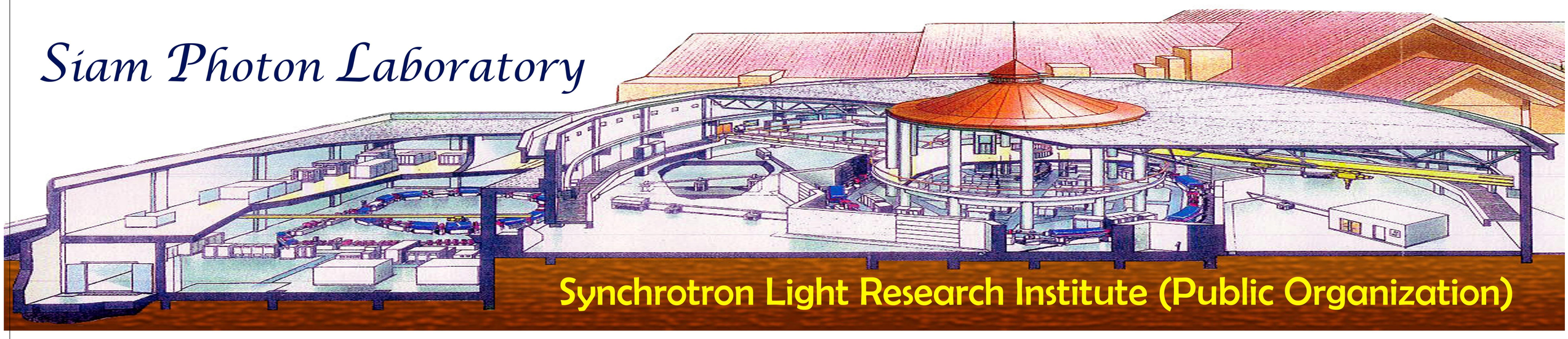

TIMING SYSTEM USING FPGA FOR MEDICAL LINEAR ACCELERATOR PROTOTYPE AT SLRI

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Introduction

Synchrotron Light Research Institute (SLRI) in Thailand has development a prototype of the 6 MeV medical linear accelerator (medical linac) for cancer treatment. This project has been proposed to help increase the availability of low-cost radiotherapy machines in Thailand. Reverse engineering approach has been employed in this project via a donated machine to develop a prototype of this machine. The linear accelerating structure has operating frequency at 2,998 MHz, a 3.1 MW magnetron driven by a solid-state modulator, and a hot-cathode electron gun. A drive stand and a gantry of the prototype provide housing for the modulator cabinet for magnetron and electron gun and automatic frequency control (AFC) system in order to provide resonant frequency tuning for the magnetron. A central control system software is designed to give access and control all subsystems. It is run on the Main Control System with a display monitor and GUI. All of the subsystems are connected to the Main Control System in a private network as shown in Figure 1

Experiment

Time domain characteristics of each of the timing signals is the main specification that needs to be verified. Figure 2 shows how the experiment was set up. All the timing signals were connected directly to an oscilloscope. Figure 2 *(left)* illustrates the block diagram of the designed system

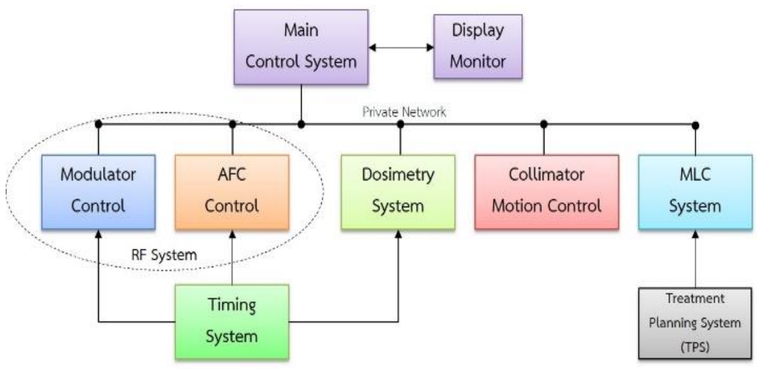
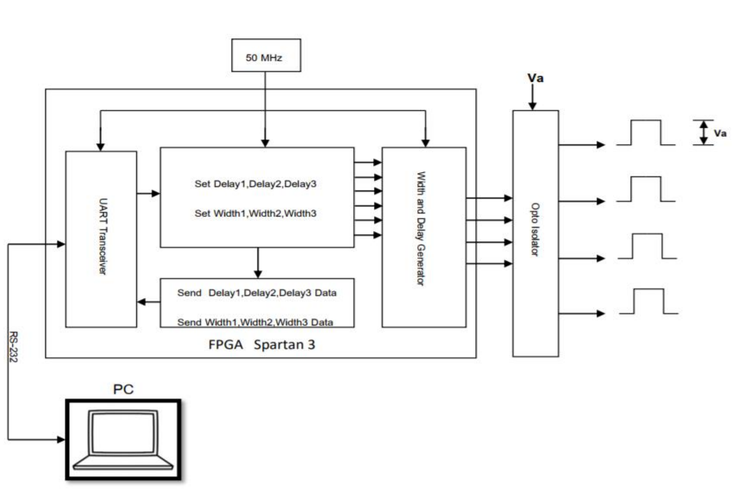


Figure 1. Network diagram of the machine prototype

Figure 2 *(right)* shows how the experiment was set up Figure 3 *(right)* shows that the reference clock shape is nearly a perfect rectangle as expected This means that it can be used as an input to the pulse width and delay generator in order to calculate and generate the correct pulse width and delay time of the required timing signals.

The following test was performed to generate four timing signals. All settings can be entered via the GUI which are listed in Table 1.



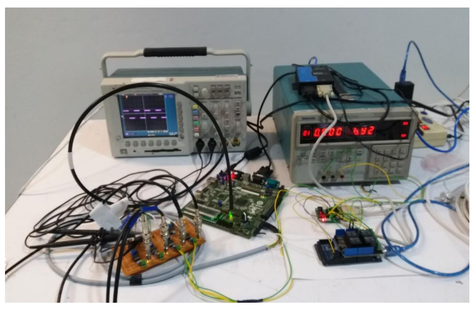
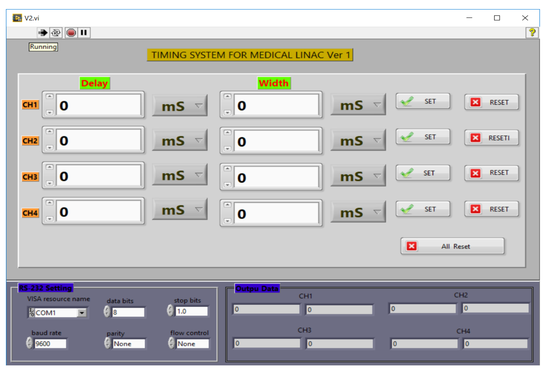


Figure 2. *(left)* Block diagram of the timing system *and (right)* Experiment set up for the timing system



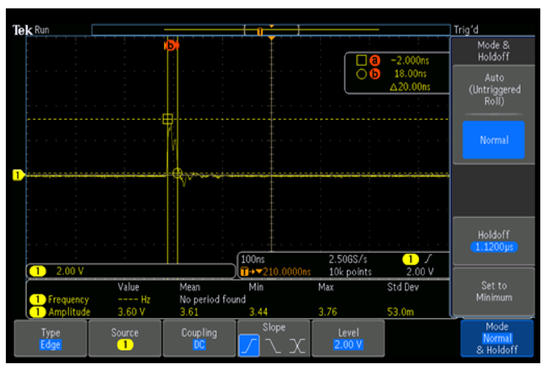


Figure 3. *(left)* Graphic user interface of the timing system *and (right)* pulse width of the reference clock

Channel	Required Values	
	Width (nsec)	Delay (nsec)
CH1	100	0
CH2	200	50
CH3	300	100
CH4	400	150

Table 1. Parameter settings of the timing signals

From the test, all four outputs from the timing system are shown to be as expected. The oscilloscope capture of the four timing signals is shown in Figure 4

Figure 4. Result of the timing signal generation

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