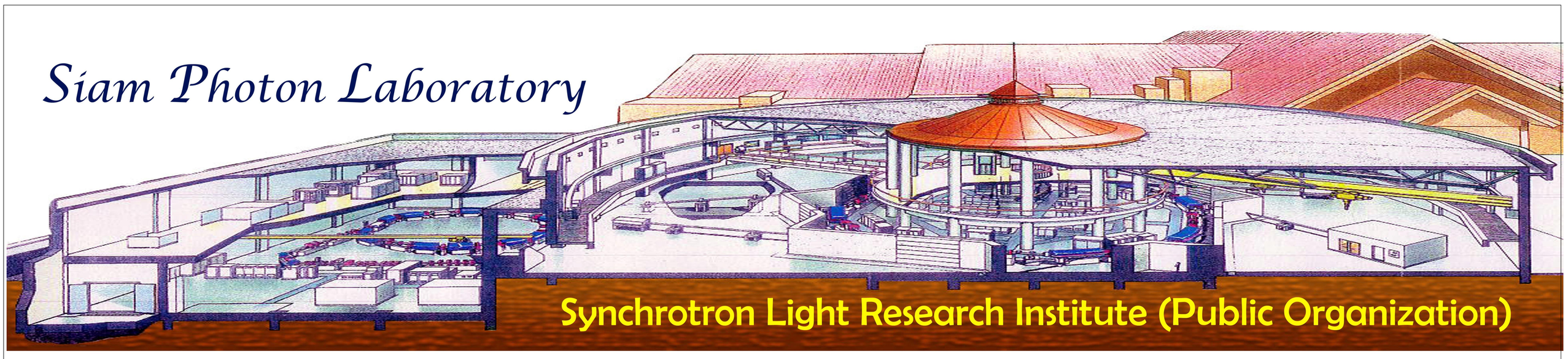

FPGA-BASED MOTION CONTROL SYSTEM FOR MEDICAL LINEAR ACCELERATOR DEVELOPMENT AT SLRI

R. Rujanakraikarn, P. Koonpong,

Synchrotron Light Research Institute, Nakhon Ratchasima, Thailand, 30000

Introduction

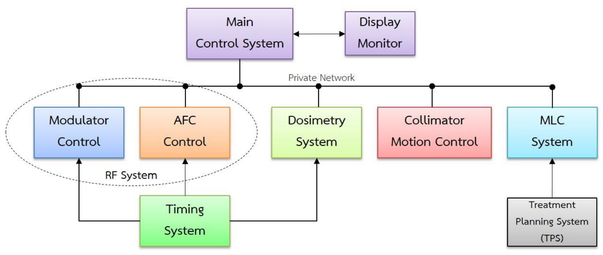

Figure 1: Network diagram of the machine prototype.

Linear accelerator has been widely utilized in radiotherapy machines. An attempt to increase the availability of the low-cost machines has been proposed for the domestic use. Currently, SLRI has developed a prototype of the 6 MeV medical linear accelerator for cancer treatment. Reverse engineering approach has been employed via a donated machine. The prototype consists of a linear accelerating structure of the S-band standing wave type at 2,998 MHz operating frequency, a 3.1 MW magnetron driven by a solid-state modulator, and a hot-cathode electron gun. A drive stand and a gantry of the prototype provide housing for a modulator cabinet and automatic frequency control (AFC) system. The main parts in a linac treatment head consist of an X-ray target, a transmission ionization chamber, and three-stage treatment beam collimators. To confine the shape and size of the radiated beam, the three-stage treatment beam collimators, which are fixed primary collimators, secondary collimators (beam limiting jaws), and a multi-leaf collimator (MLC), are used. A timing system is used to link various subsystems to provide synchronization. Main Control System software is designed to interface with all subsystems. All subsystems are connected to the Main Control System in a private network.

Control System Design

Secondary Collimators

There are two adjustable pairs of jaws, upper collimators (Y-Jaws) and lower collimators (X-Jaws), installed in the treatment head with one pair above the other and at right angles. The jaw openings can be adjusted so that a projected square or rectangular field shape at the target-to-surface distance of the machine ranges from 0x0 cm^2 to 40x40 cm^2.

Each collimator jaw is driven by a BLDC motor. Traditional H-Bridge circuit is used to provide appropriate voltage level to control the speed of the motor. The PWM and direction signals are provided by the FPGA. An in-house PWM drive PCB is designed for motor and FPGA interface. A readout potentiometer signals, whose range is from -10 volts to 10 volts, are provided to the FPGA via the PCB.

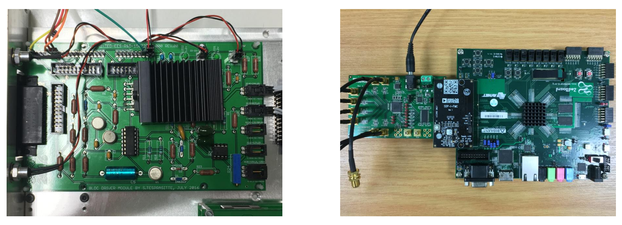

Figure 2: (left) In-house PWM drive PCB and (right) Zedboard and 8-channel ADC.

FPGA and ADC

Digilent's Zedboard featuring a Zynq XC7Z020 is chosen. Analog Devices' EVAL-AD7606SDZ and FMC adapter board are selected for a multi-channel bipolar simultaneous sampling 16-bit ADC. Two custom IPs are implemented in Programmable Logic (PL) part of the Zedboard using VHDL,

1) AD7606 Interface IP is designed with FSM to achieve timing requirements.
2) PWM Controller IP receives duty cycle in BCD form via AXI bus to generate PWM signals.

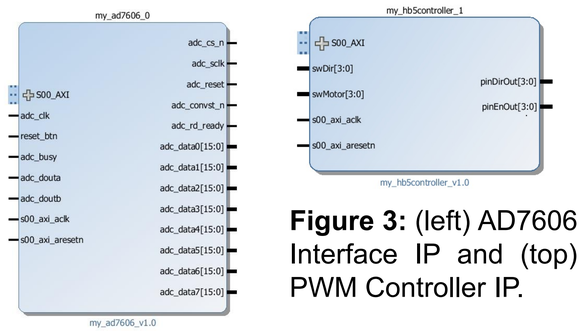

Figure 3: (left) AD7606 Interface IP and (top) PWM Controller IP.

Feedback and System Integration

DC motor position control loop is implemented using PI controller. The digital controller is realized using bilinear transformation method in the software part of the control system.

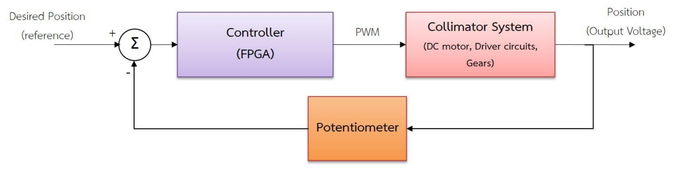

Figure 4: Feedback control loop of each collimator jaw.

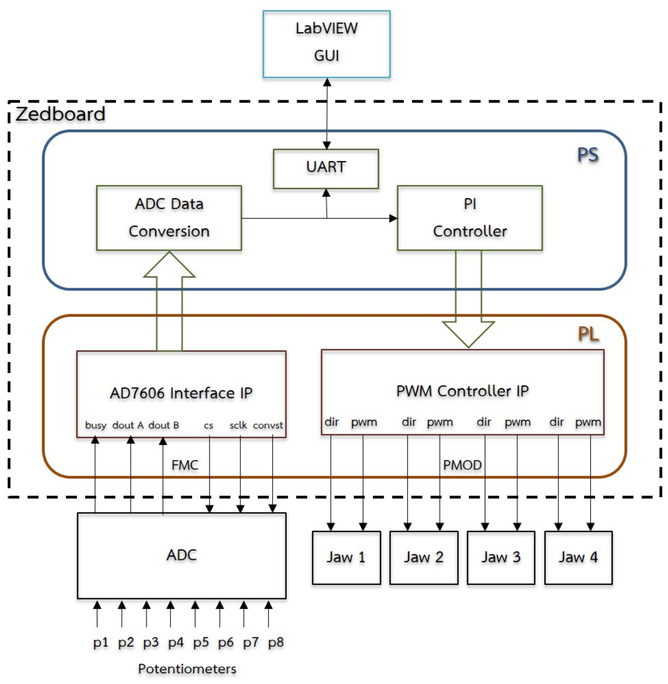

Figure 5: Block diagram of the control system and interface between hardware.

Software is coded in C in the Processing System (PS) part of the Zedboard. Three main parts, PI controller, ADC Data Conversion, and UART, are implemented in the PS. Collimator position can be displayed via LabVIEW GUI and the set points can be set and sent to PS. Both are through UART.

Two custom IPs in the PL send and receive information to PS via AXI bus interface. FMC connector is for ADC interface and PMOD connector is for PWM signals.

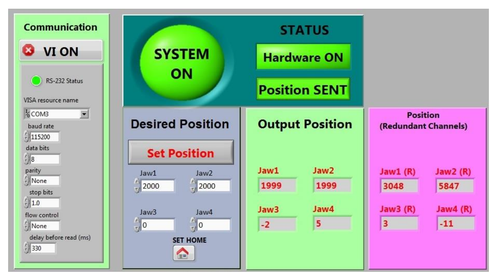

Figure 6: LabVIEW GUI.

Result and Discussion

Interface between the ADC board and FPGA was tested. The signals from FPGA to ADC are chip select (cs), serial clock (sclk), and conversion start (convst), and the signals from ADC to FPGA are busy and digital data in serial form (dout A and dout B). The result shows that all signals meet timing requirements and we receive correct information from all eight 16-bit channels with a 20 MHz sclk. The same result is also obtained from using higher sclk frequency up to 30 MHz. The result of the step response, with the best tuned gains of PI controller, was observed. The expected result of the overall system response is obtained and very satisfactory.

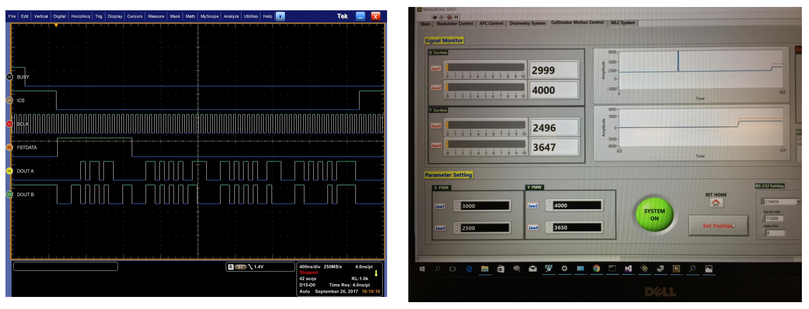

Figure 7: : (left) Interface signals between FPGA and ADC, and (right) step response of the system.

Contact

roengrut@slri.or.th
(Corresponding author)