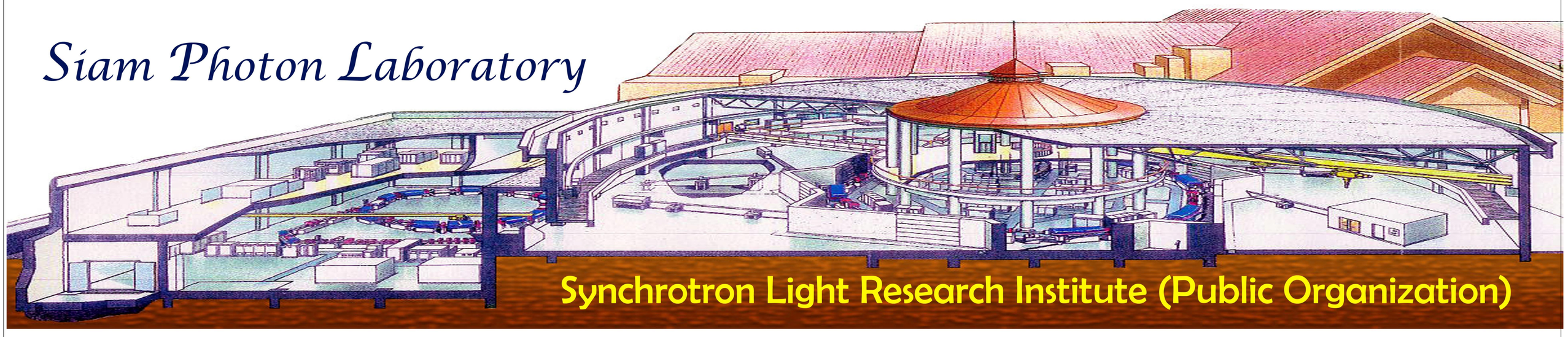

FPGA-BASED PULSED-RF PHASE AND AMPLITUDE DETECTOR AT SLRI

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Introduction

Synchrotron Light Research Institute (SLRI) is a dedicated synchrotron radiation facility in Nakhon Ratchasima, Thailand. Its 40-MeV linac has been operated since the first light in December 2001. The SLRI's linac is a 40 MeV electron linear accelerator consisting of five different parts to accelerate the electron beam. These parts are pre-buncher 1, pre-buncher 2, buncher, a 20-MeV accelerating tube 1, and 20-MeV accelerating tube 2. They are fed with a pulsed RF signal operating at 2,856 MHz as the accelerating field from a klystron. Currently, the phase and amplitude of the RF signal in the waveguide can be adjusted manually by the high power phase shifters and attenuators. With an increasing demand of higher electron beam quality, an improvement in phase and amplitude of the RF signal is necessary. The measurement system of the RF phase and amplitude in each part of the linac is needed for stability improvement.

The prototype of phase and amplitude detector is described. The system is designed to measure the phase and amplitude of a 5-μsec wide pulsed RF signal at a repetition rate of 0.5 Hz. RF front-end hardware and FPGA-based detector system are presented. An algorithm implemented in the software part is described.

Hardware and Software

RF Front-End

The amplitude measurement uses RF diode as a linear detector. The phase detection is designed to measure the phase differences between the pulsed RF and a cw RF reference line of the linac. Both of these signals have the same frequency. In the phase measurement, a double balanced mixer (DBM) is used as a phase detector.

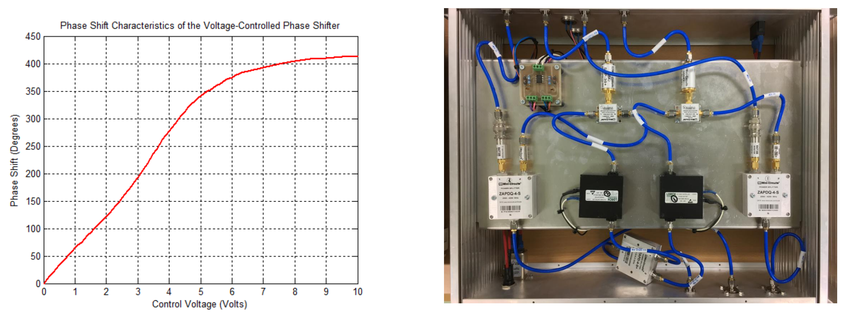

Figure 1: (left) Phase shifter characteristics and (right) RF chassis.

FPGA-Based Detector System

Xilinx's ML605 featuring featuring a Virtex-6 XC6VLX240T FPGA is chosen to be a main controller. Analog Devices' EVAL-AD7656-1SDZ and its FMC adapter board are selected. It has 6 channels ADC with a resolution of 16 bits each. Maxim Integrated's MAXSPCSPAR-TAN6+ board is chosen. It features a MAX5135 4-channel 12-bit DAC with SPI interface and available FMC connector.

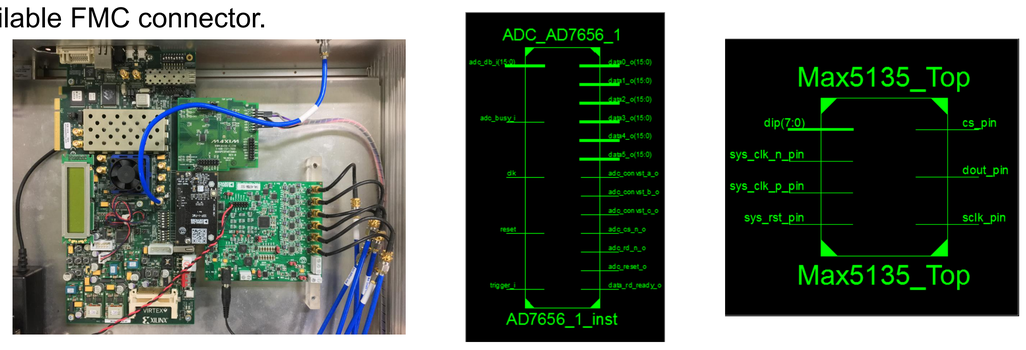

Figure 2: (left) ML605 FPGA board with AD7656-1 and MAXSPCSPARTAN6+ daughter boards, (middle) AD7656-1 driver IP, and (right) Max5135 logic block.

One custom IP block is designed using VHDL for ADC interface. It is designed with a finite state machine (FSM) so that all interface signals meet technical timing requirements. MAX5135 DAC block has a simple SPI interface. Both logic blocks are implemented in Xilinx's EDK.

System Integration

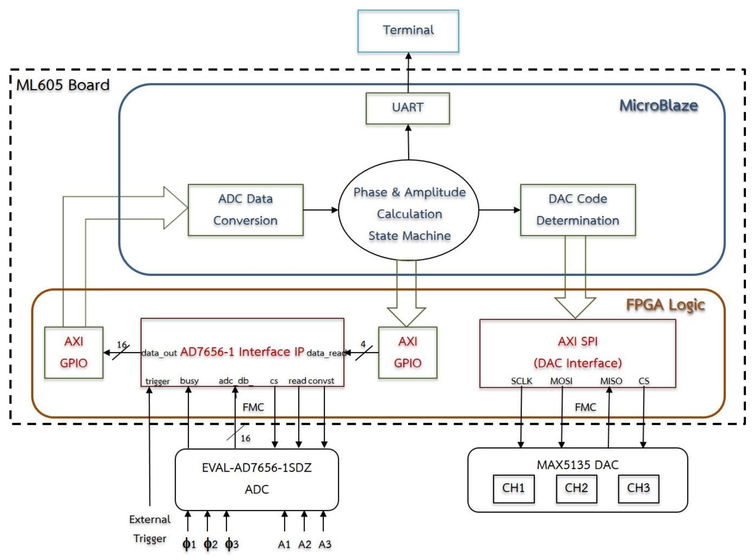

Figure 3: System block diagram for one ML605 board.

Six phase and amplitude signals are assigned to the ADC board. ADC Data Conversion and DAC Code Determination blocks are performed in the MicroBlaze processor. These two blocks are used to manage and control the signals and data flow between the FPGA logic and the main phase and amplitude calculation algorithm. AD7656-1 Interface and AXI SPI IPs are implemented to connect to the ADC and DAC, respectively, via FMC connectors. External trigger signal is used to determine when to sample the data. Two AXI GPIO IPs are used to connect to the AD7656-1 Interface IP, one is used to select the ADC channel and the other is used to receive the 16-bit ADC data.

Software

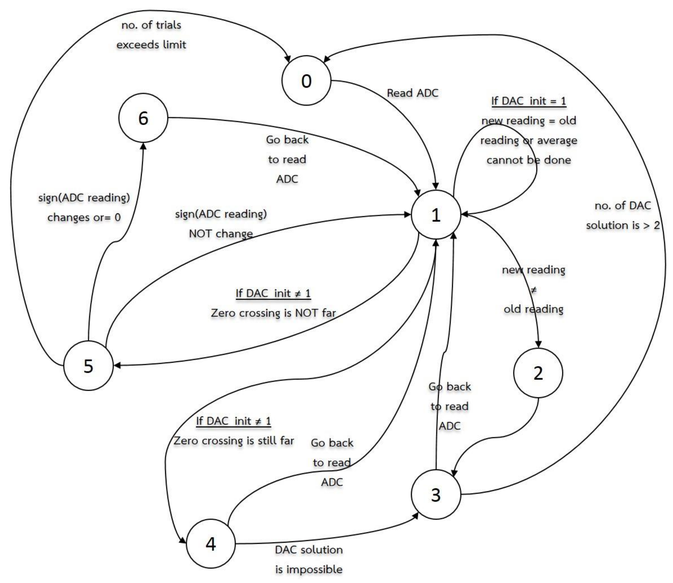

Figure 4: State machine diagram for phase calculation.

Amplitude calculation is obtained by simply multiplying by the attenuation of the RF line. The main part of the phase calculation is to find the correct zero crossing point of the DBM output and the slope in its vicinity once the DAC outputs the selected DC voltage. The detail of the implemented algorithm can be further explained in a state machine diagram.

State	Description
0	Initial state, set DAC output to 0 volt.
1	Read ADC data.
2	Find 2 DAC solutions from phase shift characteristics and compare to the ADC data.
3	Set DAC to output the DC voltage (0-10 V) to each solution. Then, verify the result from reading ADC data again.
4	Check if the DAC output is indeed the true phase solution (near the zero crossing point).
5	Search for the zero crossing point.
6	Determine the phase solution by interpolation, if necessary.

System Performance and Conclusion

Interface between ADC and FPGA was first tested in order to achieve correct data and timing requirements. The result shows that the system meets timing requirement and provides correct data for all six ADC channels. For each triggering instance (0.5 Hz), the algorithm can manage to make one transition from one state to the next but all six channels can be processed simultaneously. The result shows that, from starting at state 0, the algorithm needs at least 12 pulses to successfully calculate the phase. In the C program, DAC output is 8 times the DAC unit (8×(360°)/2^12), which contributes to a measurement resolution of ±0.703°. With the zero crossing search algorithm, the error becomes slightly less by using interpolation. The phase calculation algorithm can perform satisfactorily in the laboratory. The digital logic blocks and custom IP generated using VHDL enable concurrent operation and interface with a multi-channel simultaneous-sampling ADC and DAC.

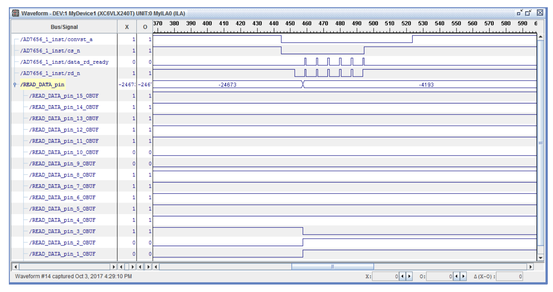

Figure 5: : Interface signals and data bus between FPGA and ADC.

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