Recent Update of the RIKEN RI Beam Factory Control System

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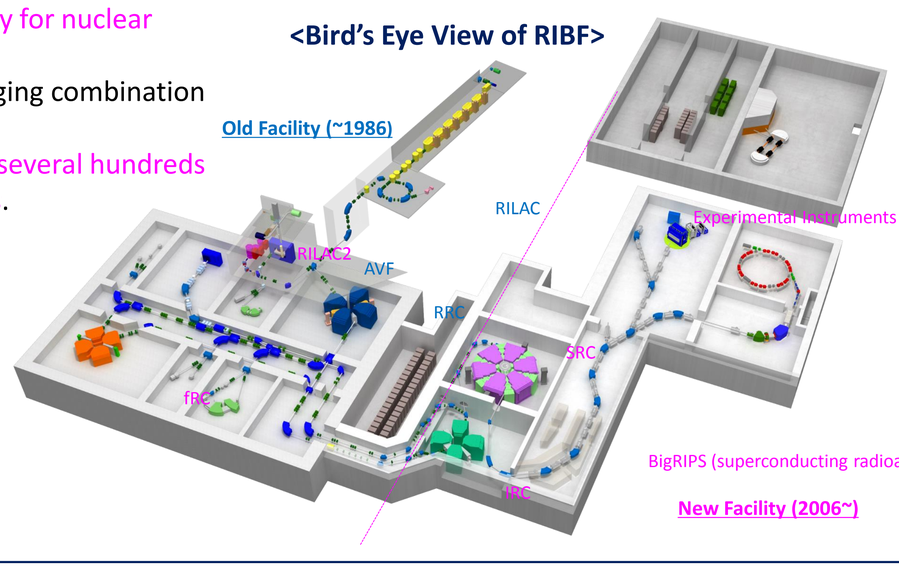
Introduction of RIKEN Radioactive Isotope Beam Factory (RIBF) and its accelerators

☆RIBF is a cyclotron-based heavy-ion accelerator facility for nuclear science.
☆Various acceleration modes can be achieved by changing combination of the accelerators used.
☆RIBF accelerators can supply RI beams at energies of several hundreds MeV/nucleon over the whole range of atomic masses.
Ex.) 345-MeV/nucleon ^{238}U beam of 58 pnA
345-MeV/nucleon ^{48}Ca beam of > 700 pnA

<RIBF Accelerators>
- Frequency-variable RIKEN heavy-ion linac (RILAC, 1980)
- New linac injector (RILAC2, 2010)
- K70-MeV AVF Cyclotron (AVF, 1990)
- K540-MeV RIKEN Ring Cyclotron (RRC, 1987)
- K570-MeV Fixed frequency Ring Cyclotron (fRC, 2006)
- K980-MeV Intermediate stage Ring Cyclotron (IRC, 2006)
- K2600-MeV Superconducting Ring Cyclotron (SRC, 2006)

<Bird's Eye View of RIBF>



<Research Activities by using RIBF>

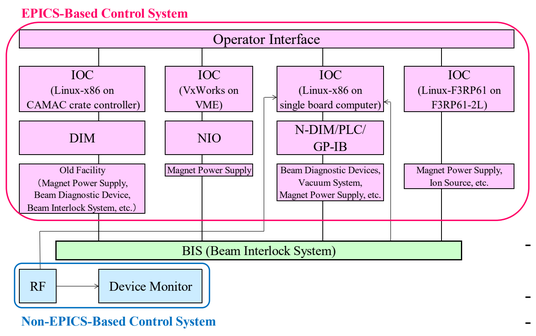
☆ Nuclear Physics Research
Studying new nuclei and exploring the mysteries of the universe and matter

☆ Discover of New Elements
Discover of the 113th element. First in Japan to discover a new atomic element

☆ Applied Research (Radiation Biology, RI Applications)
Conducting heavy ion beam breading using accelerators

Introduction of RIBF control system

☆Major Parts of the RIBF accelerator complex except RF systems are controlled by EPICS.
☆All the essential operation datasets of EPICS and other control systems are integrated into the EPICS-based control system.
☆Two types of interlock systems that are independent of the accelerator control systems are in operation;
- Radiation safety interlock system for human protection
- Beam interlock system (BIS) for hardware protection



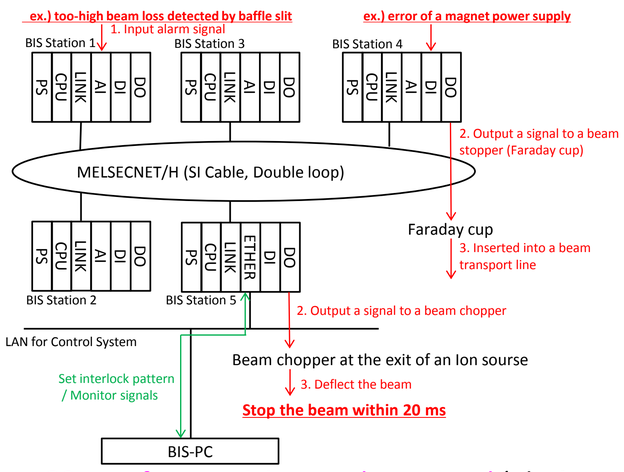
IOC	Number of IOCs	Number of Controlled Devices
CC/NET	5	~ 400
VME	7	~ 500
ALIX	33	~500
F3RP61	17	~100

- CC/NET : Commercially available network CAMAC crate controller of Toyo Corporation
- ALIX : Linux-based small single board computer
- F3RP61 : Linux-based PLC-CPU, on which EPICS programs are executed

Introduction of the Beam Interlock System (BIS)

< Purpose>
- Protect the hardware of the RIBF Accelerator Complex from potential damage from the high-power heavy-ion beams (> 10 kW).

< System>



- Stop beams >20 ms after receiving an alarm signal (design value : 10 ms) by using a beam chopper at the exit of the ion source
- Based on the programmable logic controllers (PLCs) manufactured by Mitsubishi Electric Corporation (Melsec PLC)
- 2006~ in operation
- All of the interlock signals are connected to the PLC-I/O modules
- All signal information is summarized in "BIS Station 5" that contains an Ethernet module for communication with the BIS-PC.

☆In order to secure response speed required by BIS, two BISs were introduced for old and new facility, respectively. The two BISs have the same system with the same configuration.
☆Each BIS has ~300 DI, ~70 AI and ~30 DO signals.

<Photos of BIS station-5>

Type	Product	Note
CPU	Q02HCPU	Sequence CPU
DI Module	QX41	
DO Module	QY40P	Transistor contact
AI Module	Q68ADV	
Melsecnet/H Module	QJ71LP21-25	
Ethernet Module	QJ71E71-100	

<Melsec modules used for BIS>

< Important function of BIS>
➢ There are two ways of setting BIS signals.
☐1. Set patterns of the input signals (ex. mask, alarm levels) and information on the signal output destinations individually for each input signal from BIS-PC.
☐2. Download one of the various interlock condition files in which the interlock signal pattern and alarm levels are specified and prepared in advance for each experiment from BIS-PC.
➢ When BIS detects an alarm signal of a component used in beam acceleration, BIS also inserts a beam stopper (Faraday cup) specified in the interlock condition file and installed upstream of the problem component. After inserting the relevant beam stopper, the beam chopper can be switched off and beam delivery resumed up to the inserted beam stopper. This feature is especially useful during beam tuning because beam tuning is conducted in a step-by-step manner, from an injector to a final-stage accelerator. The inserted beam stopper can be extracted from the beam line after the problem is fixed.

Development of the next-generation Beam Interlock System (BIS2)

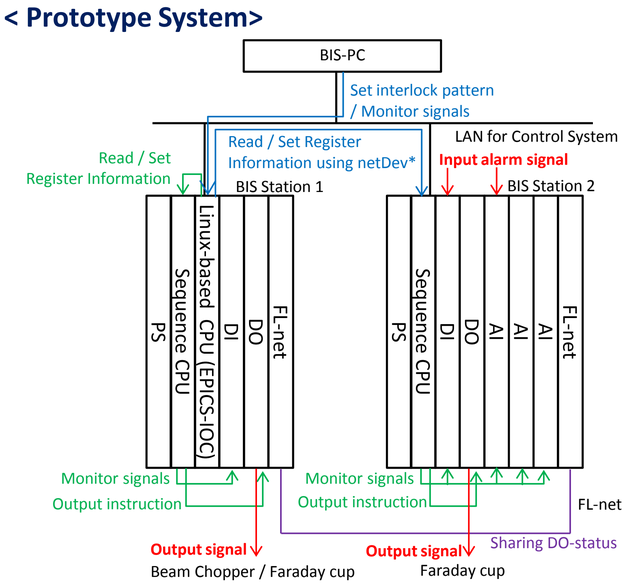
< Background of development and purpose>
- Beam operation at the level of several tens of kW is expected in the near future.
- To handle higher-power beams more safety, a much higher response speed is required of the BIS.
- It will be necessary a greater number of components than those included in the present BIS.
- There is a limit to how high the response speed can be increased to by increasing the associated components in the existing BIS.

Development of the BIS2 was started in 2016, which is designed to have more advanced performance and convenience compared to BIS.

< Design of BIS2>

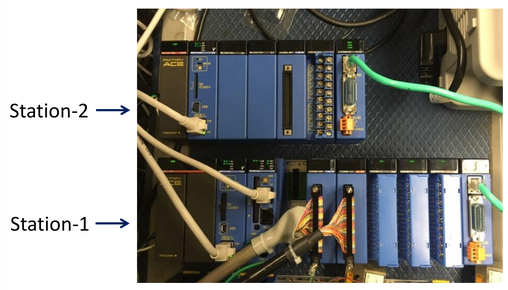
BIS2 implements interlock logic that is fundamentally equivalent to those of the existing BIS.
Based on the operation experience of more than 10 years of BIS;
- All the development of BIS2, such as module selection and program development, should be performed by ourselves from scratch.
- Reducing the amount of data shared between different stations is essential in BIS2 in order to reduce the time to stop the beam after receiving the interlock signal. Only the output signal status is shared among stations in BIS2.

< Prototype System>



Blue line : communication via Ethernet
Green line : communication via PLC-bus
Purple line : communication via FL-net
netDev : program developed by the control group of KEK and RIKEN Nishina Center in 2004 aiming at controlling various kinds of PLCs and the in-house controller developed by the RIEKN Nishina Center

<Hardware constitution and process flow in BIS2>
- Based on the PLCs manufactured by Yokogawa Electric Corporation (FA-M3)
- All of the interlock signals are connected to the I/O modules
- Multi-CPU configuration using a Linux-based PLC-CPU on which EPICS programs can be executed in addition to a sequence CPU. Interlock logic is implemented in the sequence CPU because high-speed processing and high reliability are required. Such high-speed processing is not necessary for setting and monitoring the interlock signal; these functions are implemented in Linux-based CPU. We execute EPICS on the Linux-based CPU and access it from the upper-level PC in the control room via Ethernet.
- Interlock signal information transfer between two stations is performed through FL-net—an open network protocol used for interconnection between controllers.



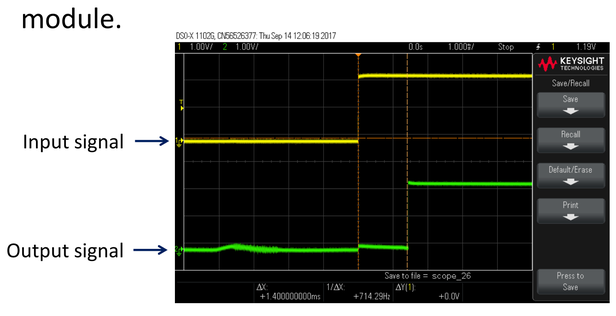
<Photos of BIS2 prototype>

Type	Product	Note
CPU1	F3SP71-4S	Sequence CPU
CPU2	F3RP61-2L	Linux-based CPU
DI Module	F3XD32-3F	
DO Module	F3YD14-5A	Transistor contact
AI Module	F3AD08-1V	
FL-net Module	F3AD08-1V	Transmission speed : 10 Mbps

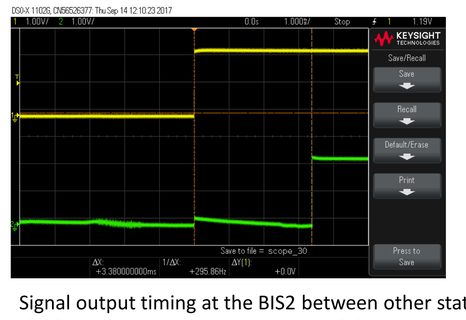
<FA-M3 modules used for BIS2>

< Performance tests of BIS2 prototype>

Simulating the application of BIS2 prototype to the AVF cyclotron and its low-energy experiment facility, we registered 18 DI, 0 AI and 7 DO signals to the I/O modules in station-1, and 25 DI, 23 AI and 0 DO signal to the I/O modules in station-2.
✓ BIS2 prototype outputs signals correctly when changing the pattern of the input signals.
✓ Measurement of the signal transmission speed in the system. In our case, the transmission data size between the two stations via FL-net is designed to be 4 words for the link relay area and 0 word for the link register area at the FL-net module. Sampling period of the input signal is set to minumum at the DI module.



Signal output timing at the BIS2 within the same station
(1.40 ms, Average response time : ~ 1.4 ms)



Signal output timing at the BIS2 between other stations
(3.38 ms, Average response time : ~ 3.8 ms)

< Results and Next>
✓ Time used for data transmission through the FL-net is 2.4 ms, which is consistent with the specification listed in the catalog.
✓ The measured response speed is greater than the specification requires in BIS2 development.
✓ We have started a test using EtherCAT instead of 10-Mbps FL-net expecting higher speed performance.