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LIA-20 EXPERIMENT PROTECTION SYSTEM

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Abstract

In Budker Institute of Nuclear Physics (BINP) is being developed an electron linear induction accelerator with beam energy 20 MeV (LIA-20) for X-ray flash radiography. Distinctive feature of this accelerator in protection scope is existence both machine, person protection and experiment protection system. Main goal of this additional system is timely experiment inhibit in event of some accelerator faults. This system based on uniform protection controllers in VME form-factor which connected to each other by optical fiber. By special lines protection controller fast receives information about various faults from accelerator parts like power supplies, magnets, vacuum pumps and etc. Moreover, each pulse power supply (modulator) fast send its current state through a special 8 channel interlock processing board, which is base for modulator controller. This system must processing over 4000 signals for decision in several microseconds (less than 50 us) for experiment inhibit or permit.

INTRODUCTION

LIA20 – is an electron linear induction accelerator for X-ray flash radiography with energy up to 20 MeV and 2 kA beam current. It will produce three pulses (two short and one long) in one shot and divide the long pulse on nine parts for researching an experiment object from nine directions. A final radial beam dimension after lens correction will be 1 mm. LIA20 is an evolution of a LIA2 [1] which was designed as injector on energy 2 MeV for big accelerator.

The experiment is very expensive and has long preparation time therefore LIA20 should has a special experiment protection system (EPS). This system should inhibit start of the experiment when accelerator does not operate in normal mode. An accelerator structure defines some specific parameters for the experiment protection system. First, reaction time on accelerator malfunction should be less than 50 us for inhibit experiment in time. Secondly, total accelerator length with a beam dividing hall is approximately 150 m., therefore optical lines for protector devices are necessary. LIA 20 has many systems with a big quantity of units thus protector device should be multi-channel (16 or more).

EXPERIMENT PROTECTION SYSTEM

The experiment protection system based on a specific VME designed modules – preventers. It's a 6U height VME module with channels for receiving signals from devices or another preventers. This module based on FPGA controller with capability of adjusting inner parameters. All preventers and devices connected together via special "workability" channels. Each preventer has 8 "workability" channels on its front panel and this number can increase up to 24 by installation a 16-channel rio-module. Also preventer has one "workability" channel for connecting to another preventers, one CAN channel and special channel for connecting bus with modulator controllers so-called "fault-bus".

Logic Structure

Experiment protection system general structure is represented in Fig.1. It's a "star" network with a three layers – low, middle and high.

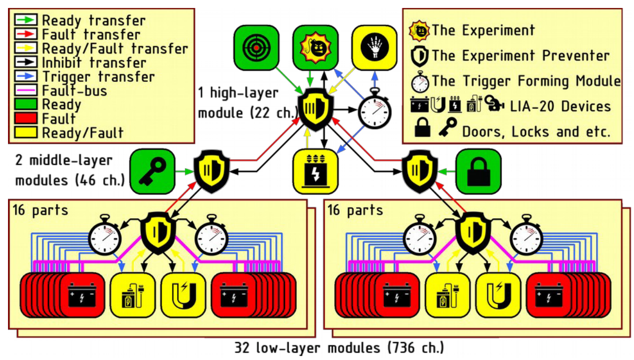

Figure 1: LIA20 EPS logic structure.

There are 32 preventers on a low layer of the network, which are located in a regular VME crates. This preventers are collect signals from devices (degausser, HV charger, lens power supply, thyratron heating unit and etc.) over "workability" channels and from modulator controllers over special "fault-bus". They send a "fault" signal to middle-layer preventer after processing all "workability" channels. There are two preventers on the middle-layer. They can receive signal not only from low-layer preventers but from not regular devices or system, for example, from doors, locks or another devices from personal safety system. In its turn middle-layer preventers send "fault" signal to single high-layer preventer, which are located in the central VME crate. Also this terminal preventer receive "workability" signals from a cathode heating power supply, vacuum and gas system, target and detector system. Main goal of this preventer (and whole system) is inhibit experiment start unit and inhibit its trigger signal when something wrong in accelerator or detector system.

How was mentioned above the preventer and devices are connected together over "workability" channels. Every "workability" channel consist of three lines – "ready" signal transfer line, "fault" signal transfer line and "inhibit" signal transfer line. A device ready for work when it already done all preparatory procedures (heating, charging, "cold" turning-on and etc.) and waits external events, which define device further behaviour. The device transfers "fault" signal when it cannot working in normal mode. If device receive an inhibit signal it must be stopped in safe manner all work.

A device final malfunction is defined on a "fault" signal and a "ready" signal received in time. A "fault" signal has

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influence on a result of an interlock processing procedure asynchronously. A device readiness is checked synchronously with trigger signal or with “ready” signal from another devices. For example, device A should be already ready for work when device B will be send “ready” signal. If this was not happened, the system will decide that device A is faulty and will produce proper inhibit actions.

Trigger and Device Inhibits There are two general inhibit actions. First of all, the experiment protection system can send “inhibit” signal over “workability” channel to devices which should be turning-off. Secondly, the system can inhibit trigger pulses for devices starting. Each trigger forming module has four lines DZ0-3 for inhibit its outputs. A trigger output can be configured that it will be inhibited from one selected DZ line.

A basic structure of “ready” and “fault” signals processing are represented in Fig. 2. Final “fault” register consist of two parts – primary “fault” which was received from device over “workability” channel and secondary “fault” which was produced by checking “ready” signals on a defined times. Time moments at which device readiness was checked are defined by TTL[1] pulses (falling edge) and/or “ready” signal from another devices (transition from “not-ready” to “ready”).

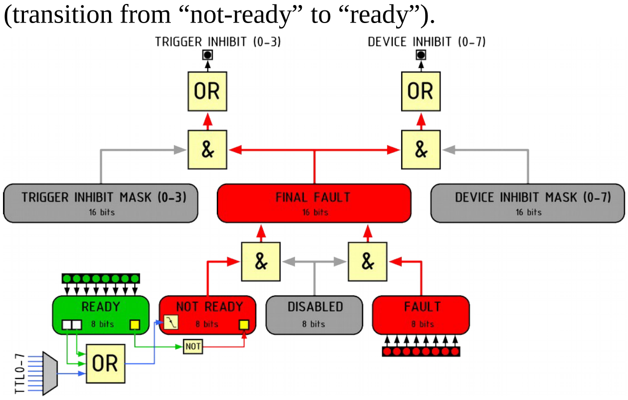

Figure 2: “Ready” and “fault” signals processing.

If a device is disabled by setting corresponding bit in a special register, its “workability” signals will be ignored and its “inhibit” signal will be in an active state. A “fault” value are latched in the register and multiply with masks by AND scheme for further processing. A trigger inhibit circuit has four masks since trigger forming module has only four DZ lines for blocking output signals. A device inhibit circuit has as many masks as “workability” channels. Masks and the final “fault” register have a double size as compared with primary receiving register of “fault” or “ready” signals. After masking all bits of “fault” value are added together by OR scheme for producing the “inhibit” result.

Physical Interpretation

“Workability” channel can be implemented in “copper” or optic realization. Channels that join preventers in one network are optic, another channels for connecting devices are “copper”. For this purpose one of the “workability” channel of the preventer is optic.

Copper Version There are two optocouplers for “ready” and “fault” signals receiving and one optocoupler with photo-transistor output for “inhibit” signal transmit. This approach allow to save galvanic isolation between channels and don't need with DC/DC converter on each channel. But disadvantage of this decision is larger transition time (3 us) to transmit the “inhibit” signal than receiving “ready” or “fault” signals from an input (1 us). A light presence in the optocoupler from an input diode means that device is ready for work (for “ready” signal), malfunction is a light absence (for “fault” signal) and vice versa. If photo-transistor of the “inhibit” output is in “on” state it means that an “inhibit” signal in active and device should stops all work in safe manner with latching its state. The device can use its “inhibit” input with “dry” door contacts connected in sequence for personal safety organization.

Optic Version Optic realization of “workability” channel has only two lines – “fault” transmit and “inhibit” receive. This lines totally identical and differ only direction. This lines transfer constant level in a simple version of communication between two preventers. There are no faults if preventer send light over optic line and it not produce “inhibit” signal when receiving light. In more complicated version preventers can communicate with each other by sending and receiving bite sequences with baudrate up to 10 Mb/s.

“Fault-Bus” A special bus are used for receiving a “fault” signal from modulator controllers since there are 16 identical modulator controllers for one preventer. If every controller are connected to individual channel then number of all channels will be hugely increased. Therefore, all modulator controller are connected with each other and the preventer via the special “fault-bus”.

The “fault-bus” is based on CAN physical layer [2]. There are two levels on a CAN-bus – dominant and recessive. The dominant level on in terms “fault-bus” means “fault” and recessive level means normal device operating. All modern CAN drivers have a time-out on dominant level transmitting that exclude possibility of sending constant dominant level on the bus. Therefore, “fault” signal is transmitted by long dominant level (less then time-out) and very short recessive level for restarting a time-out timer. Another device on the bus filters line by capacitor and receive only the dominant level. For implementing the CAN physical layer a modern NXP driver TJF1051 is used with baud rate up to 5 Mb/s.

Simple “Fault” Line For redundancy every modulator controller has a simple “fault” line that is implemented on “inhibit” line scheme. All 16 controllers and the preventer are connected together by a “ring” topology in which preventer generate current over this simple “fault” line. If any controller switches-off an output photo-transistor then preventer will receive a “fault” signal.

Modulator Controller as an EPS Unit

A special controller (CoMoD) was developed for accelerator modulator since modulator is a basic unit of a pulsed power supply system. LIA20 uses 512 modulator

[1] TTL lines are located on a BINP-VME crate backplane and connecting together all module. Timer module produces pulses over TTL lines for slow synchronization.

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with his controller. One of the important functions of this controller is inform preventer about a modulator failure. The controller is based on 3U eurocard interlocks processing board (IPB in Fig. 3). IPB is a smart board with FPGA Lattice LCMX02-200HC and Renesas microcontroller UPD78F1035 which operate under FreeRTOS. IPB has 12 slots for small terminal modules :

- 2 modules with DAC based on 8-bit PWM (not used in CoMoD);
- 8 analog input modules with a comparator (160kHz bandwidth);
- 2 digital modules with 4 isolated inputs (not used in CoMoD);
- 2 digital modules with 4 isolated outputs;

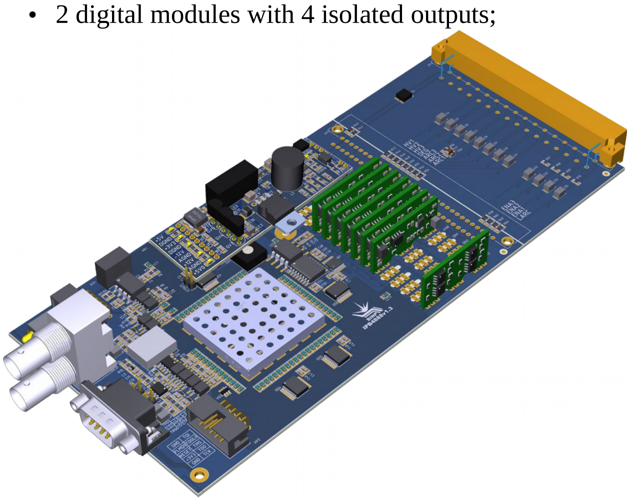

Figure 3: IPB 3D model.

For CoMoD purposes the IPB has only 7 analog input modules and one digital output module. In addition, it has 8-channels 12-bit ADC with 500kHz conversion rate and 512 kB SRAM for signal saving. IPB has two I2C potentiometers for adjusting threshold voltage levels for comparators on analog modules. This board collects information about voltages on PFN lines, thyratron arc current and thyratron heater voltage and degausser current.

IPB checks all input analog signals after digital filtering by using time-gates which started by an external trigger. The controller can produce only “fault” signal over “fault-bus” and over simple “fault” line. Reaction time on an abnormal signal is 1 us over “fault-bus” and 3 us over simple “fault” line.

CONCLUSION

Designing of modulator controller already is finished and more than one hundred devices were produced. An experiment preventer which is main unit in experiment protection system was prototyped and will be test in a real machine.

Now in BINP an accelerator injector on 2 MeV and several accelerating modules with all necessary systems are assembled together for testing purposes. Test results will be obtained in the beginning of 2018 year.

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