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A TIME STAMPING TDC FOR SPEC AND ZEN PLATFORMS BASED ON WHITE RABBIT

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Abstract

Sub-nsec precision time synchronization is requested for data-acquisition components distributed over up to tens of km^2 in modern astroparticle experiments, like upcoming Gamma-Ray and Cosmic-Ray detector arrays, to ensure optimal triggering, pattern recognition and background rejection. The White-Rabbit (WR) standard for precision time and frequency transfer is well suited for this purpose.

We present two multi-channel general-purpose TDC units, which are firmware-implemented on two widely used WR-nodes: the SPEC (Spartan 6) and ZEN (Zynq) boards. Their main features: TDCs with 1 nsec resolution (default), running deadtime-free and capable of local buffering and centralized level-2 trigger architectures. The TDC stamps pulses are in absolute TAI. With off-the-shelve mezzanine boards (5ChDIO-FMC-boards), up to 5 TDC channels are available per WR-node. A SPEC-TDC design with 0.25 nsec resolution is currently in exploration. The TDC units are under test for long-term performance in a harsh environment application at TAIGA-HiSCORE/Siberia, for the Front-End DAQ and the central GPSDO clock facility.

INTRODUCTION

Time measurement of sub-nsec precision is required in modern astroparticle experiments like Cosmic Ray, Gamma-Ray and High Energy Neutrino Telescopes, with sensor units distributed over large area and operating under harsh conditions. The White Rabbit (WR) technology for precision time and frequency transfer [1] offers technical performance parameters, adequat for this task.

White Rabbit is in use in an astroparticle experiment since 2012 [2, 3]. This WR-installation in the TAIGA Gamma-astronomy project [4, 5] aimed to supply precision timing to the distributed Air-Cherenkov detectors, and also served as a WR test-bed. In-situ nsec-performance-verification was an essential part of the system design.

After very positive experience [6] we proposed White Rabbit as the time-distribution system for the next generation Gamma-Ray Observatory, CTA [7, 8]. WR has numerous advantages compared to custom-made solutions, most noticably avoiding the substantial design, verification and maintenance effort for custom-made solutions.

Conceptually, WR offers a standard way to transport a precision clock over a network of WR-devices, via WR-switches from a central time-master to distributed WR-nodes (the 'WR endpoints'), see e.g. [1, 3]. These WR-nodes can either be (1) standalone WR-devices, or (2) have the WR-functionality integrated directly into the user-hardware.

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In this paper we follow option (1), which implies an exchange of signals between the WR-node and the user hardware (e.g. DAQ-components of a Telescope, or a detector station in a multi-component setup). It is convenient to rely on standard off-the-shelf WR-devices, which only need to be firmware-adapted for the specific functionalities (and eventually, equipped for with trivial signal-level adapters); since this minimizes development of new hardware.

In this paper, we present the design of a new universal multi-channel TDC for two types of popular commercial WR-nodes - the SPEC [9, 10] and the ZEN card [9]. We developed

- a deadtime-free 4-channel TDC with 1 nsec resolution on the SPEC and ZEN, and
- a TDC designed for improved time resolution up to 0.25 nsec.

These TDCs are also useful for efficient and flexible monitoring of the timing system functionality, as will be discussed.

EXTENSION OF THE 1 NSEC TDC

In [2] we presented a TDC based on the open source WR design for the SPEC in combination with the highly flexible DIO card. In this setup, shown in Fig.1, one signal of the DIO card is sampled with the in FPGA SERDES blocks and timestamped if above a certain adjustable threshold (a feature of the DIO card). We created for various applications firmware to run a time-precision DAQ, including dedicated IO-control [3]. A similar design has been implemented on the ZEN, see Fig.2).

4-Channel TDC

Due to the high flexibility of the DIO card all ports can be used as inputs. In our design we instantiated four TDC cores, each connected to one of the DIO input signals Each of the four TDCs is connected to a FIFO which keeps the timestamps until the CPU reads it and builds UDP packets. This implementation is realized in the SPEC and the ZEN node, (see e.g. Fig.3). While on the SPEC WR node the lm32 cpu is used to assemble the network packets the ZEN WR node the embedded ARM core is doing this job. The ARM core is connected to the WR core via an AXI-to-Wishbone Bridge. Due to the more powerful ARM core the trigger rate is by far higher than on the SPEC card. It is planned to use the Fabric Interface of the White Rabbit core to generate the packets without a CPU.

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High Resolution TDC

With the 4-channel TDC setup design, it is possible to increase the sampling frequency for a single input signal. This signal has to be split up into 4 with a simple fanout board and fed into the 4 TDC input channels of the DIO card (currently done by an external fanout; though a splitter can easily be implemented on the 5ChDIO). The FPGA design has been modified to delay the input signals in steps of 250ps, as shown in Fig.4. We note, that the IDELAY blocks of the Spartan 6 FPGA (on the WR SPEC node) are not temperature compensated, we therefore plan to implement the design on the Zynq based ZEN board as well.

A MULTI-CHANNEL NSEC-MONITORING SYSTEM

Based on the above described 4-channel TDCs, a field application at the TAIGA project was created. Figure 6 shows three SPEC boards (4-Chan-TDC) and one ZEN-board, which make up the central-clock nsec-monitoring facility, as part of the TAIGA DAQ [5]. Time-alignment of the WRS-network components is monitored by their PPS pulses (or WR-node derived), together with those from the primary GPS's and the GPSDO(Rb), as well as other TAIGA reference signals, as sketched in Fig.5. The advantage of the WR-based TDCs is their absolute time-scale (rather than referenced to a local common trigger signal, like "Common-Stop"), which allows to keep nsec precision for signals arriving at arbitrary times, on locations at large distances.

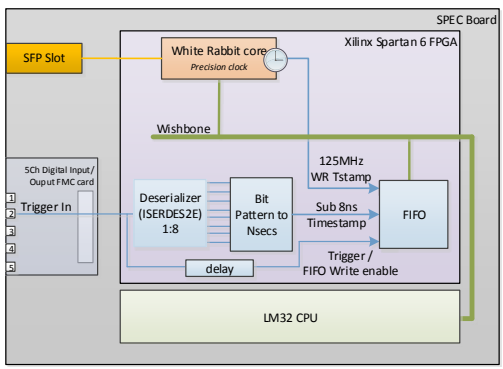

Figure 1: Modified SPEC firmware using the 5ChDIO card and the in-FPGA SerDes blocks. Timestamps are written into a FIFO read out by the LM32 CPU. The basic 1 nsec TDC design uses the ISERDES blocks of the FPGA and the White Rabbit timing system. Implemented are 1 TDC-channel with 1 nsec resolution, and 4 I/O lines for DAQ-control purposes [3, 12].

CONCLUSION

We are operating over several years a sub-nsec White-Rabbit timing system at the TAIGA facility - a km^2-scale Gamma-Ray facility with an Imaging Atmospheric Cherenkov Telescope and a large area Non-Imaging Cherenkov timing array. Nanosecond time-stamping of distributed trigger signals is done with custom-modified WR-nodes (SPECs) [3, 5]. Our experience confirms early expectations [6], that White Rabbit delivers the performance and reliablity required for precision time synchronization in large scale astroparticle projects like e.g CTA. Following the 1-TDC-SPEC concept [2], the SPEC has recently been

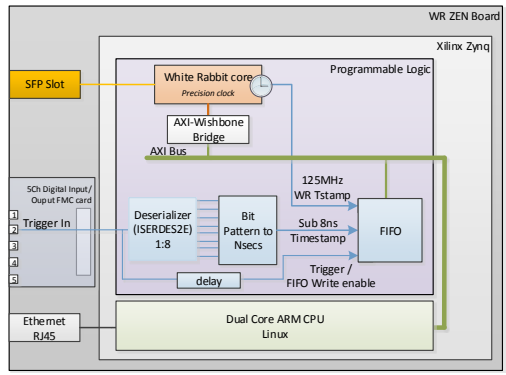

Figure 2: Modified ZEN firmware using the 5ChDIO card and the in-FPGA SerDes blocks. Timestamps are written into a FIFO read out by the ARM CPU (Linux).

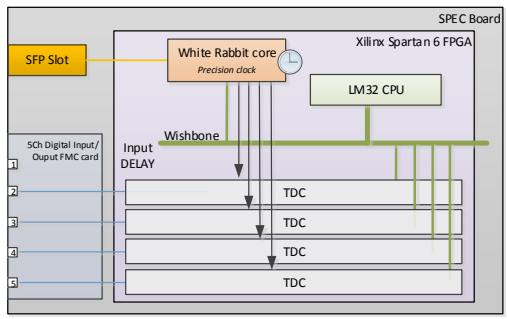

Figure 3: 4-Channel-TDC on the WR-SPEC and 5ChDIO card. Firmware schematics with TDC units to timestamp 4 input signals, with 1 nsec resolution each.

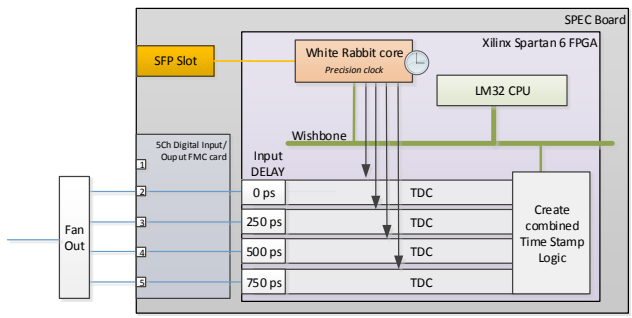

Figure 4: SPEC-based TDC for improved time resolution. FPGA IDELAYs with n×0.25nsec delay increase the resolution to 0.25 nsec (input split by an external fanout, implementation the 5ChDIO is possible).

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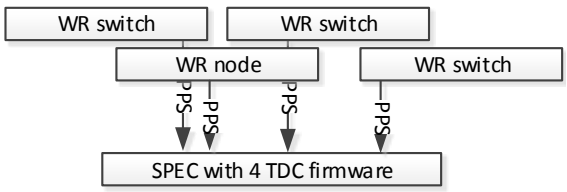

Figure 5: A simple use-case for the 4-channel-TDC: monitoring the WRS-PPS phase alignment of a group of WR-switches.

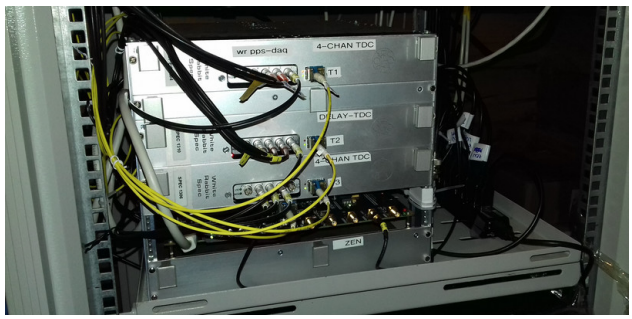

Figure 6: The 4-Channel TDC in application: nsec-monitoring of the TAIGA central timing system (GPS, GPSDO, WRS-Master and -network) by three 4-channel SPEC TDCs and a ZEN TDC.

adapted in [11] to fit formfactor and specific signal-level required by CTA.

We present in this work a universal 4-channel TDC module, that is based on firmware modification of standard WR-units (SPEC or ZEN). It shows excellent time-stamping performance, and provides deadtime-free multi-hit operation. Another SPEC-modificaton aiming at TDC performance with time-resolution of up to 0.25 nsec is under longterm study. Upgrade of the TDCs to larger channel density (8 or 16 TDC-chnnels per WR-node) is realistic, and only requires an upgrade of the cheap 5ChDIO-card.

These 4-channel TDC units allow for a flexible and cost-efficient design of precision timing setups: both for interfacing to experimental DAQ-components (like time-stamping of trigger signals issued by front-end DAQ units), as well as for monitoring any test-signals with nsec resolution (e.g to verify the performance of timing system itself). Routine operation of an additional medium size monitoring system started in fall 2017 at TAIGA, which also includes central GPSDO-based timing.

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