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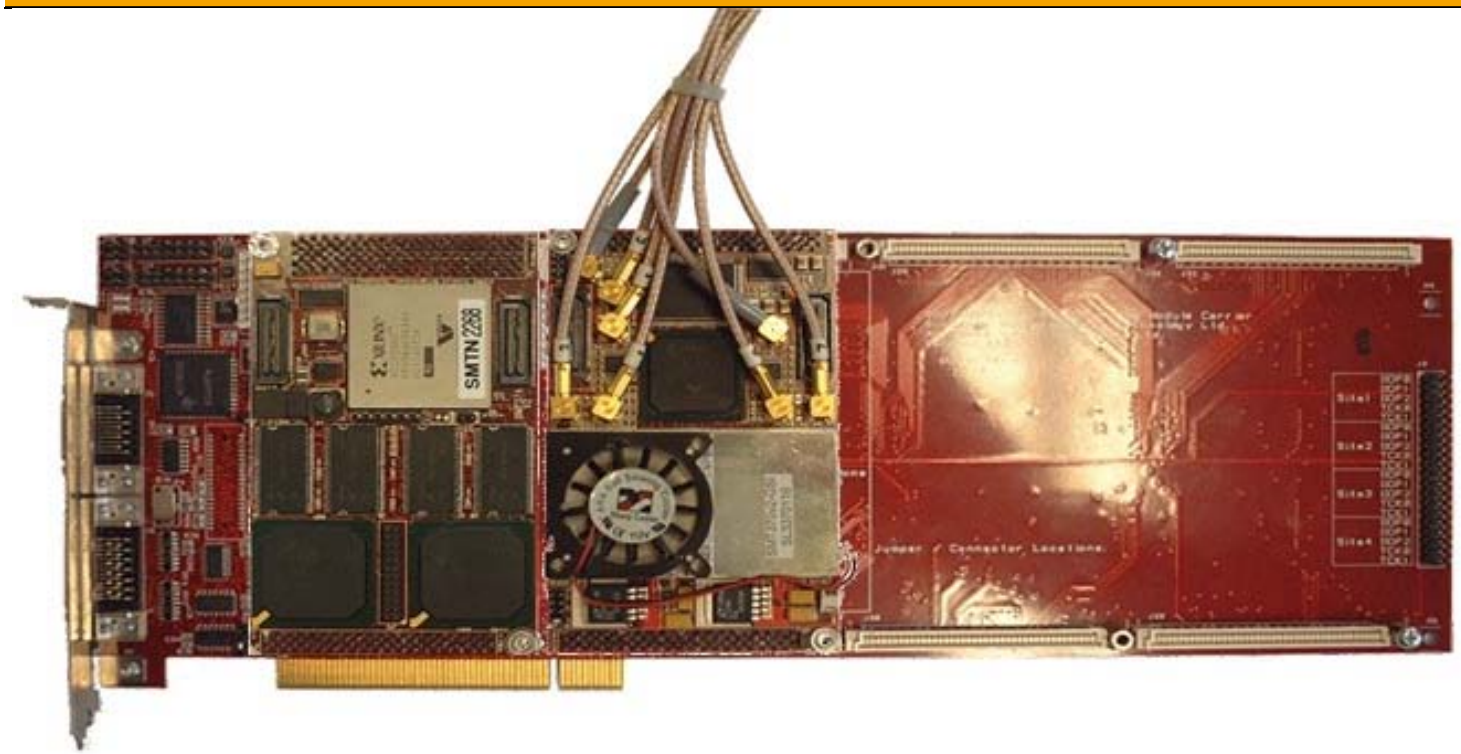
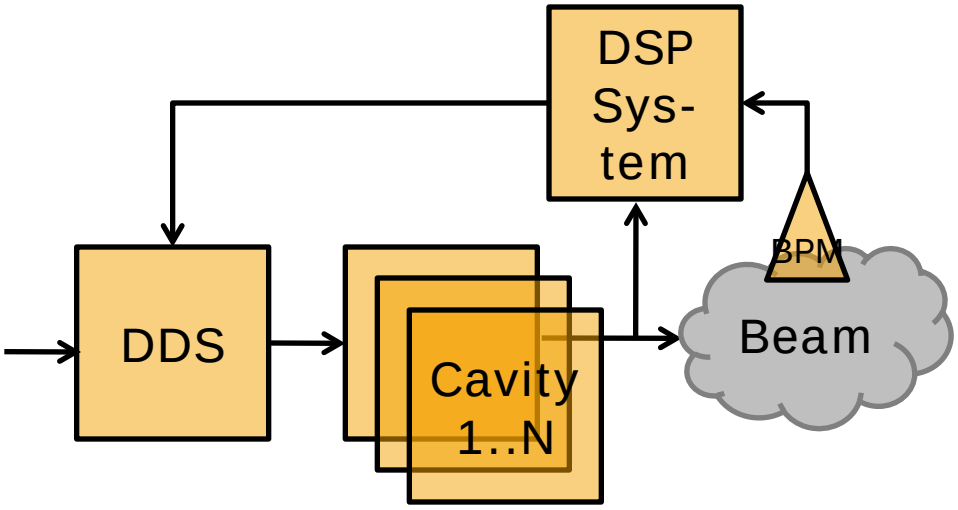
Floating-Point HW Accelerator for Phase & Magnitude Detection and Filtering in a Beam Phase Control System

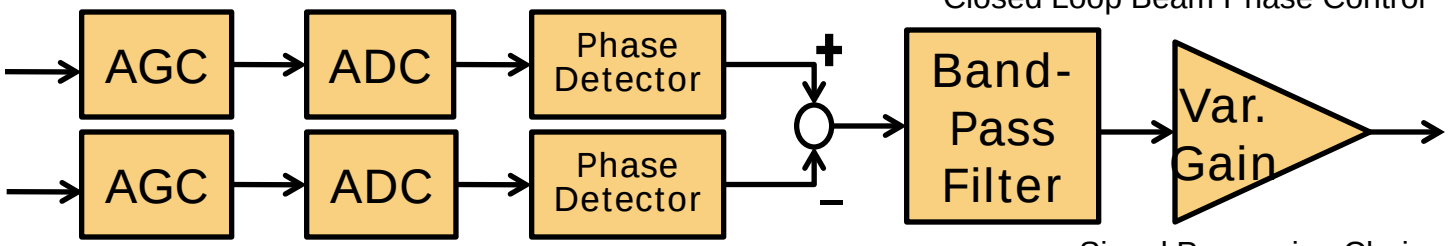


Application Overview

- We present a hardware accelerator for digital signal processing tasks in a beam-phase control system, such as
  - phase and magnitude detection,
  - frequency-adaptive filtering and
  - variable-gain amplification.



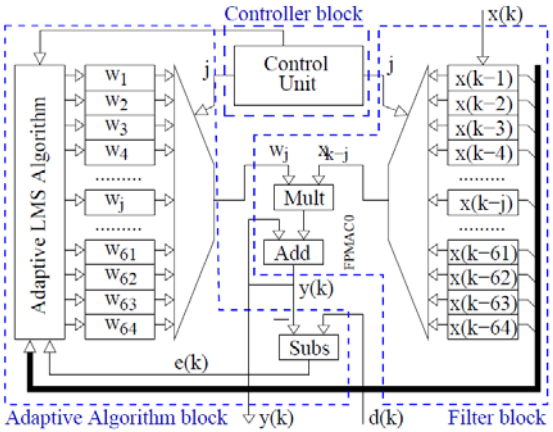
Closed Loop Beam Phase Control



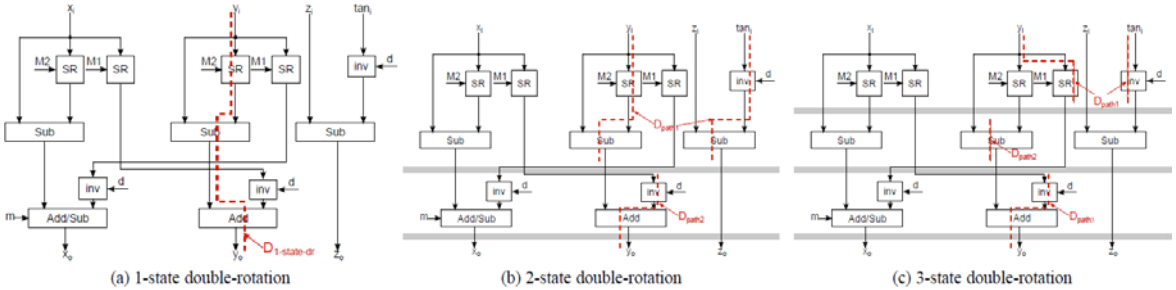
Signal Processing Chain

Hardware Architecture

- Our architecture primarily consists of
  - CORDIC-based phase & magnitude detectors
  - LMS-adaptive FIR filters
- All computation is performed in 32-bit floating-point arithmetic
  - to improve the precision and
  - to better deal with the large dynamic data range
- Different design alternatives have been investigated



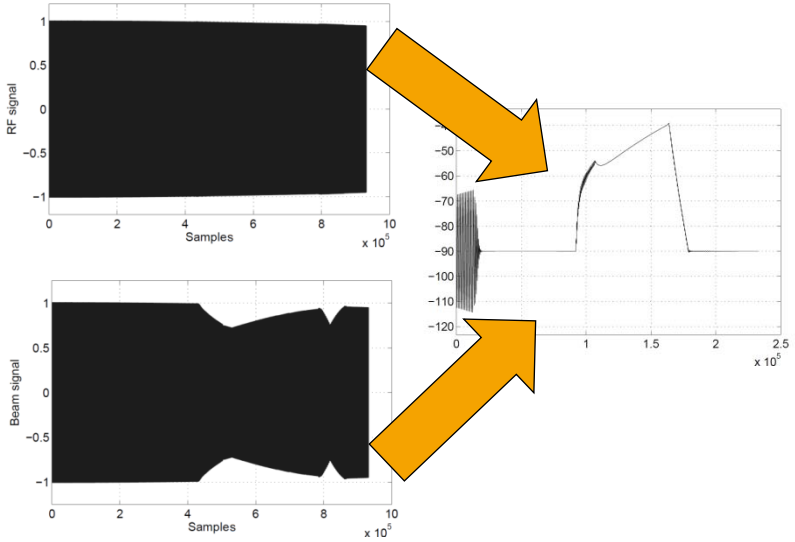
Adaptive FIR filter architecture



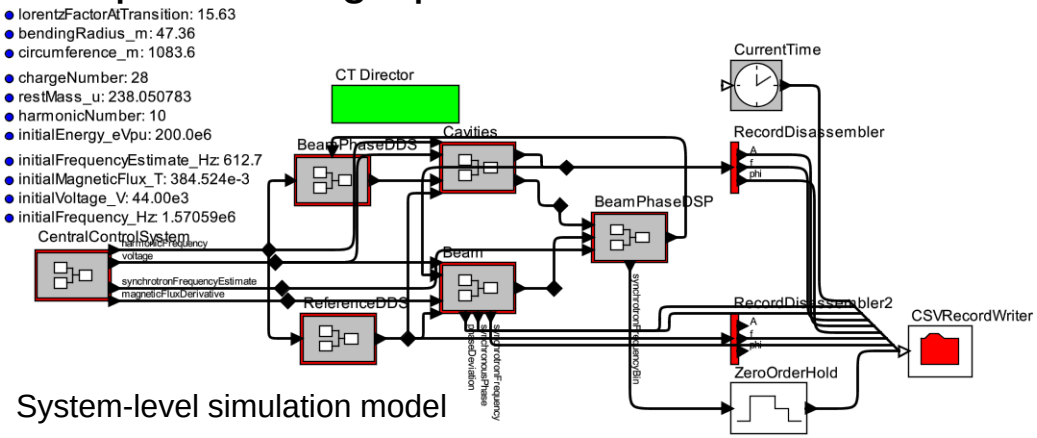
CORDIC architecture alternatives

Results

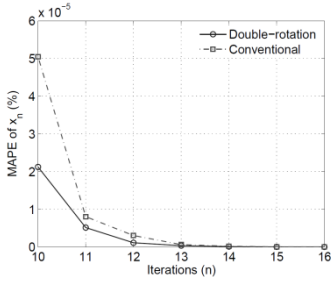
- We compared the output of our system against a reference model and determined the error
- We analyze the effect of different design parameters
  - on the output error and
  - on resource consumption and processing speed

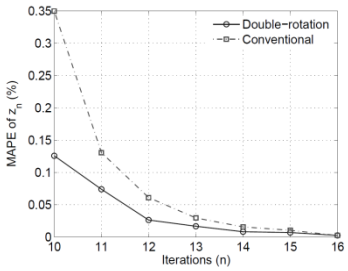


System Input and Output



System-level simulation model





Error vs. # of Iterations