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Floating-Point HW Accelerator for Phase & Magnitude Detection and Filtering in a Beam Phase Control System



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We present a hardware accelerator for digital signal processing tasks in

- a beam-phase control system, such as
- phase and magnitude detection,
- frequency-adaptive filtering and
- variable-gain amplification.

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Application Overview





Signal Processing Chain



Hardware Architecture

- Our architecture primarily consists of
 - CORDIC-based phase & magnitude detectors
 - LMS-adaptive FIR filters
- All computation is performed in 32-bit floating-point arithmetic
 - to improve the precision and
 - to better deal with the large dynamic data range
- Different design alternatives have been investigated



Adaptive FIR filter architecture





|x(k

Controller block



We compared the output of our system against a reference model

and determined the error

- We analyze the effect of different design parameters
 - on the output error and

CT Director

Bear

 on resource consumption and processing speed
Identification: 15.63

initialFrequency_Hz: 1.57059e6 Pro MAPE (CentralControlSystem 0.15 0 1 Bo 0.05 CSVRecordWriter 10 10 12 13 Iterations (n) ZeroOrderHold System-level simulation model

CurrentTime

RecordDisa

semble

BeamPhase

Results

bendingRadius m: 47.36

circumference m: 1083.6

restMass u: 238.050783

initialVoltage V: 44.00e3

initialEnergy_eVpu: 200.0e6

initialFrequencyEstimate_Hz: 612.7

initialMagneticFlux_T: 384.524e-3

harmonicNumber: 10

chargeNumber: 28





