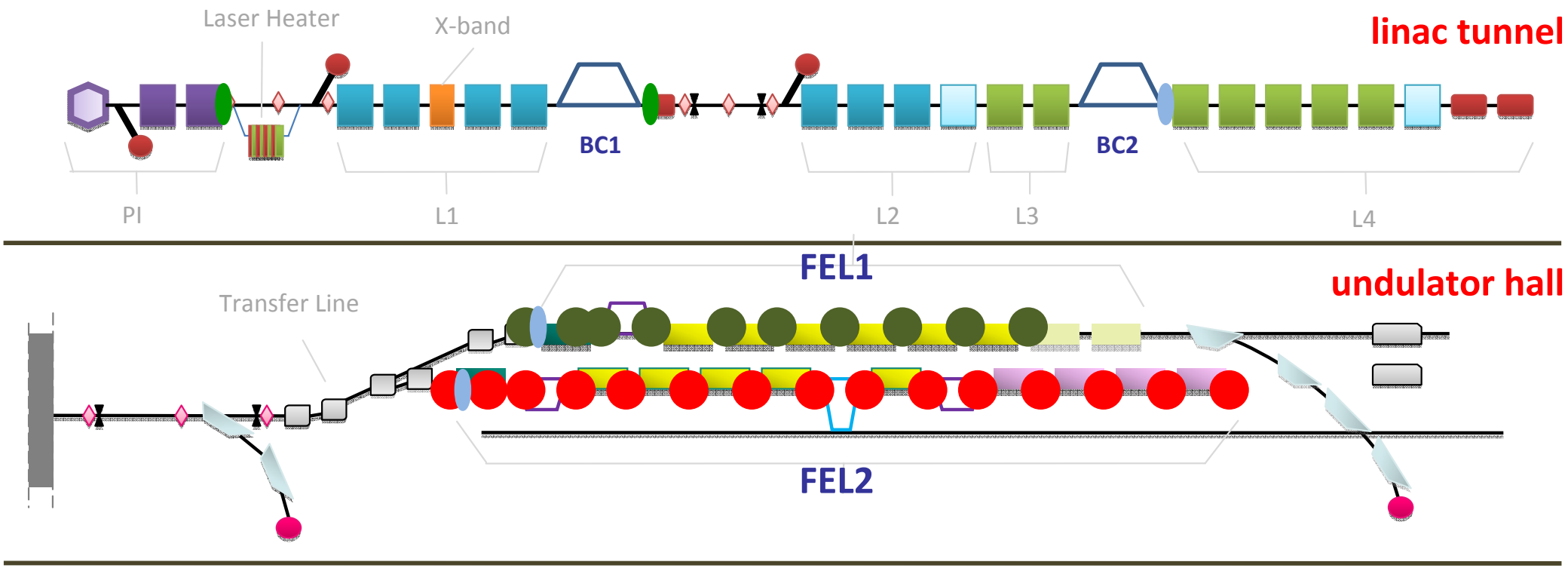
The MicroTCA Acquisition and Processing Back-end for FERMI@Elettra Diagnostics

A. Borga
on behalf of the Timing and Diagnostics
FERMI@Elettra Team

Outlook

- **FERMI@Elettra FEL project: Simple Machine Layout**
- **MicroTCA architecture for FERMI@Elettra:**
  - Diagnostics back-end electronics: system requirements
  - Diagnostics back-end electronics: necessary uTCA modules
- **Custom FERMI@Elettra MicroTCA modules:**
  - A|D|A, A|D|O, MiTiCH
- **Common gateware and software infrastructure**
- **FERMI@Elettra specific cases:**
  - The BAM case: from concept to results
  - The C-BPM case: from concept to results
- **Other MicroTCA related developments**
- **Our field experience with MicroTCA (joy and sorrow)**
- **Acknowledgements**

FERMI@Elettra: Simple Machine Layout



2 BAM stations installed	3 BAM stations to be installed
10 C-BPM stations installed	15 C-BPM stations to be installed

- **Diagnostics is crucial for electron beam transport along the machine**
- **BAM: Bunch Arrival Monitor**
  - **Measure the beam arrival with respect to a timing reference**
- **C-BPM: Cavity – Beam Position Monitor**
  - **Measure the beam transverse position in the undulator hall**

MicroTCA: system requirements

- **Diagnostics back-end: development started in 05/2009**
- **Whole system in numbers:**
  - 25 – 30 stations in locations distributed along the machine
  - ~ 100 ADC inputs (in groups of 2-4)
  - ~ 40 DAC fast + slow outputs (in groups of 2+2)
- **Other features required**
  - General IO for slow control and monitor of field devices (frontend)
  - Fast communication to the control system (real time operation and machine feedback)

→ **Obvious need for a modular system**

  - Usual VME?
  - In 2009 still digging on a parallel bus architecture?

- **Why not xTCA?**
  - At the time not ripe
  - MicroTCA sounded already like a big step

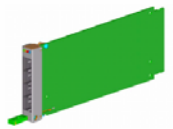
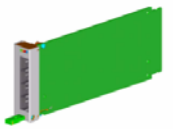
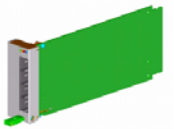
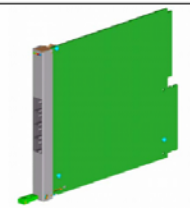
→ **We wanted to lase**

19 months later…

MicroTCA: necessary modules

❑ Advanced Mezzanine Cards (AMC)

- Double module (150mm) full size (29 mm)
- 4 converters per card (limited by real estate)
- IPMI (Intelligent Platform Management Interface)

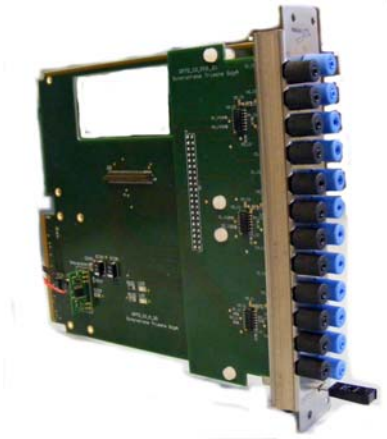
	Compact-Size (3HP)	Mid-Size (4HP)	Full-Size (6HP)
Single modules	 73.8x13.88x181.5mm	 73.8x18.96x181.5mm	 73.8x28.95x181.5mm
Double modules	 148.8x13.88x181.5mm	 148. 8x18.96x181.5mm	 148. 8x28.95x181.5mm

❑ MicroTCA Central Hub (MCH)

- Single module (74 mm) full size (29 mm)
- Clock distribution only
- I2C connectivity for IPMI testing

❑ Side Transition Modules (FERMI custom)

- Double module (150mm) full size (29 mm) → Introduce natural shielding
- AMC for general purpose digital I/O only
- AMC for specific BAM clock phase control

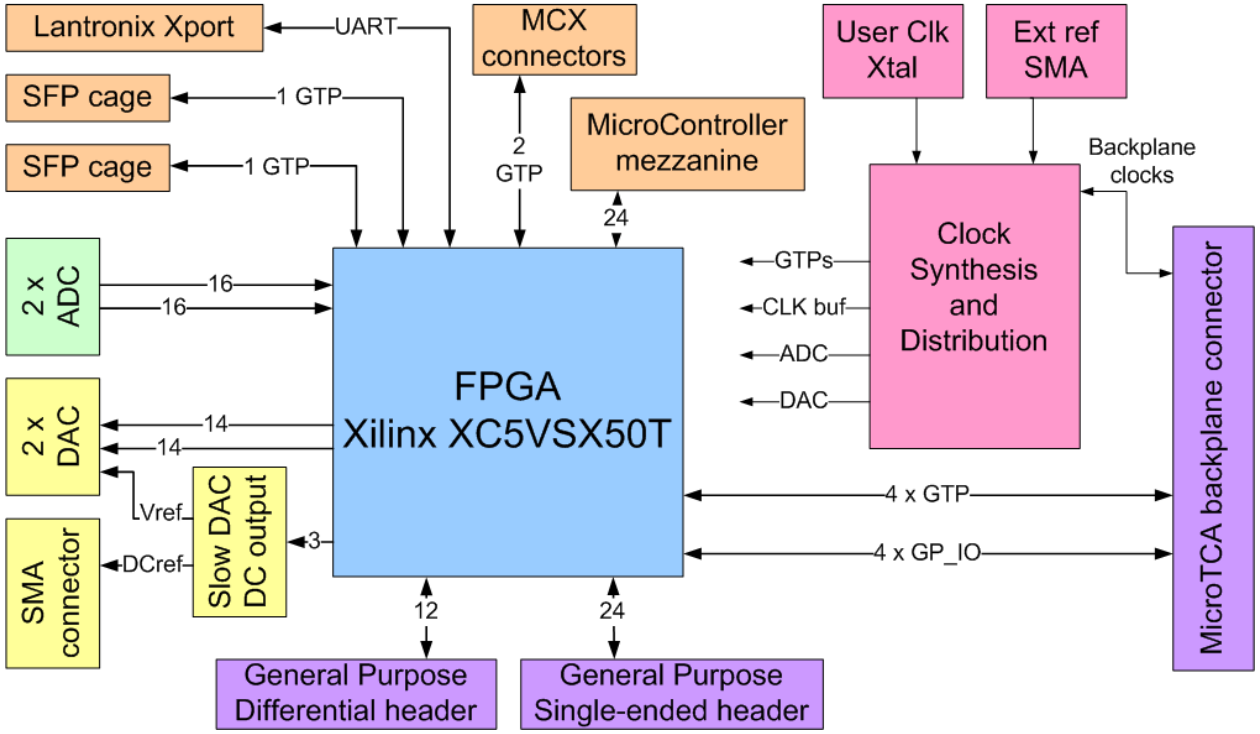


OPTIO_IO rev 1

❑ Backplane connectivity

- MicroTCA common test backplane sufficient
- Two clock frequencies distributed to all modules
- Gigabit connectivity (at least one GbE line)
- Ext. fat pipe routed to GPIO for trigger distribution (FERMI custom)

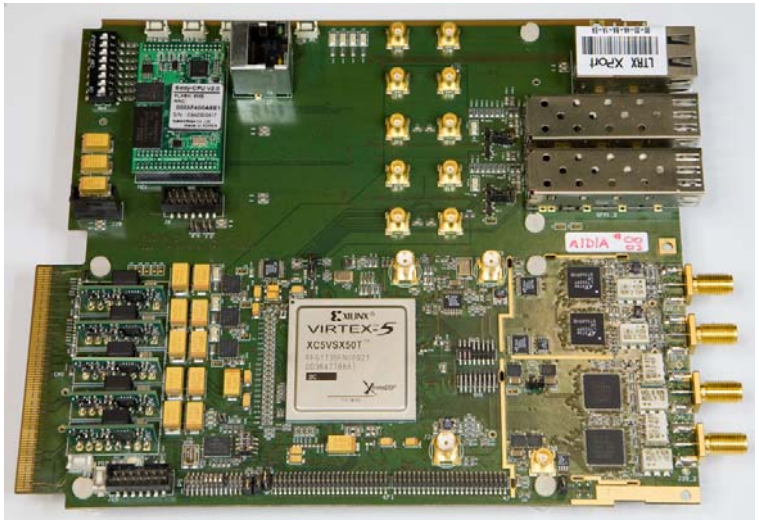
A|D|A
Analog Digital Analog converter board



- FPGA
  - Xilinx Virtex-5 SX50T
- 2 x ADC
  - Linear Technology LTC2209
- 2 x DAC
  - Maxim MAX5890
- Ethernet interface
  - Lantronix (10 Hz operation)
  - 2 x SFPs (50 Hz operation)
  - Backplane communication to MCH (future)
- Supplementary gear

❑ USE: fast waveform acquisition and synthesis

- ✓ Batch one: 4 prototype (rev0) units produced and tested
- ✓ Batch two and three: 6 + 14 (rev 1.5) produced all tested
  → 7 installed for diagnostics purposes
- 10 more units in production this year



ADA rev 1.5

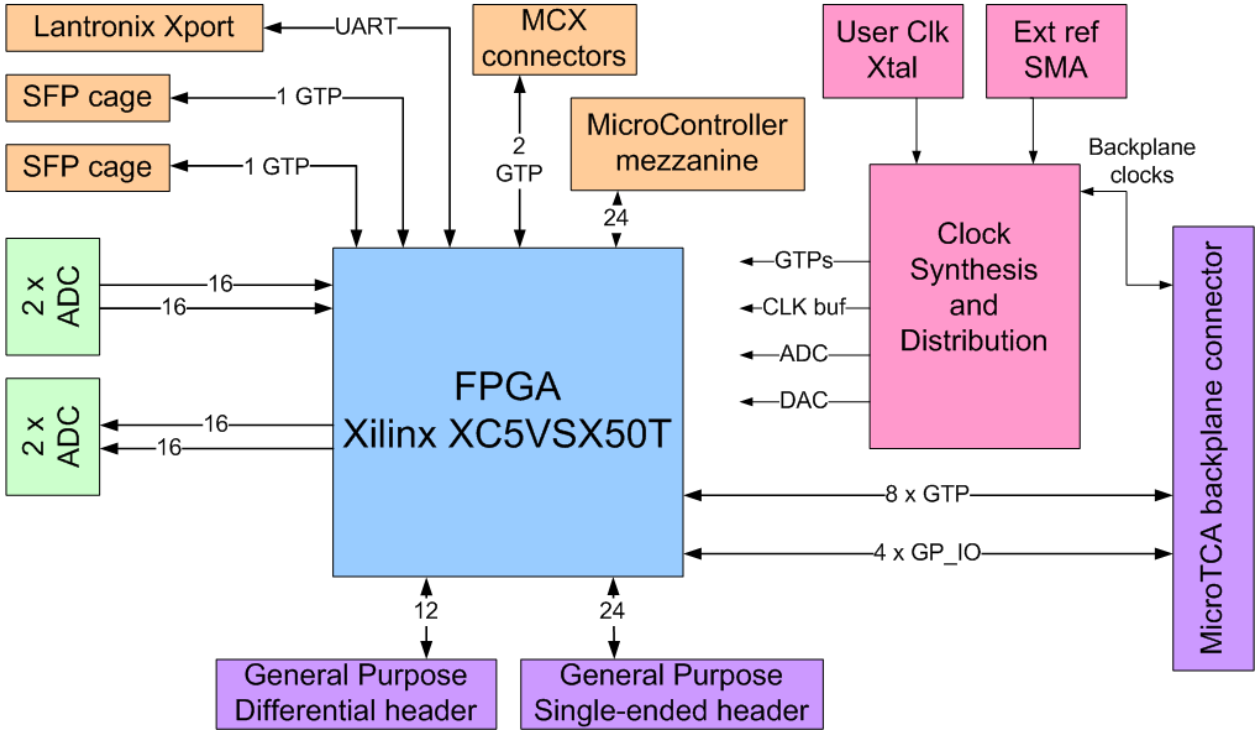
Technical Note ST/F-TN-09/14

Fermi Engineering Specification Document (FESD) #070

A|D|A: in numbers

- **FPGA Xilinx Virtex-5 SX50T**
  - Configurable Logic Blocks (CLB=1LUT+4FF): 8.160
  - Internal RAM blocks: 4.752 Kb
  - IOs: 480 single ended (240 differential)
- **ADC Linear Technology LTC2209**
  - Resolution: 16-bit @ 160 Msps
  - Input range: 1.5 or 2.5 Vp-p (hardware configured)
  - Passive input matching network (hardware reconfigurable) 700 MHz bandwidth max (ADC limited)
- **DAC Maxim MAX5890**
  - Resolution: 14-bit @ 600 Msps
  - Output range: -1.0 to +1.1 V (also remotely controllable acting on the reference with LTC2602)
  - Passive output matching network (hardware reconfigurable)
    default AC coupled with Bandwidth 0.130 – 425 MHz
- **DAC LTC2602 dual output 16 bits, DC coupled**
  - Bandwidth DC – 1 KHz and Amplitude range 0 – +3.3 V
  - Optional fast DAC output range control acting on the reference
- **Supplementary features**
  - General purpose IOs (dual row 1.27 mm pitch headers and SMAs)
  - Hardware configurable clock distribution
  - Gigabit Transceivers Pair (GTP) optical and electrical (including SFPs)
  - MicroTCA backplane communication (4 GTPs)

A|D|O
Analog Digital Only converter board

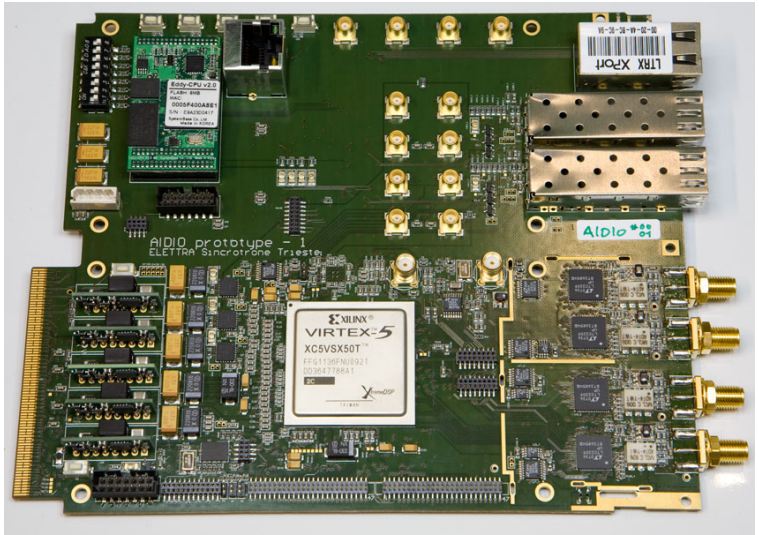


- FPGA
  - Xilinx Virtex-5 SX50T
- 4 x ADC
  - Linear Technology LTC2209
- Ethernet interface
  - Lantronix (10 Hz operation)
  - 2 x SFPs (50 Hz operation)
  - Backplane communication to MCH (future)
- Supplementary gear
  - Enhanced with respect to ADA

USE: fast waveform acquisition

- ✓ Batch one: 4 prototype (rev1) units produced and tested
- ✓ Batch two and three: 4 + 10 (rev 1) produced all tested
  → 10 installed for diagnostics purposes
- 4 more units in production this year

Fermi Engineering Specification Document (FESD) #014

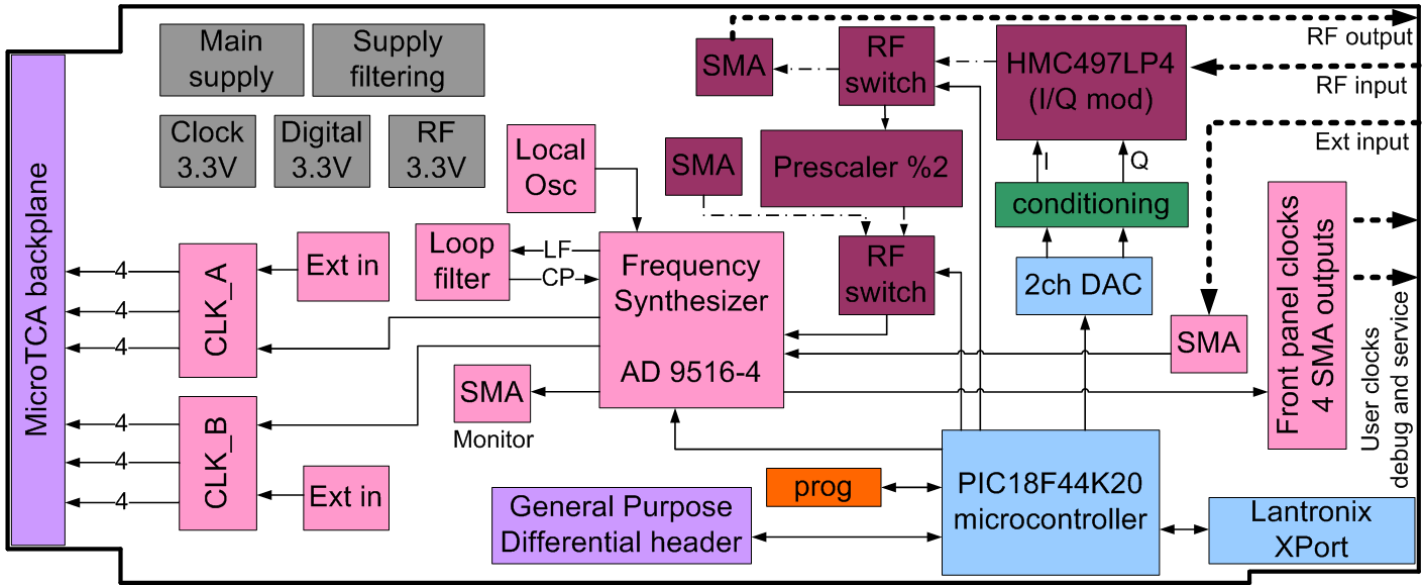


ADO rev 1

A|D|O: in numbers

- **FPGA Xilinx Virtex-5 SX50T**
  - Configurable Logic Blocks (CLB=1LUT+4FF): 8.160
  - Internal RAM blocks: 4.752 Kb
  - IOs: 480 single ended (240 differential)
- **ADC Linear Technology LTC2209**
  - Resolution: 16-bit @ 160 Msps
  - Input range: 1.5 or 2.5 Vp-p (hardware configured)
  - Passive input matching network (hardware reconfigurable) 700 MHz bandwidth max (ADC limited)
- **Supplementary features**
  - General purpose IOs (dual row 1.27 mm pitch headers and SMAs)
  - **Hardware configurable clock distribution modified and improved**
    Micrel SY58040UMY 3x3 cross point switch
  - Gigabit Transceivers Pair (GTP) optical and electrical (including SFPs)
  - **MicroTCA backplane communication enhanced**
    more transceiver pairs connected (8 GTPs)

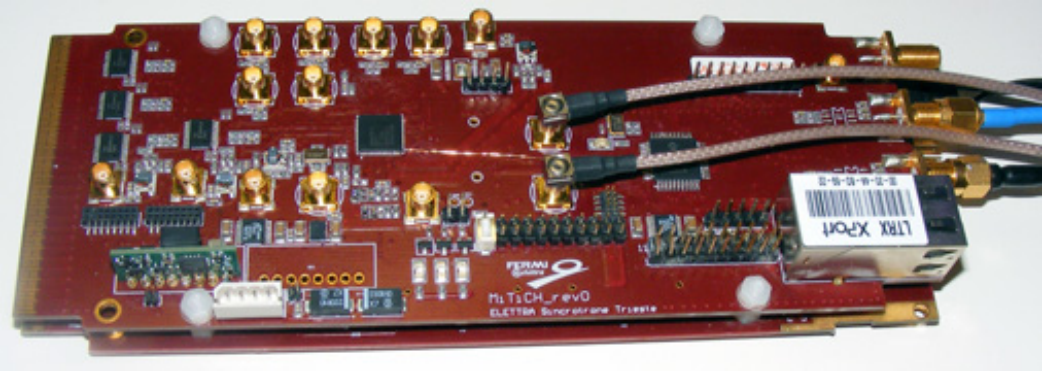
MiTiCH
MicroTCA Timing Central Hub



- Clock chip
  - Analog Devices AD9516
- Ethernet interface
  - Lantronix
- Board control
  - PIC 18F44K20
- Supplementary gear
  - RF vector modulator

USE: Clock distribution via uTCA backplane

- Serve up to 12 AMC
- Output freq.: 50-300 MHz and 100-600 MHz
- RF frequencies: up to S-band (3 GHz)
- Lock to external frequencies
- Local oscillator: user select 10-250 MHz
- ✓ Batch one: 6 units produced (4 mounted)
  → 4 installed (without RF vector modulator)
- 5 units in production this year (second revision foreseen)

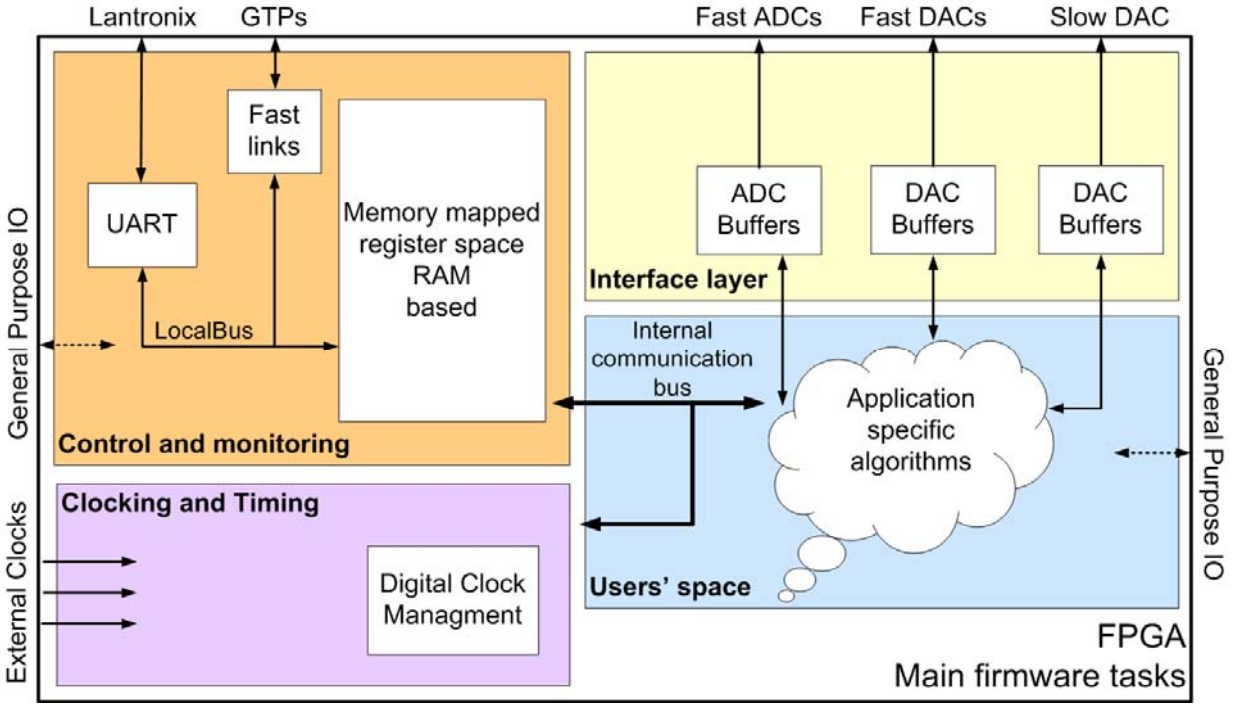


MiTiCH base and tongue2 rev 1

Fermi Engineering Specification Document FESD #077 draft

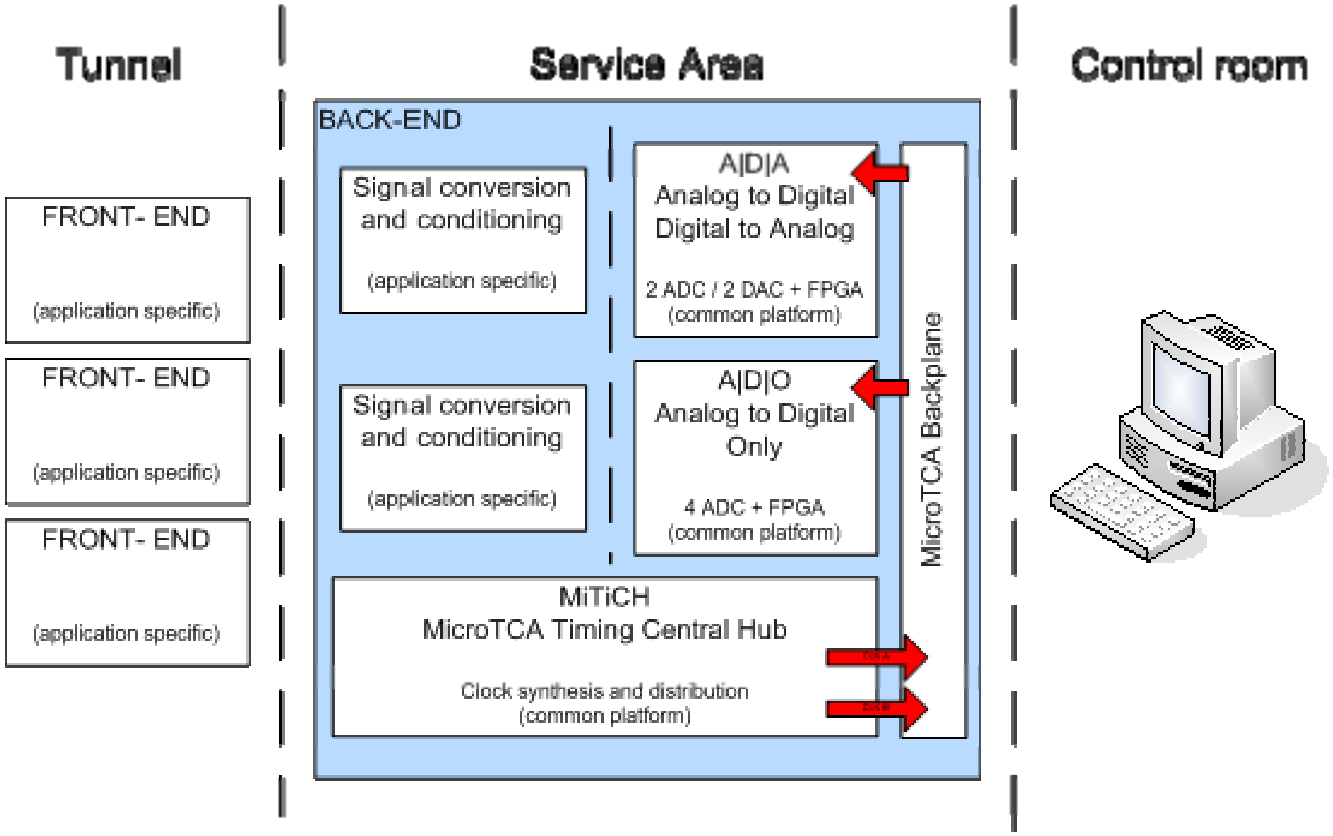
Gateware and Software infrastructure

- **Gateware common infrastructure code:**
  - Control system communication
  - ADC and DAC buffering
  - Internal logic clocking
- **Gateware application specific users space:**
  - BAM: calculate beam arrival time
  - C-BPM: calculate beam position



- **Control field stations, network, and control room software:**
  - Machine triggered data acquisition via Micro Research Event System (10 and 50 Hz)
  - UDP/IP based data transfer from the uTCA back-end systems to the field stations
  - Field stations based on MVME7100 VME PowerPC boards
  - Linux with Xenomai real time extension
  - Tango control system software

FERMI@Elettra specific cases



- Having defined, built, and tested the individual building blocks
- We started commissioning our diagnostics' systems
- Continuous feedback from the field triggered further in-depth examination in the lab

The BAM case: hardware

- **1 BAM station**
  - 1 A|D|A module
  - 1 Signal Conditioning Board (SCB) for high accuracy clock shift (157 MHz)
  - 2 wideband (12 GHz) Photo Diodes (PD)
- **System initial idea**
  - 1U uTCA crate (Schroff)
  - Custom front panel
- **Actual implementation**
  - Replaced the 1U box PSU (the original far too EMI noisy)
  - Disconnected a few fans
  - Separate custom chassis for PDs and SCB (very sensitive to noise)

Fermi BAM back-end in the klystron gallery

The BAM case: summary and results

❑ Goal

- Install 3 stations
- Measure the arrival time with an accuracy of less than 20 fs

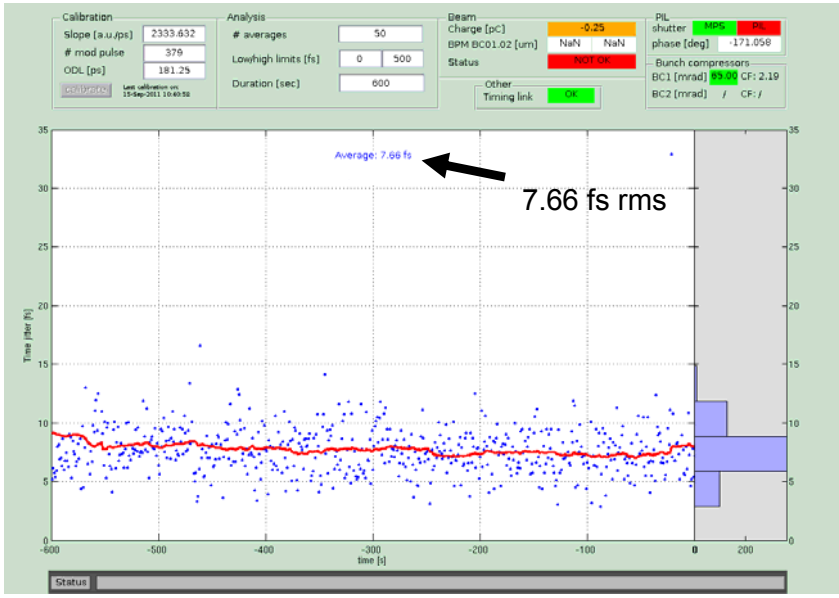
❑ Achievements

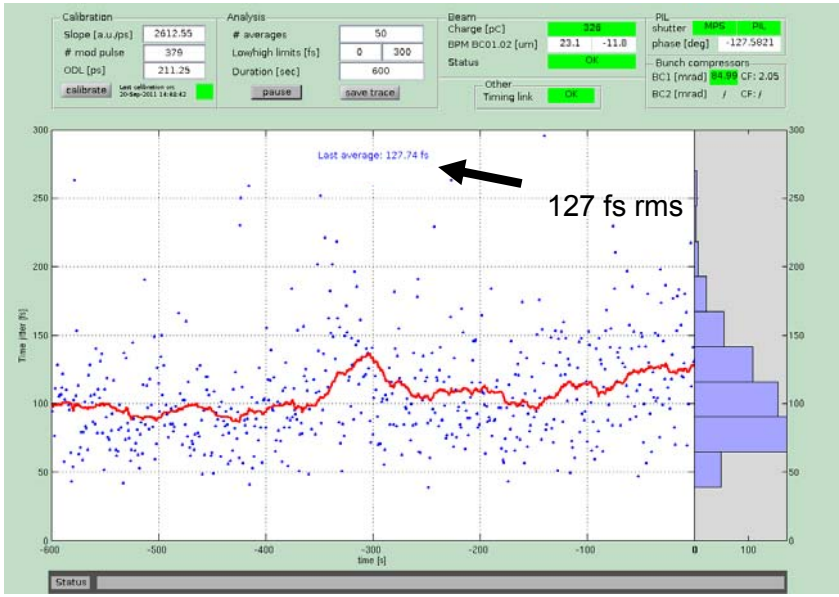
- 2 systems on the field
- Prove the overall concept
- Demonstrate the capabilities of the digitizer
- Demonstrate the communication interface to the control system
- Provide a basic system to lase
- Rudimental platform for physics case studies (bunch compressor, linac)

❑ To do

- Further refine all systems
- Better integrate in the control system
- Further study calibration and measurement algorithms

BAM measurement noise floor and beam jitter

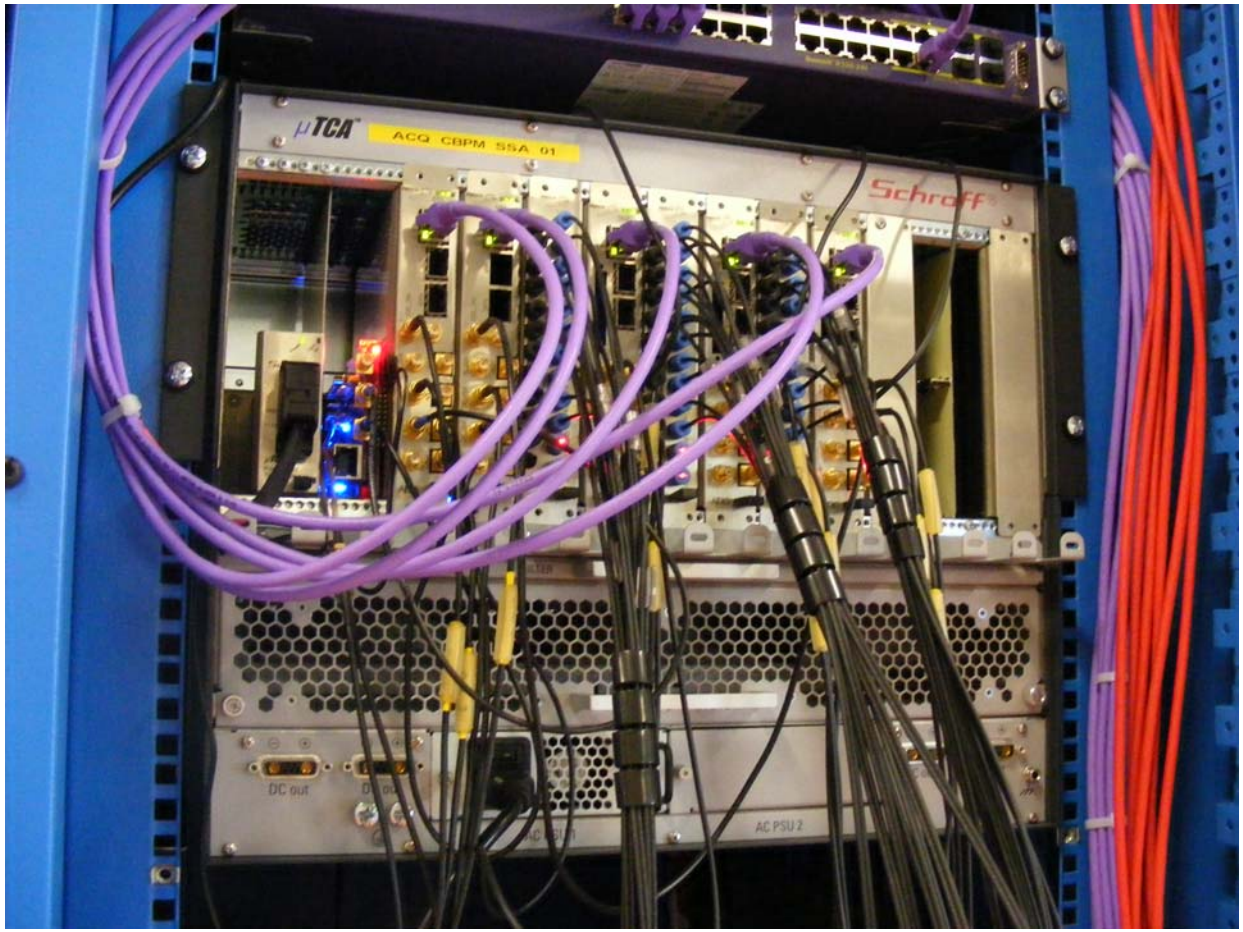




The C-BPM case: hardware

- **1 C-BPM station**
  - 1 A|D|A module
  - 1 A|D|O module
  - 1 MiTiCH module
  - 1 OptioIO module
- **System initial idea**
  - 9U uTCA test crate (Schroff)
  - 3 C-BPMs per crate
  - 2 A|D|A modules
  - 3 A|D|O modules
  - 1 MiTiCH modules
  - 3 OptioIO modules
  - 1 patch panel
- **Actual implementation**
  - As foreseen
  - Replaced the 220VAC to 12DC PSU (the original coupling EMI noise to devices outside the crate)

Fermi C-BPM back-end in the service area



The C-BPM case: summary and results

Goal

- Install 10 systems
- Measure the beam position in the undulator area with an accuracy of 1 um (or better)

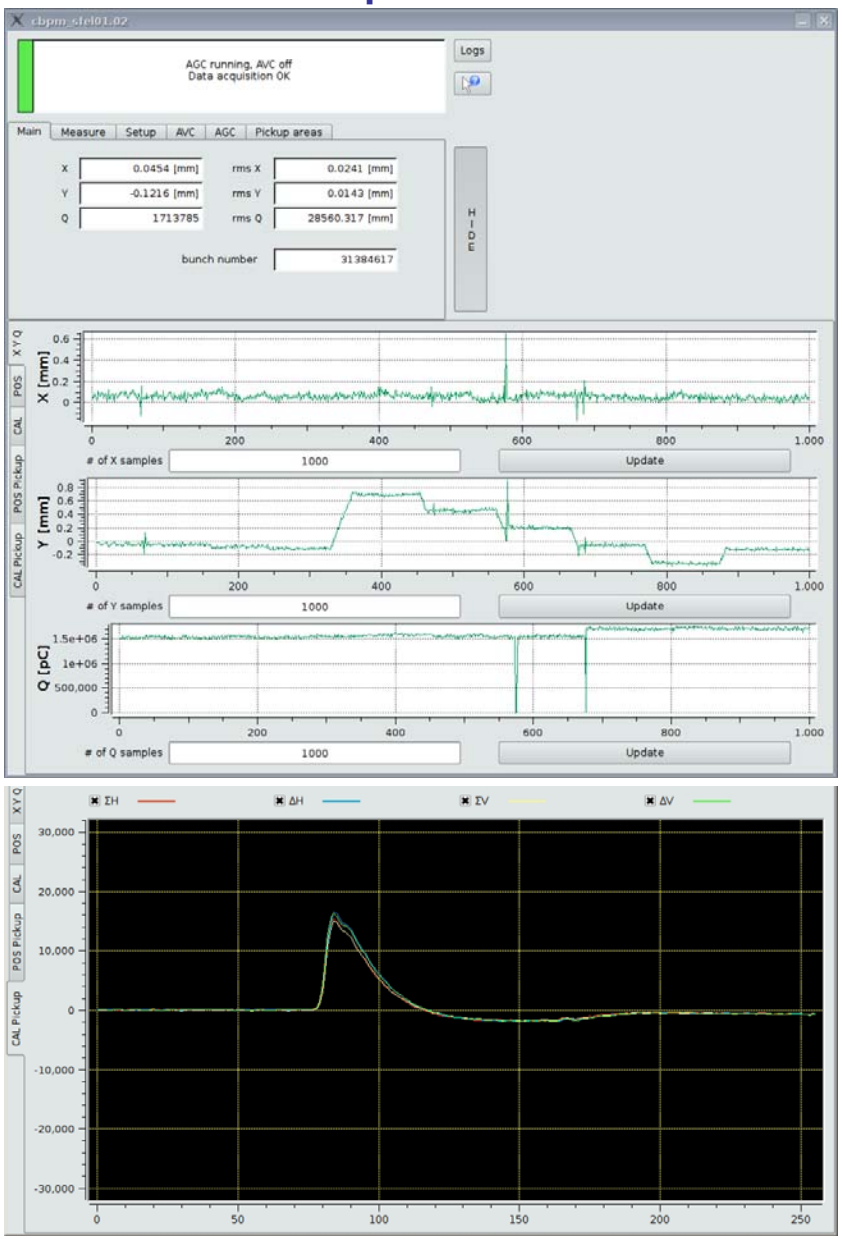
Achievements

- All systems on the field
- Provided a basic system to lase with an accuracy of 1.7 um on average
- Solid platform for physics case studies (machine feedback, alignment matrix)
- Robust and reliable system on the field (no hardware faults in 5 runs)

To do

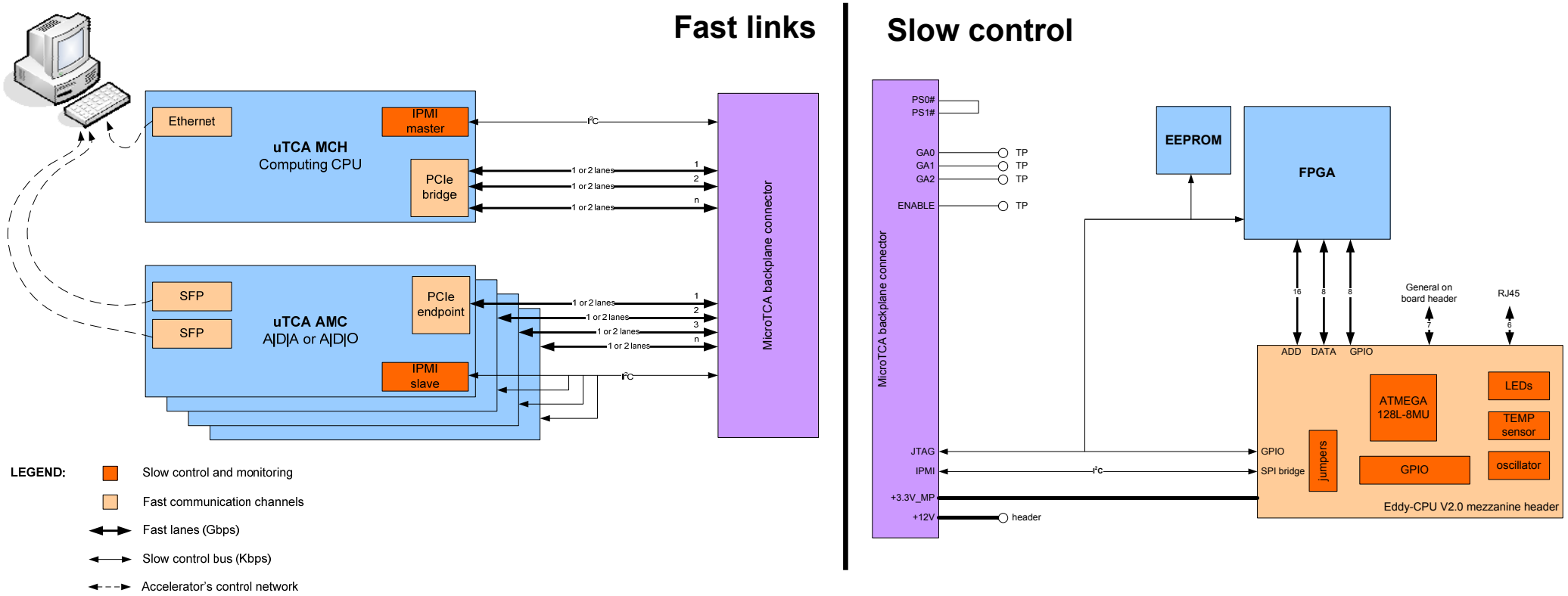
- Commission the systems for the FEL2 line
- Further improve the frontends performance to meet resolution specs
- Upgrade for 50 Hz machine operation
- Further study calibration and measurement algorithms

C-BPM operator interface

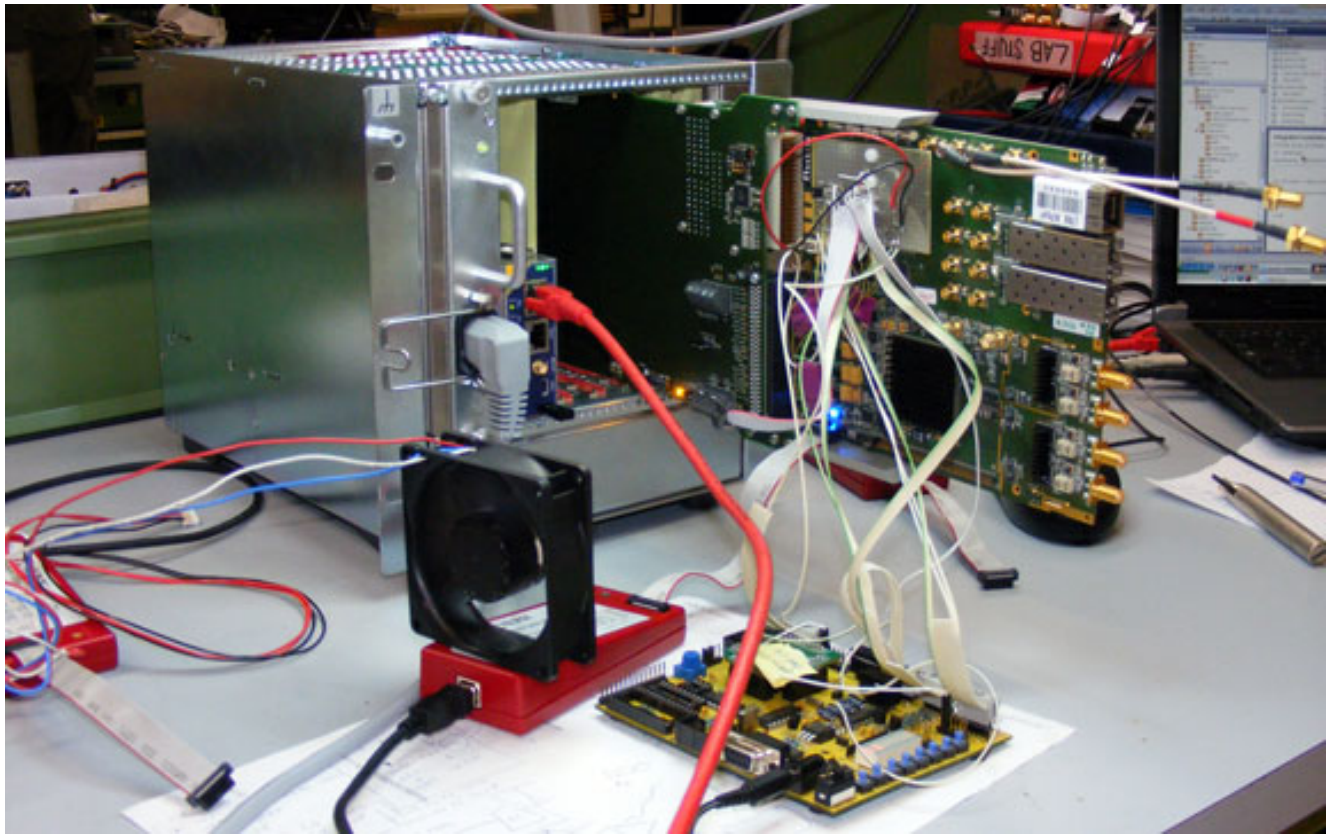


Other MicroTCA developments

- IPMI controller integration on A|D|A and A|D|O
- PCI express end-point for data transfer from an AMC to a CPU
- Gigabit Ethernet communication via onboard SFPs (or backplane)



Other MicroTCA developments



- ✓ IPMI controller feasibility tests
  - wired eval kit Atmega 128L-8MU on A|D|O
  - Micro controller firmware for IPMI courtesy of DESY
- ✓ PCI express end-point (4 x 2.5 Gbps) data transfer from/to CPU on A|D|O
  - ADLink CPU AMC1000 (/L7400/M1G(EA) (intel x86 64bit) SANBLADE SATA HDU
  - MCH N.A.T.
  - Linux drivers and firmware infrastructure courtesy of DESY

Infinite thank you to P. Gessler and DESY

Work founded by IR-UV-X framework

Our experience with MicroTCA

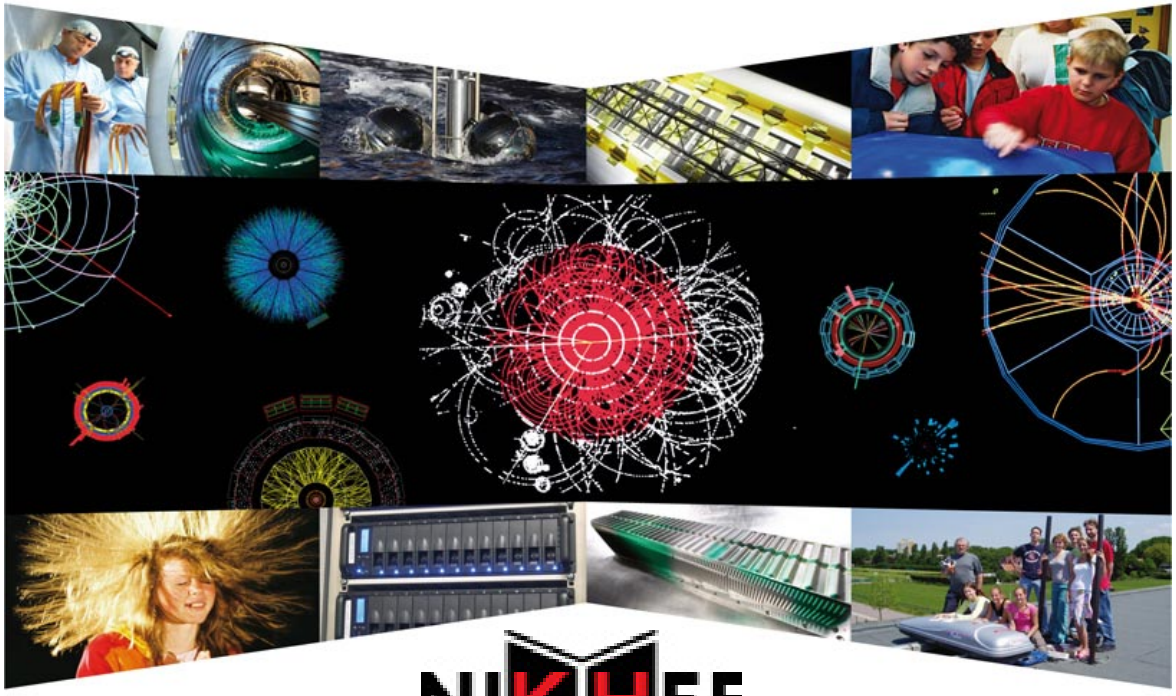
- Overall the choice of MicroTCA as a common platform for beam diagnostics applications has been proved to be correct
  - It is a robust type of system , easy to service and maintain
- We had to face the common difficulties of the pioneers
  - Workarounds and hacks included in the fun!
- Especially working on the technology advanced features
  - We touched with hands its great potential
  - IPMI and backplane bandwidth capabilities are really impressive
- We believe that the experience with uTCA will bring great benefits to its specific implementation for physics (xTCA)
  - All the limitation and pitfalls are clear and somehow understood
- uTCA as is can still be a good option for smaller systems
  - And uTCA AMCs can be integrated in ATCA blades
- We hope that this work will be followed by many others

Acknowledgements

That is the result of a successful and fruitful team work

- **R. De Monte** : C-BPM acquisition system layout and RF front-end
- **L. Pavlovic** : BAM front-end and SCB
- **F. Rossi** : global timing and optical systems
- **M. Predonzani** : FPGA programming
- **G. Gaio** : Tango server/Real Time
- **F. Asnicar** : Fermi CR panels
- **M. Ferianis** : head of Fermi's timing and diagnostics
- **M. Pontremoli** : board layout (Fidenza – Italy)
- **TVR s.r.l. :** PCB manufacturing (Treviso – Italy)
- **SCEN s.r.l.** : PCB mounting (Trieste – Italy)
- **Officine Barnobi** : custom and rugged uTCA panels (Trieste – Italy)

What's next ?



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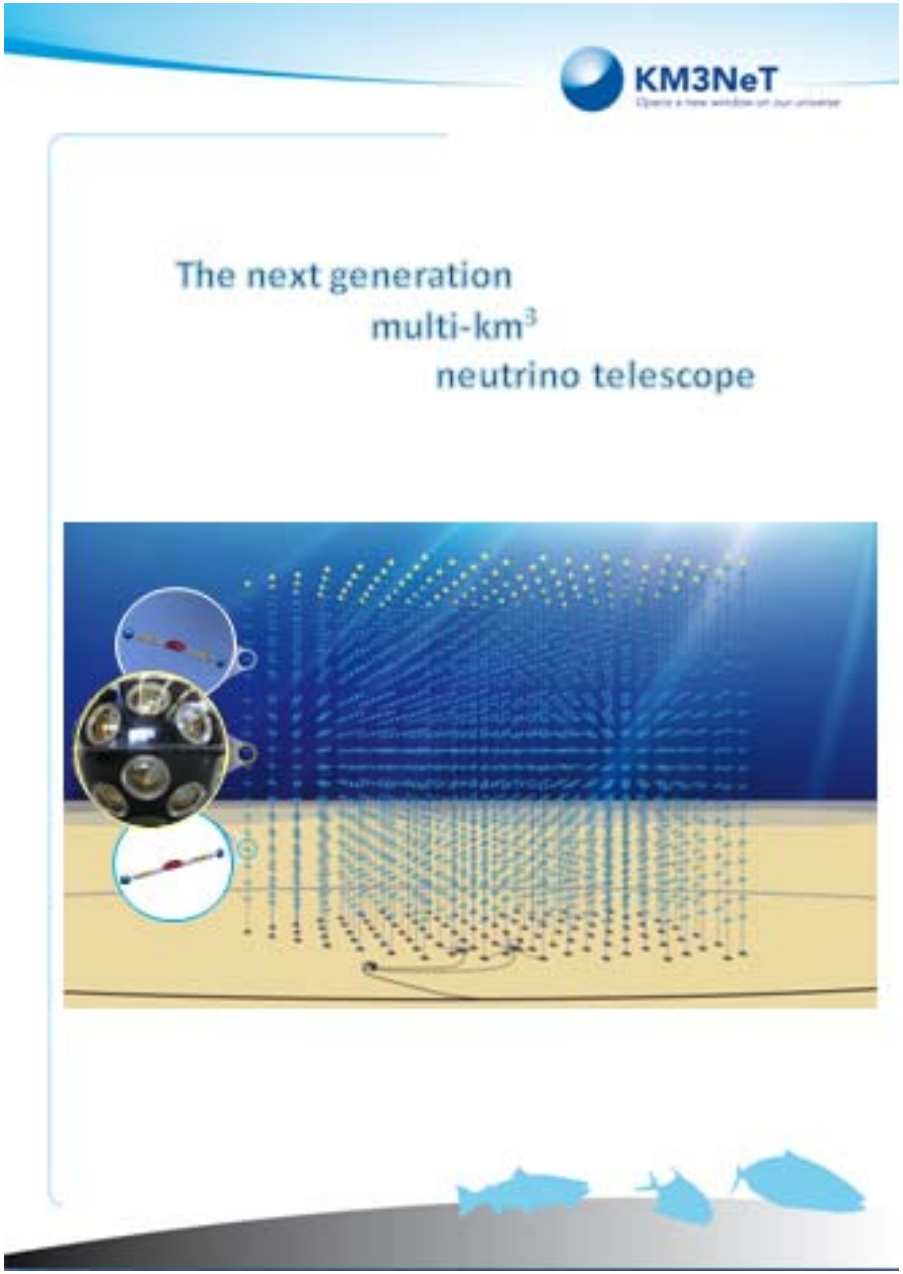
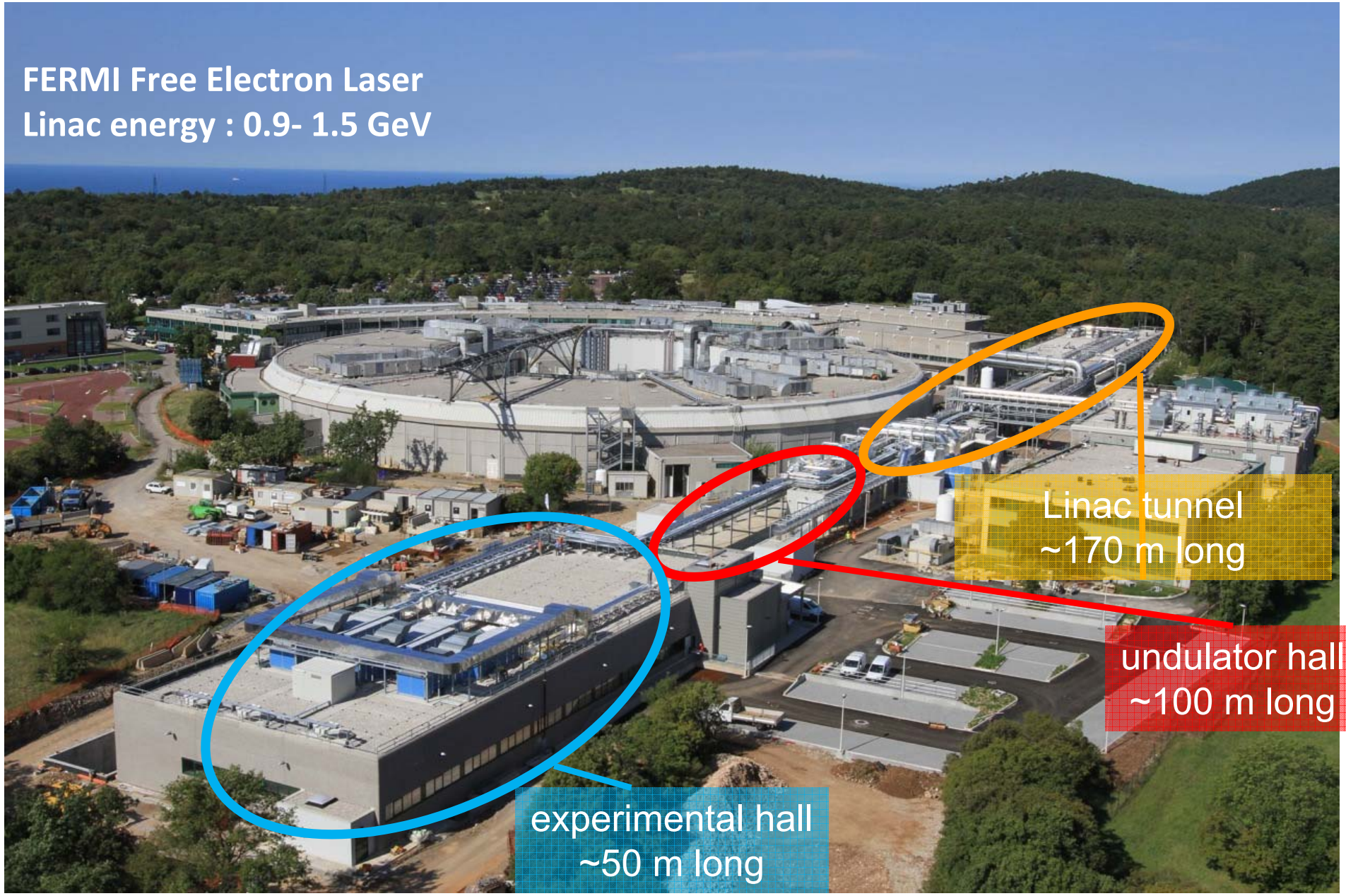


More HEP frontiers

to be explored!

Backup slides

FERMI@Elettra Light Source

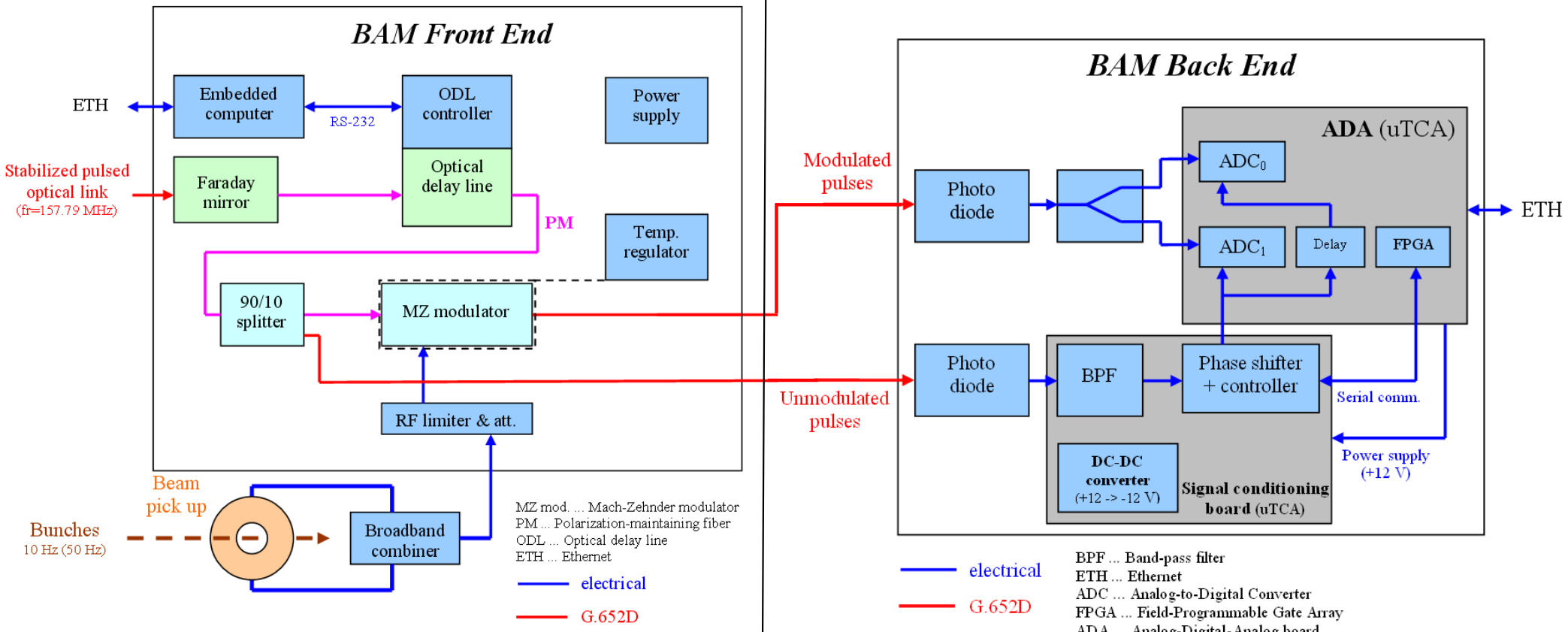


The BAM case: architecture

Measure the bunch arrival time along linac and undulators

FERMI
linac tunnel

FERMI
Klystron gallery



Courtesy of L. Pavlovic

The C-BPM case: architecture

Measure the transversal beam position in the undulator area