FPGA-based hardware instrumentation development on MAST

Billy Huang[1,2], Graham Naylor[1], Nizar Ben-Ayed[1], Geoffrey Cunningham[1], Anthony Field[1], Sunita Khilar[1], Richard Myers[2], Ray Sharples[2], Roddy Vann[3]

[1]EURATOM/UKAEA Fusion Association, Culham Science Centre, Abingdon OX14 3DB, UK.
[2]Department of Physics, University of Durham, South Road, Durham DH1 3LE, UK.
[3]Department of Physics, University of York, Heslington, York YO10 5DD, UK.

b.k.huang@dur.ac.uk, graham.naylor@ccfe.ac.uk, nizar.benayed@ccfe.ac.uk, geoffrey.cunningham@ccfe.ac.uk, anthony.field@ccfe.ac.uk, sunita.khilar@ccfe.ac.uk, r.m.sharples@dur.ac.uk, r.m.myers@dur.ac.uk, roddy.vann@york.ac.uk.

Funded by EPSRC and EURATOM.

Introduction

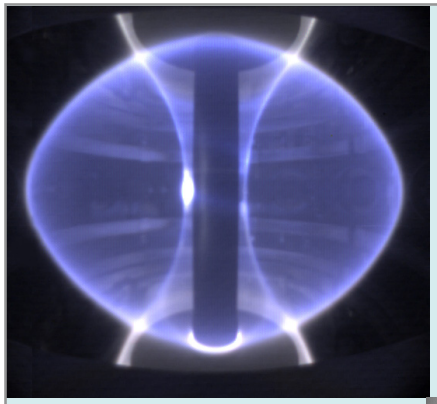
- A very brief introduction to the Mega Amp Spherical Tokamak (MAST) machine and general development context for an FPGA system on MAST.

- Details on the hardware used for 7 different FPGA systems on the Mega Amp Spherical Tokamak (MAST).

- Description of the hardware methodology used to create these systems.

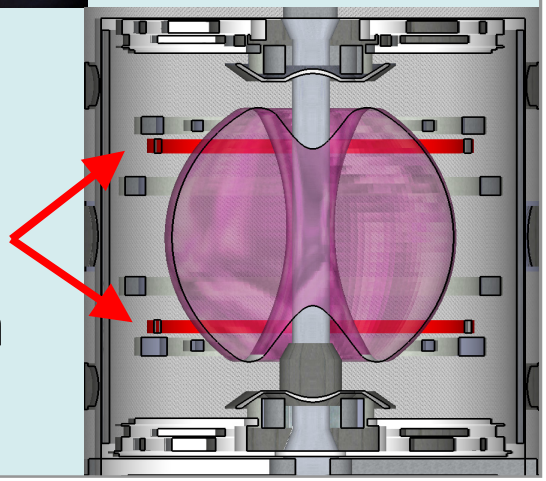
Vertical Stabilisation

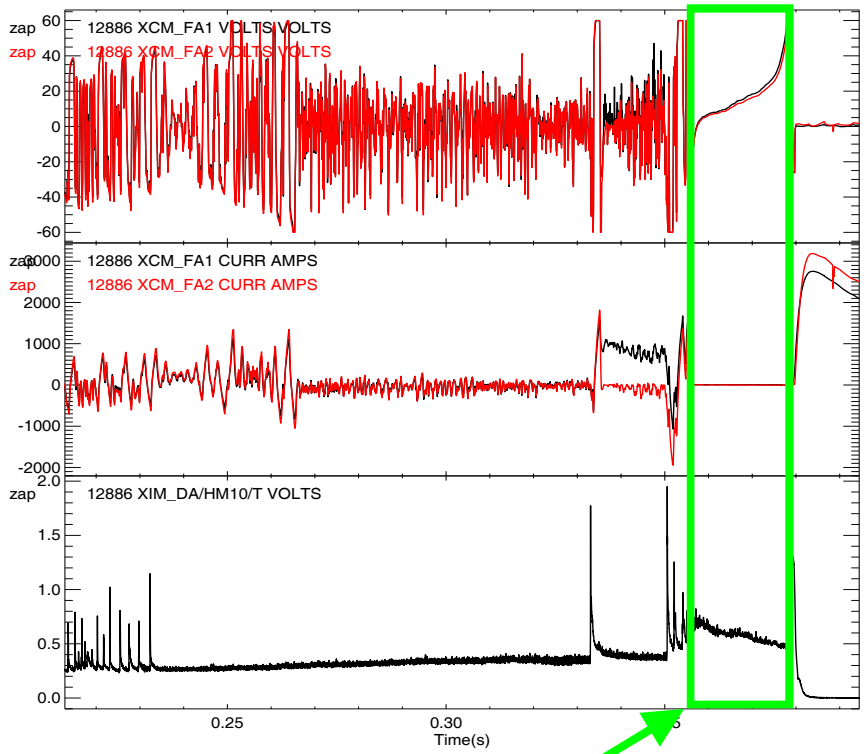
MAST Tokamak Plasma



Hydrogen fuel (deuterium) heated to ~ 30 million degrees.

Plasma vertical (P6) stabilisation coils

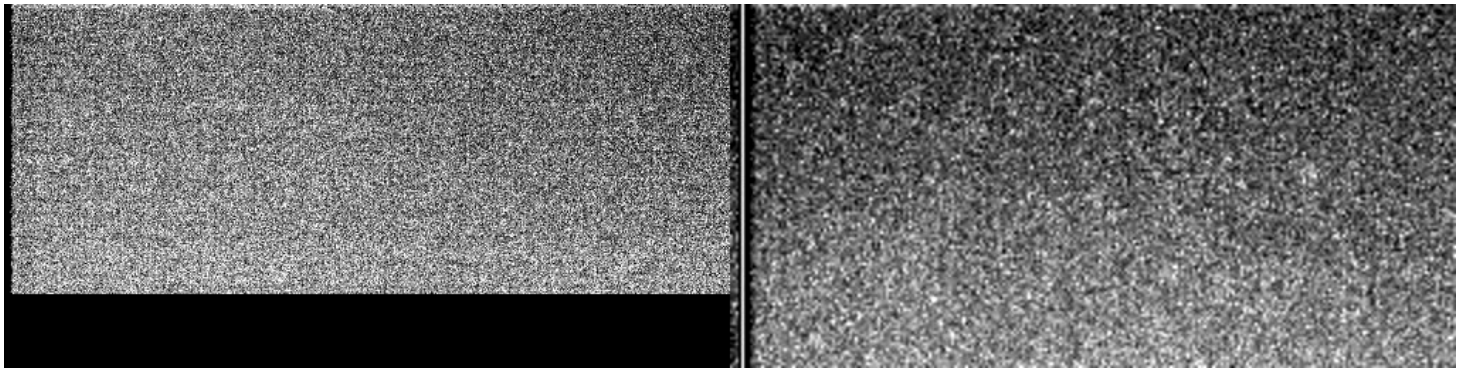


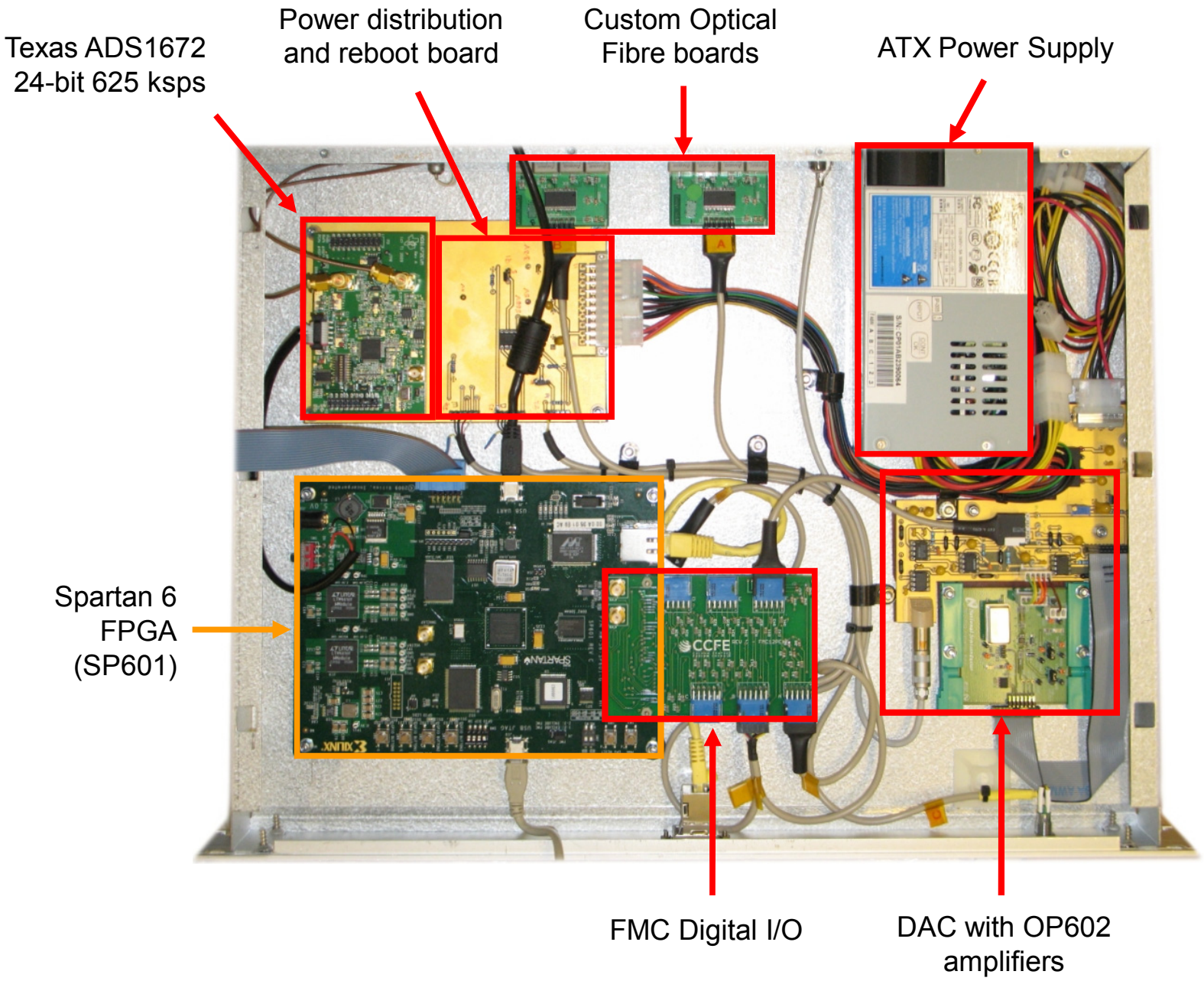


Plasma lost due to amplifier trip induced by plasma eruption (ELM)

Viewing a vertically unstable plasma

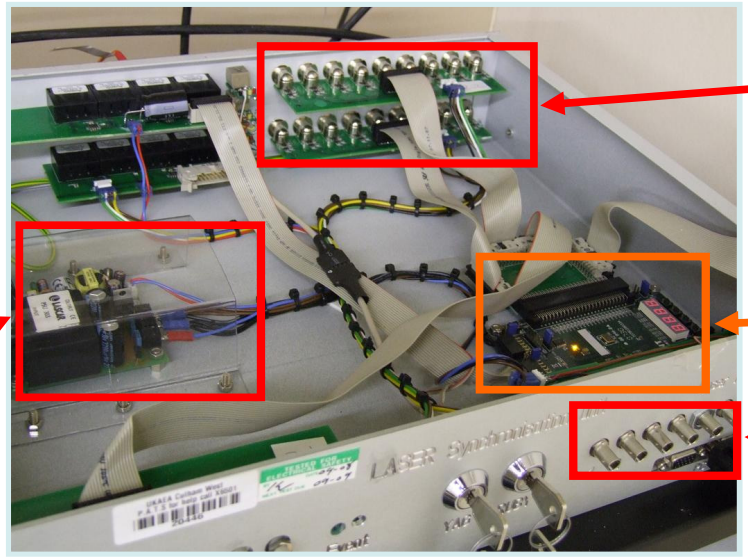
(Shot 12886)




Texas ADS1672
24-bit 625 ksps
Power distribution
and reboot board
Custom Optical
Fibre boards
ATX Power Supply
Spartan 6
FPGA
(SP601)
FMC Digital I/O
DAC with OP602
amplifiers

Laser Triggering System

The old way of doing things using the Spartan 3E and serial UART for communication



BNC 50 Ohm driving signals to each of the 8 lasers

Spartan3E FPGA

Custom Power supply

Optical amplitude digitisation for laser energy.

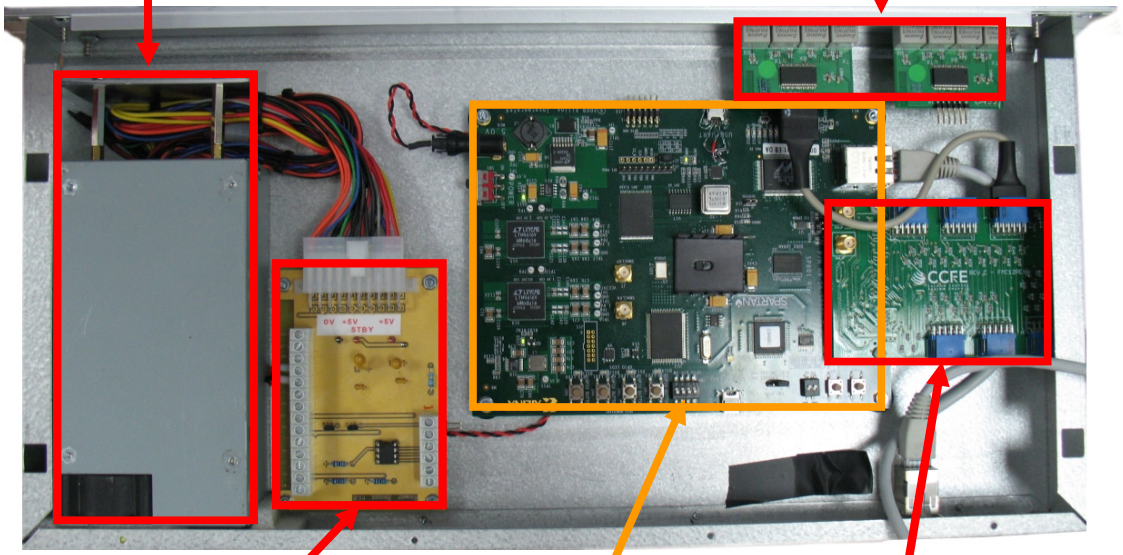
Controls 8 Nd:Yag 1.6J Lasers at 30 Hz (megawatts of Peak power)

PLC Pulse Generator - Fast Timer

ATX Power supply

37 ns precision pulse generator with variable delay and width

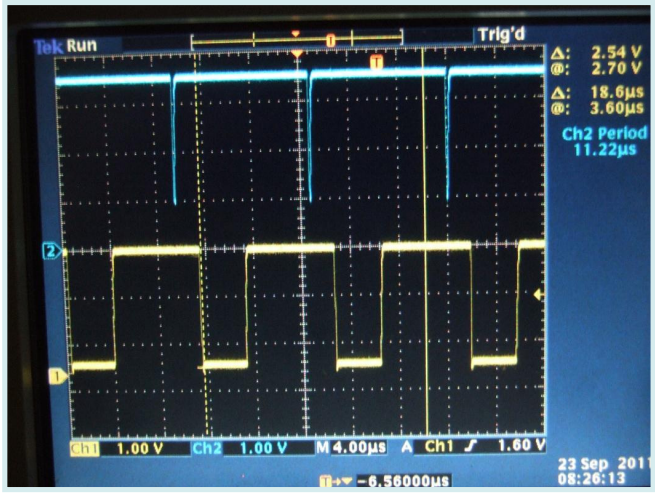
Optical TX/RX for Trigger and Pulse Generator



Power distribution and remote reboot

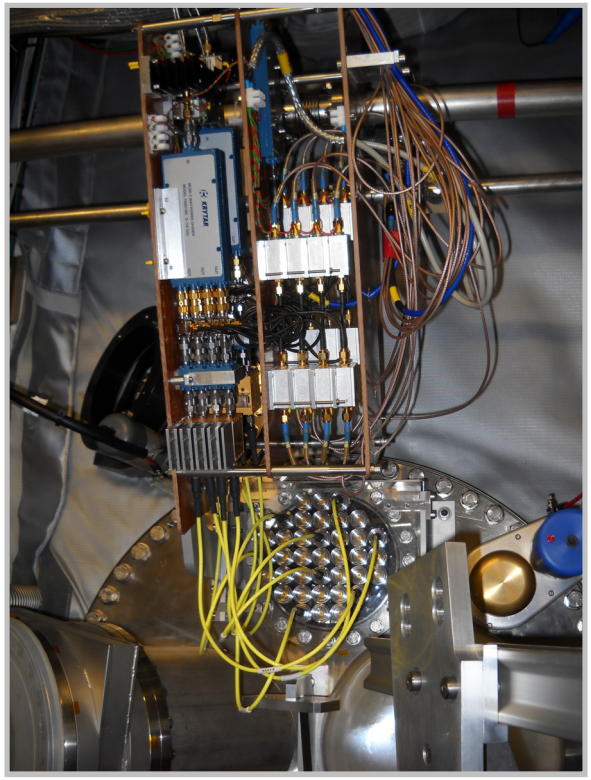
Spartan 6 FPGA (SP601)

FMC Digital I/O



Real-time fast acquisition

Microwave Imaging System



Ultra high performance FPGA system for acquiring and analysing 6-40 GHz microwave radiation emitted by the plasma.

5U Chassis. 16 Channels, 250MHz at 14-bit digitising 125 MHz bandwidth signals.

Streaming in real-time at 8GB/s (for 0.5s)

This was a joint project led by Dr. Roddy Vann of York University.

FMC 108 4DSP
8 Channel ADC
14-bit 250 Msps

SSMC Connectors

(High density but fragile, always wire internally)

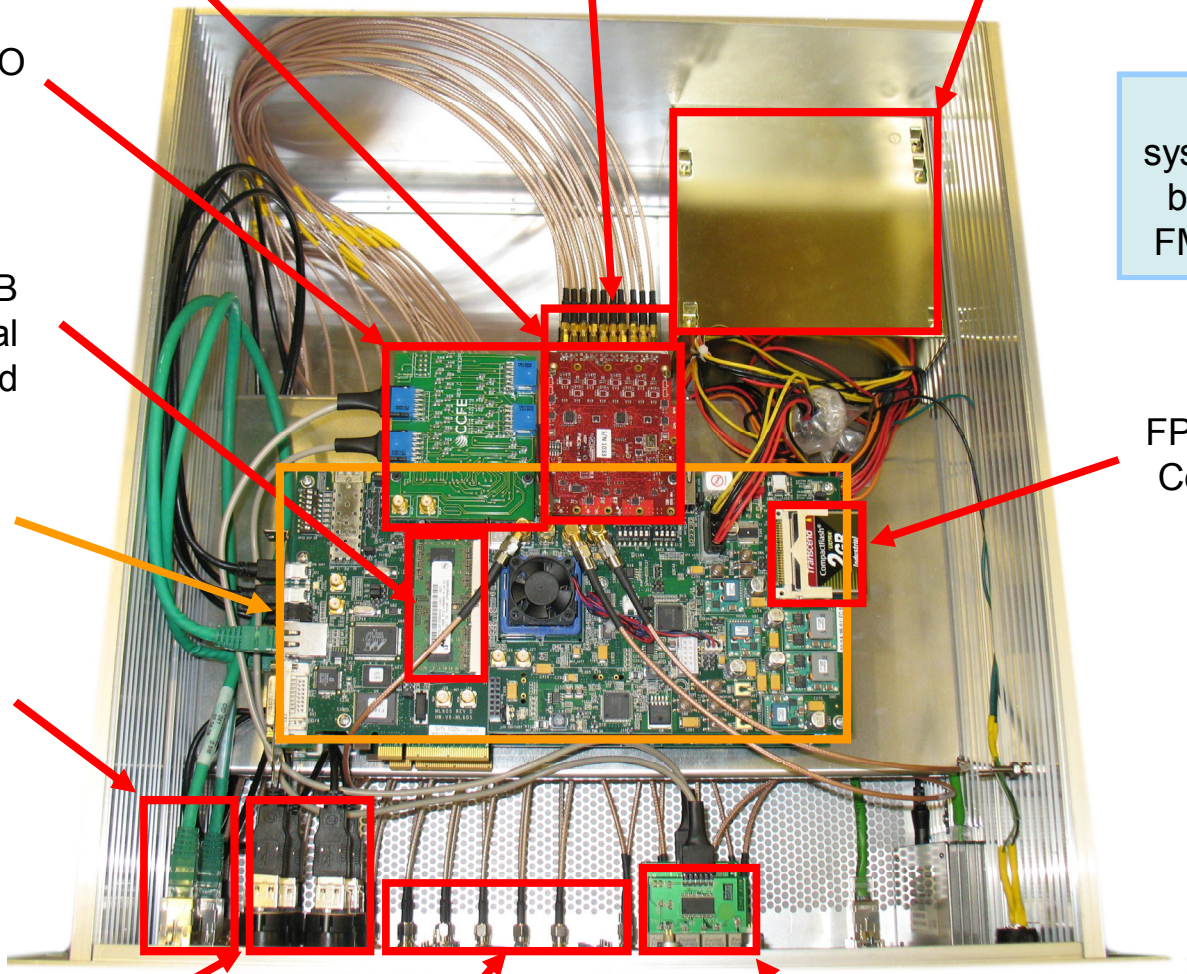
Standard ATX Power Supply

FMC I/O

DDR3 RAM 2GB
6.4 GB/s Theoretical
5+ GB/s Achieved

Virtex 6 FPGA Board (ML605)

Gigabit Ethernet



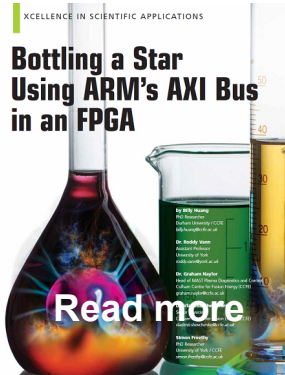
Dual Layer system: 2 FPGA boards with 2 FMC108 ADCs

FPGA Firmware CompactFlash

USB JTAG/UART

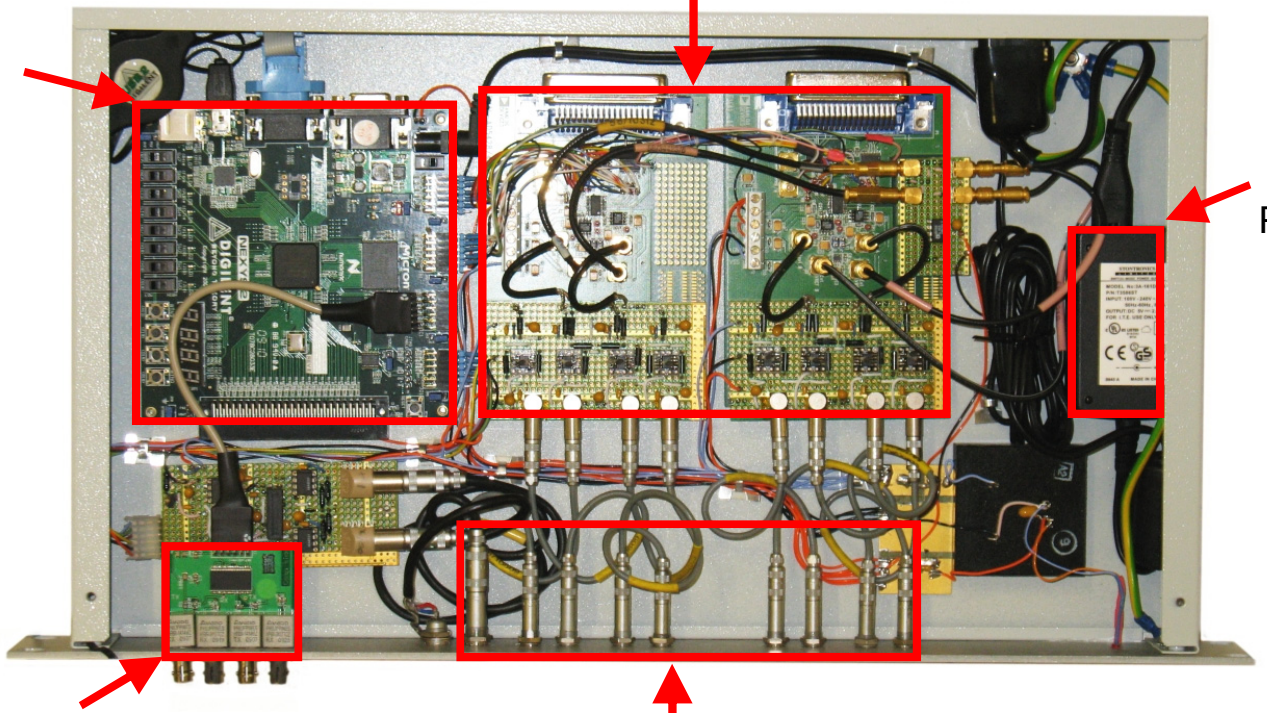
SMA Front Panel

Opto Clock, Trigger, Reboot



Resonance Monitoring/Driving - TAE System

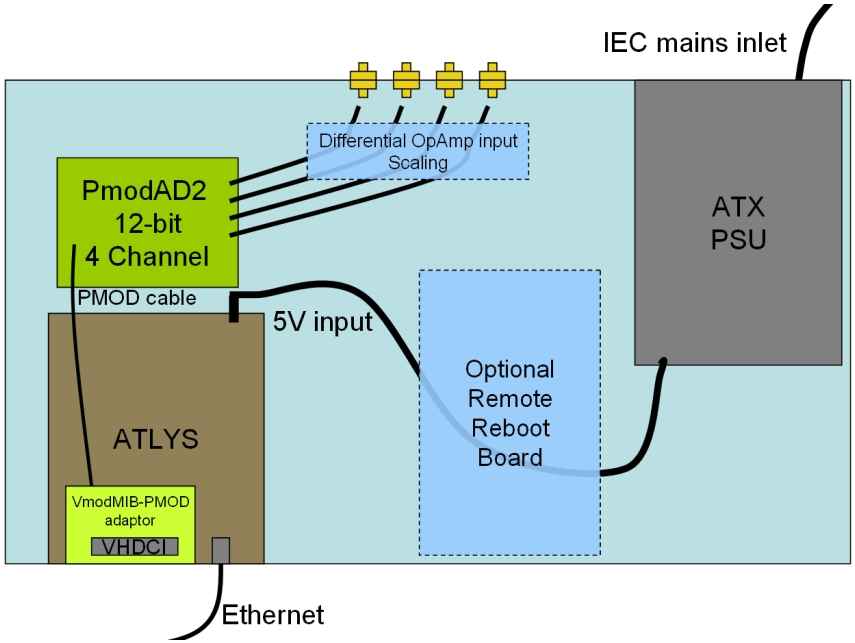
Toroidal Alven Eigenmode (TAE) are global plasma modes. They can be driven by the FPGA system below at different frequencies. Similar to a Tune Monitor.

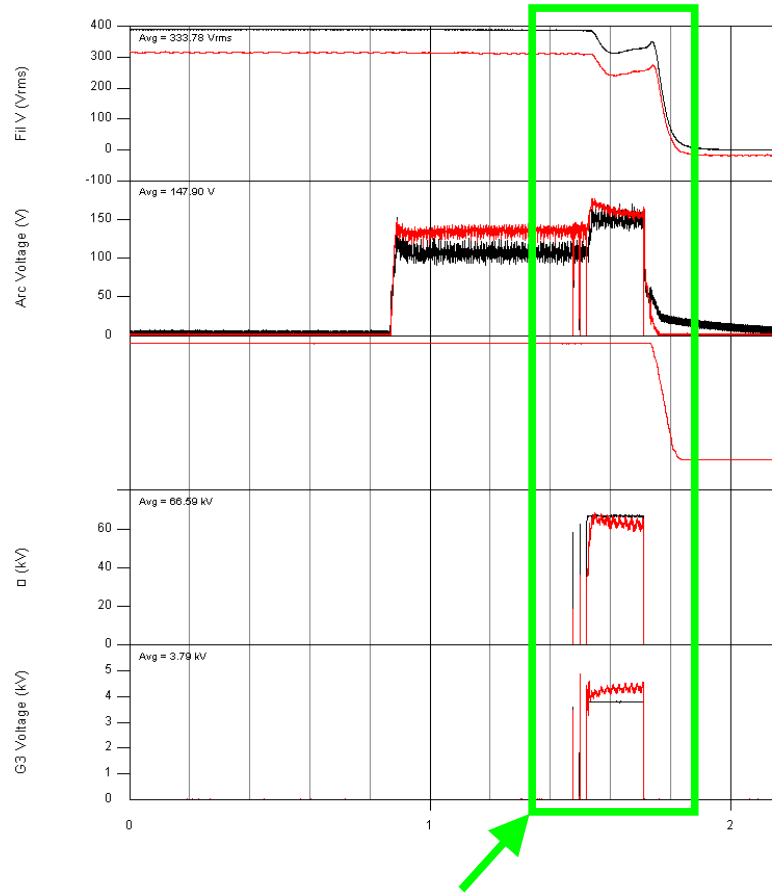


Monitoring - NBI Arc Current

Neutral Beam Injection (NBI) on MAST provides over 3.2MW of power.

In development: Atlys Spartan6 FPGA Board, 1U Rack, ATX Power supply, 1 MHz 12-bit 4 Channel DAC.



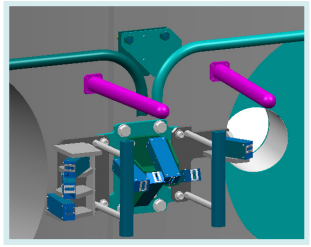


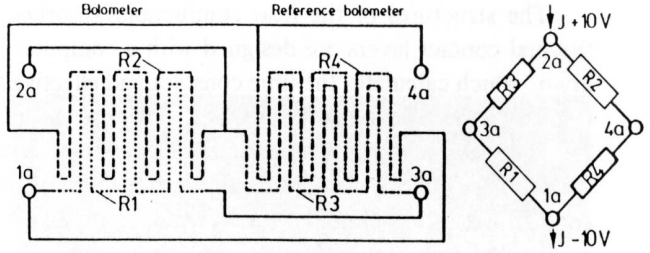
NBI arc current: Measuring in greater detail helps diagnosis system failures.

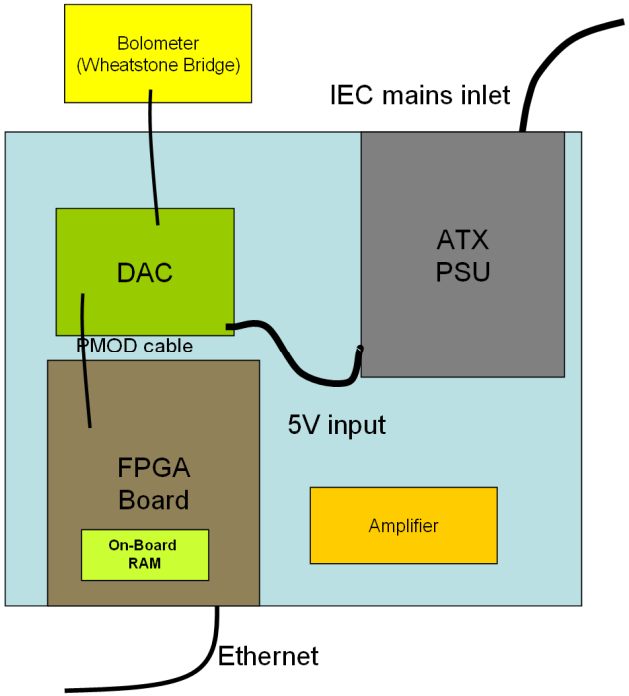
Synchronous detection – Bolometer Upgrade

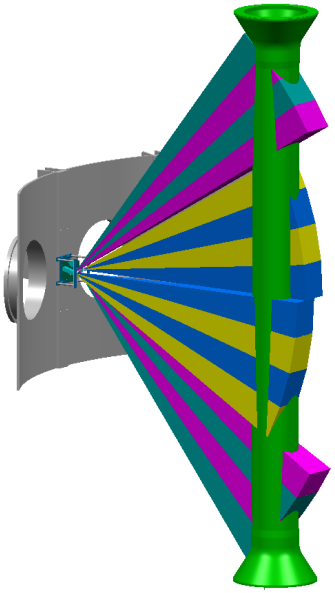
The MAST 32 channel bolometer array is used to image plasma irradiation energy.

In development: Simplified conceptual system below.

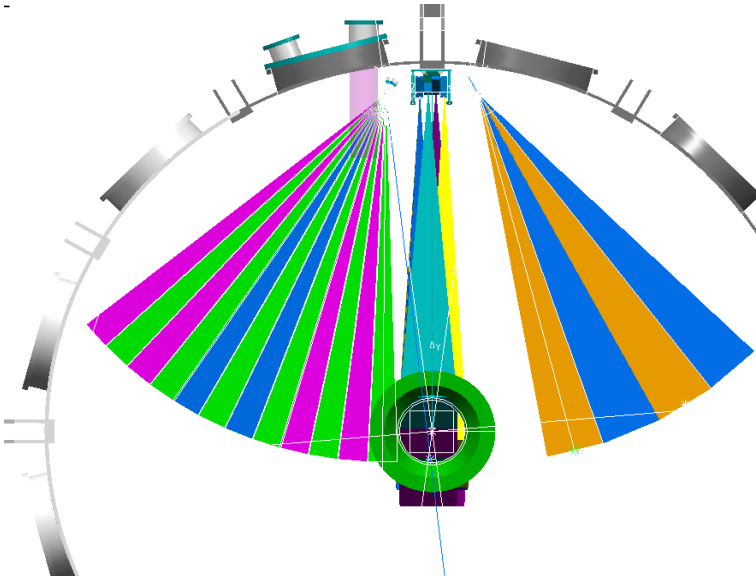








Vertically on the centre column

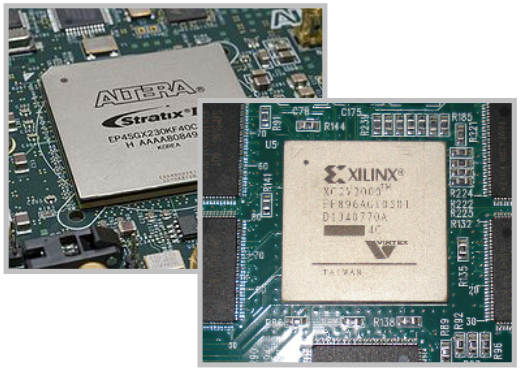


Tangentially through the tokamak

Standardisation of an FPGA system

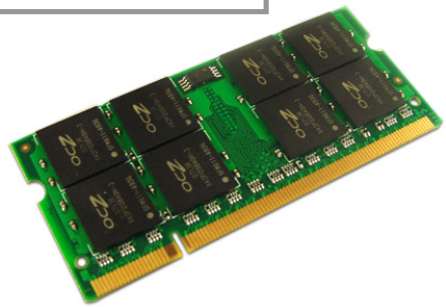
FPGA Firmware

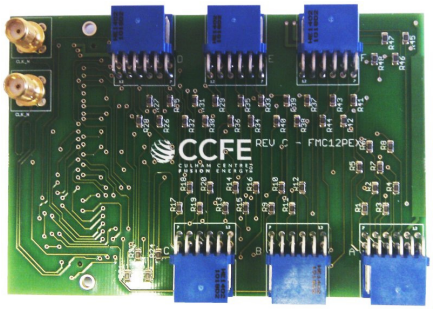
FPGA



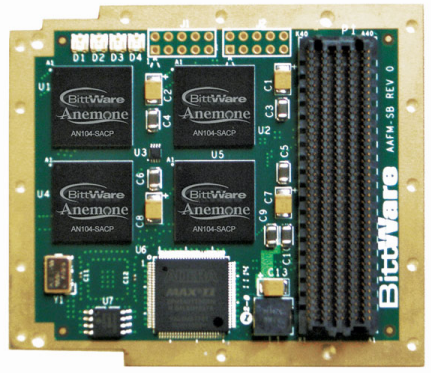
Communication Interface

Memory





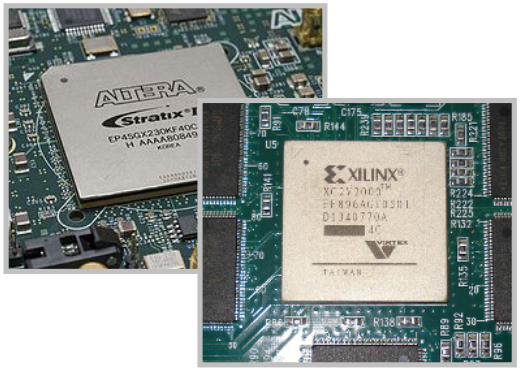
I/O



Standardisation of an FPGA system

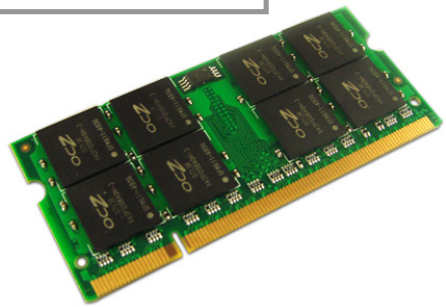
BPI/Compact/SD Flash

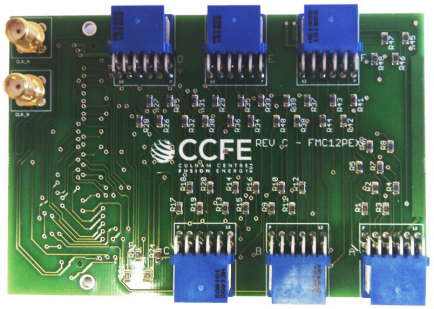
FPGA



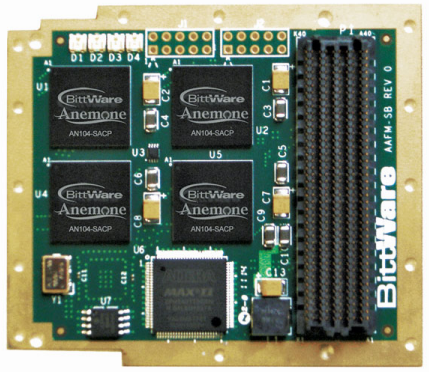
Gigabit Ethernet

DDR3



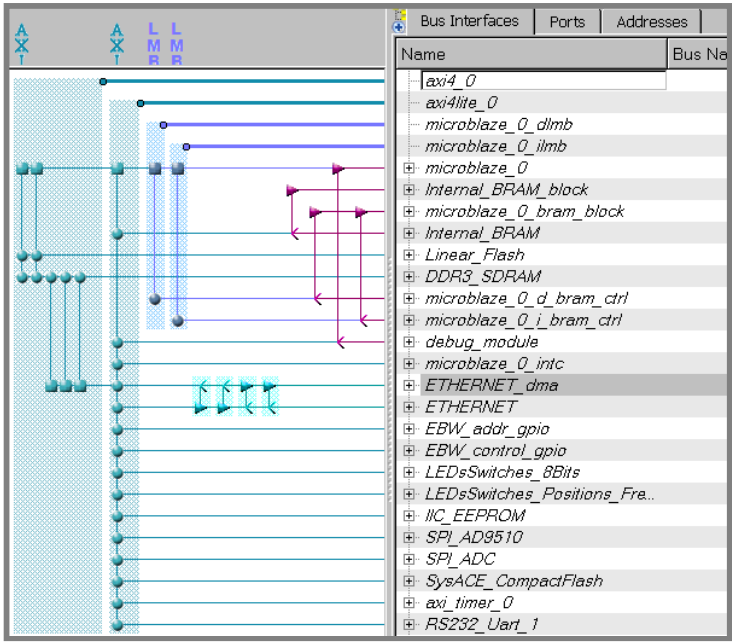


FMC



AXI Bus

- The AXI Bus is supported on Xilinx FPGAs and becoming supported on Altera FPGAs. The AXI bus can be 256+ bits wide at 200MHz. Translates to 51.2+ Gbps bus lines, such as to a memory DIMM or other peripherals.

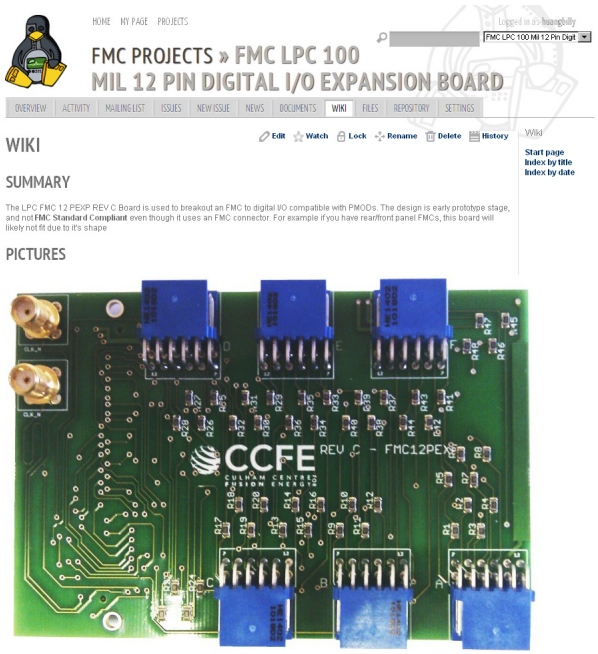


AXI bus viewed in Xilinx Platform studio

- AXI is easy to develop for and could be integrated in future with the ARM processor, such as anticipated for the ZYNQ FPGA using a dual core 1GHz ARM processor.

Open Hardware

- For FPGA dev: www.opencores.com
  - Many open cores. Some of these are supported in the mainline Linux kernel.
- For Hardware: www.ohwr.org
  - We have moved our design for the LPC FMC12PEXP (I/O FMC Expansion board) to the OHWR, a first step into sharing hardware design.



A small first contribution towards open hardware.

Summary

- A generic methodology for developing FPGA systems on MAST has been used successfully to develop a variety of FPGA systems – both simple and complex.

- Developing hardware systems that can perform complex functionality relies not just on assembling the right hardware, good investment in the development using open-source software where possible allows the integration of these systems.

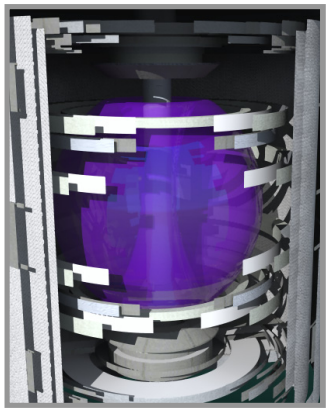
FPGA Workshop 2012

- Building on last year, we will be running another hands-on FPGA Workshop at CCFE, Oxfordshire, UK in early February 2012. It will include embedded Linux and FPGA development. Please email billy.huang@ccfe.ac.uk if you are interested in joining.

Thanks

- Thanks to all the authors with whom I have worked with on a variety FPGA systems and who have given huge amounts of work and effort only briefly glanced at in this presentation.

- Thanks to you for listening!



- **Extra info at http://www.ccfe.ac.uk/fpga**