Open Hardware for CERN's Accelerator Control Systems

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CERN, Geneva, Switzerland

ICALEPCS 2011

Outline

Outline

CERN Beams Controls group

Responsible for

- Controls infrastructure for all CERN accelerators, transfer lines and experimental areas
- General services such as machine and beam synchronous timing and signal observation
- Specification, design, procurement, integration, installation, commissioning and operation

Supports

- beam instrumentation, cryogenics, power converters etc.

Software

- Linux device drivers, C/C++ libraries, test programs

Beams Controls standard kit

Hardware kit

- analog and digital I/O
- level converters, repeaters
- serial links, timing modules

Currently, end 2011

- about 120 module types
- most are custom designed: only 1 in 4 is commercial
- 1 in 4 is obsolete

Outline

Bus standards for new designs

Two bus standards

- VME64x
  - 6U, large front-panel space, may use rear transition module
- PICMG 1.3
  - Industrial type PC with the processor on a plug-in board
  - Internal buses PCI Express and PCI

Need for a mezzanine approach

- Functions (e.g. ADC, TDC) are needed for both buses
- Would need twice as many designs, more if additional standards are needed (PXIe, xTCA)

Advantages of the carrier/mezzanine approach

Re-use

- One mezzanine can be used in VME and PCIe carriers.
- People know standards, more likely to re-use or design for it.

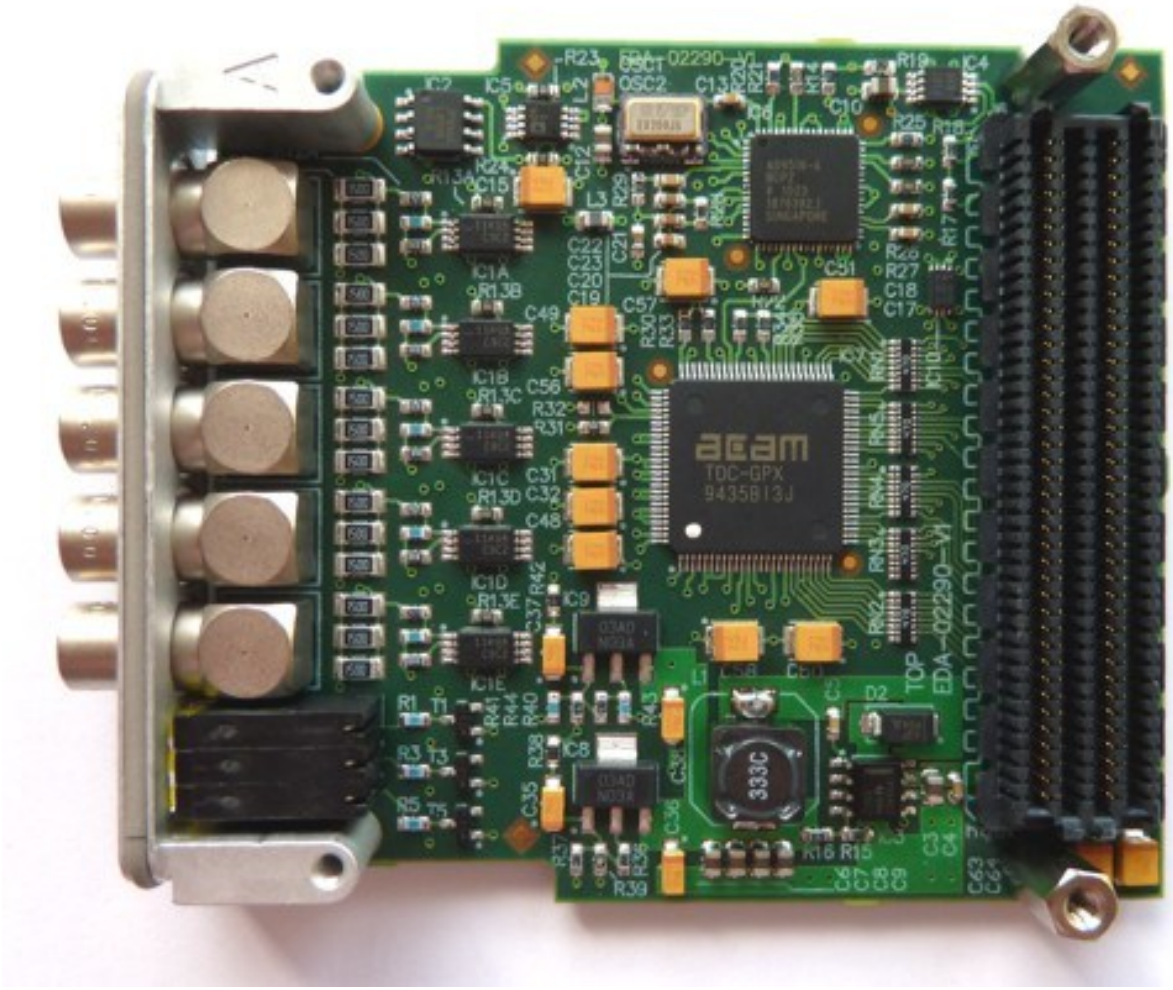
Reactivity

- Carrier: place and route a complex FPGA/Memory PCB once.
- Mezzanine: small and easier to route cards, easy assembly.

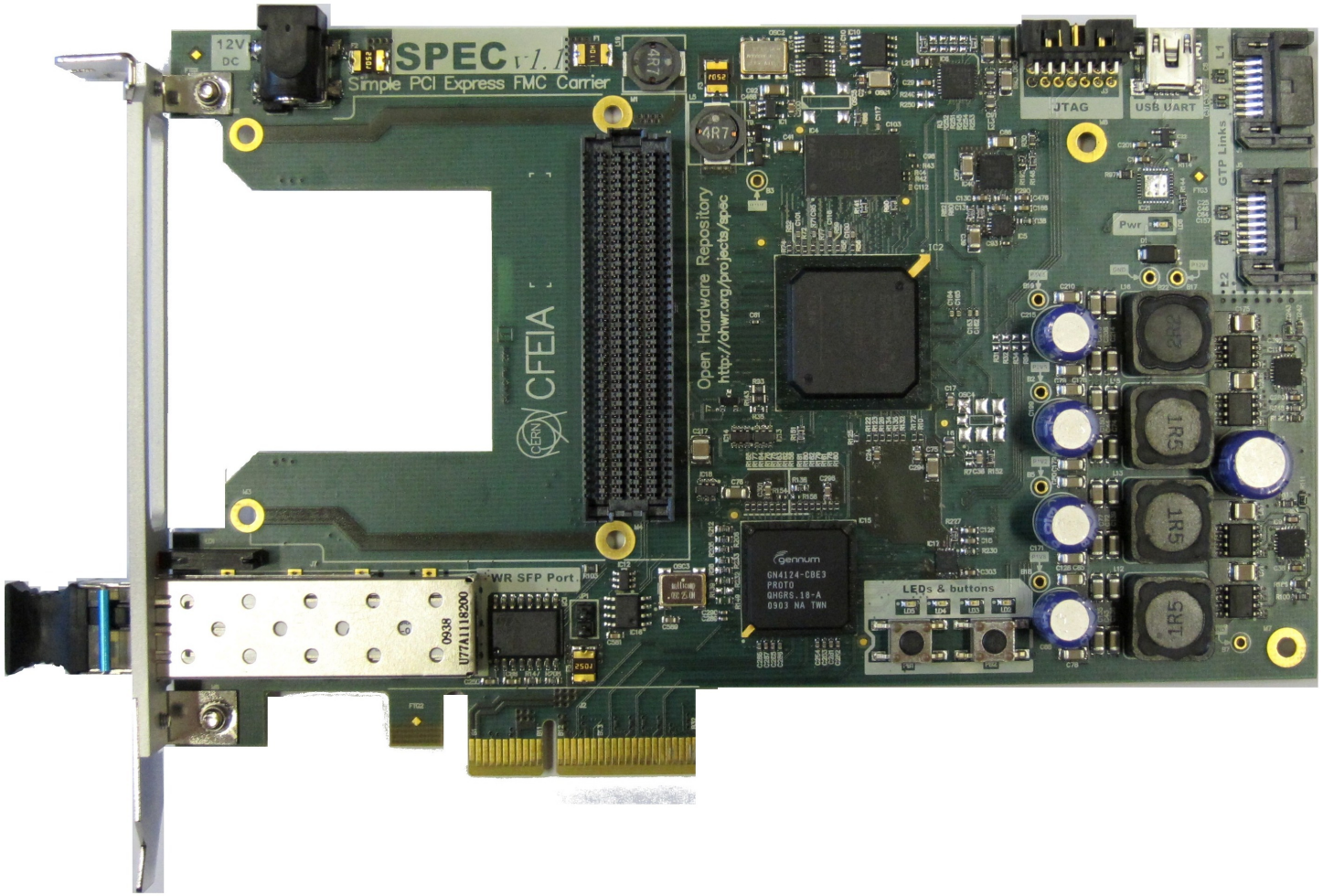
Rational split of work

'Controls' can design the carrier, 'Instrumentation' an ADC mezzanine, 'RF' a DDS one, etc.

Example of an FMC mezzanine: 5-channel 1ns TDC



Example of a PCI Express FMC carrier (SPEC)



Inside the FPGA: Wishbone

- System becomes pretty complex: System-on-a-chip
- Build up from re-usable IP blocks
- Connect blocks with Wishbone bus
  - open standard
  - simple address/data bus
  - extended with pipelined mode
  - many cores already available
- We developed a design infrastructure
  - scripts to interconnect Wishbone IP blocks
  - IP blocks with descriptors to aid driver development
  - support to compile designs with distributed sources
  - library of Wishbone IP blocks

Outline

Why we use Open Hardware

Get a design just the way we want it

We specify fully the design.

Peer review

Get your design reviewed by experts all around the world, including companies!

Design re-use

When it's Open, people are more likely to re-use it.

Healthier relationship with companies

No vendor-locked situations. Companies selected solely on the basis of technical excellence, good support and price.

Open Hardware Repository – ohwr.org

A web-based collaborative tool for electronics designers

- Wiki, News
- File repository
- Issues management
- Mailing list

Fully open access

- All information readable by everyone, without registration

Server made itself of open software

- ChiliProject (a fork of Redmine)
- SVN/GIT for version management, integrated in OHR

Example of an OHR project

HOME MY PAGE PROJECTS

Logged in as erikva

» Si

FMC PROJECTS » SIMPLE PCIE FMC CARRIER (SPEC)

OVERVIEW | ACTIVITY | MAILING LIST | ROADMAP | ISSUES | NEW ISSUE | NEWS | DOCUMENTS | WIKI | FILES | REPOSITORY | SETTINGS

OVERVIEW

A simple 4-lane PCIe carrier for FPGA Mezzanine Cards (VITA 57). It has memory and clocking resources and supports the White Rabbit timing and control network.

- **Detailed project information**
- Subprojects: **Software support for the SPEC board**
- Status: Beta
- Licence: CERN OHL

OHR Status
October 2011

Projects

- 46 active projects
  - 38 initiated by CERN groups, 8 by other institutes
- 3.6 developers on average

Types of designs

- About 30 hardware designs (of which 20 FMC projects)
- About 20 re-usable IP blocks
- General tools
  - Production test environment (Python based)
  - ADC performance test

CERN FMC projects in OHR – some examples

FMC Carriers

- VME64x (BE/BI), PCIe (BE/CO), AMC (PH/ESE), VXS (BE/RF)
- PXIe likely to come (EN/ICE)

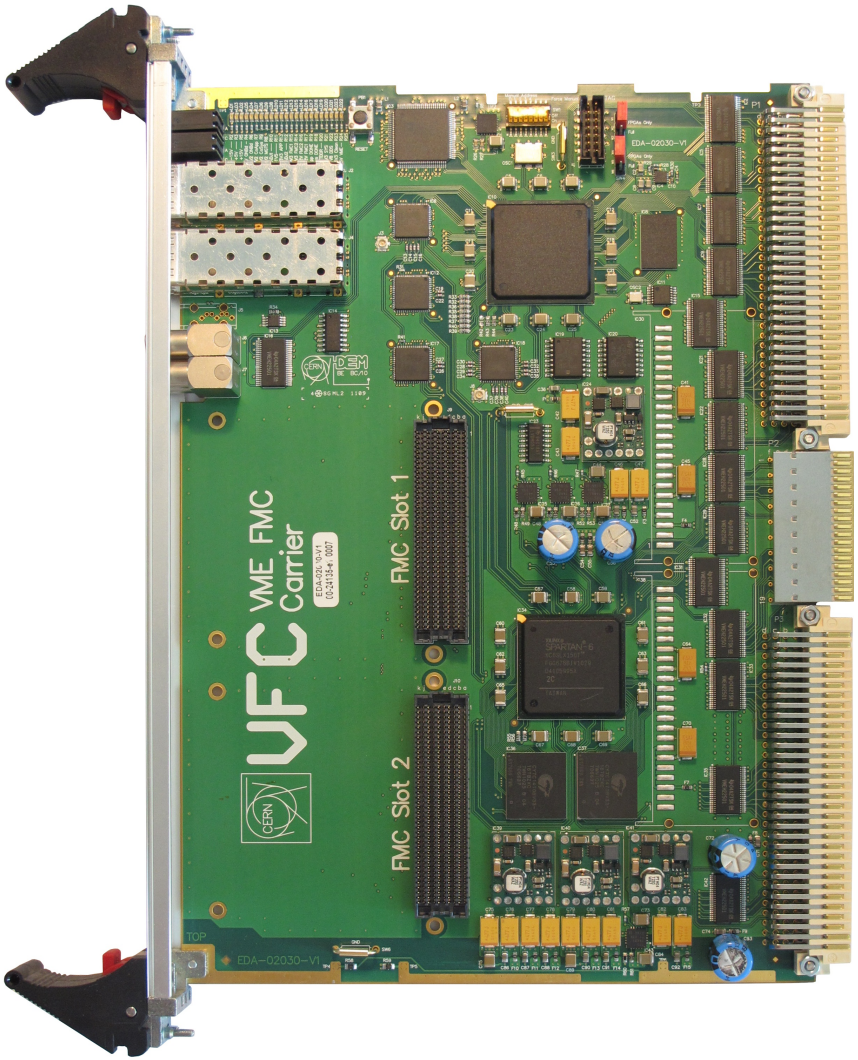
FMC Mezzanines

- ADC's, sampling speeds: 100 kSPS, 100 MSPS
- TDC and Fine delay (resolution 1 ns)
- Digital I/O: 5 channels, 16 channels

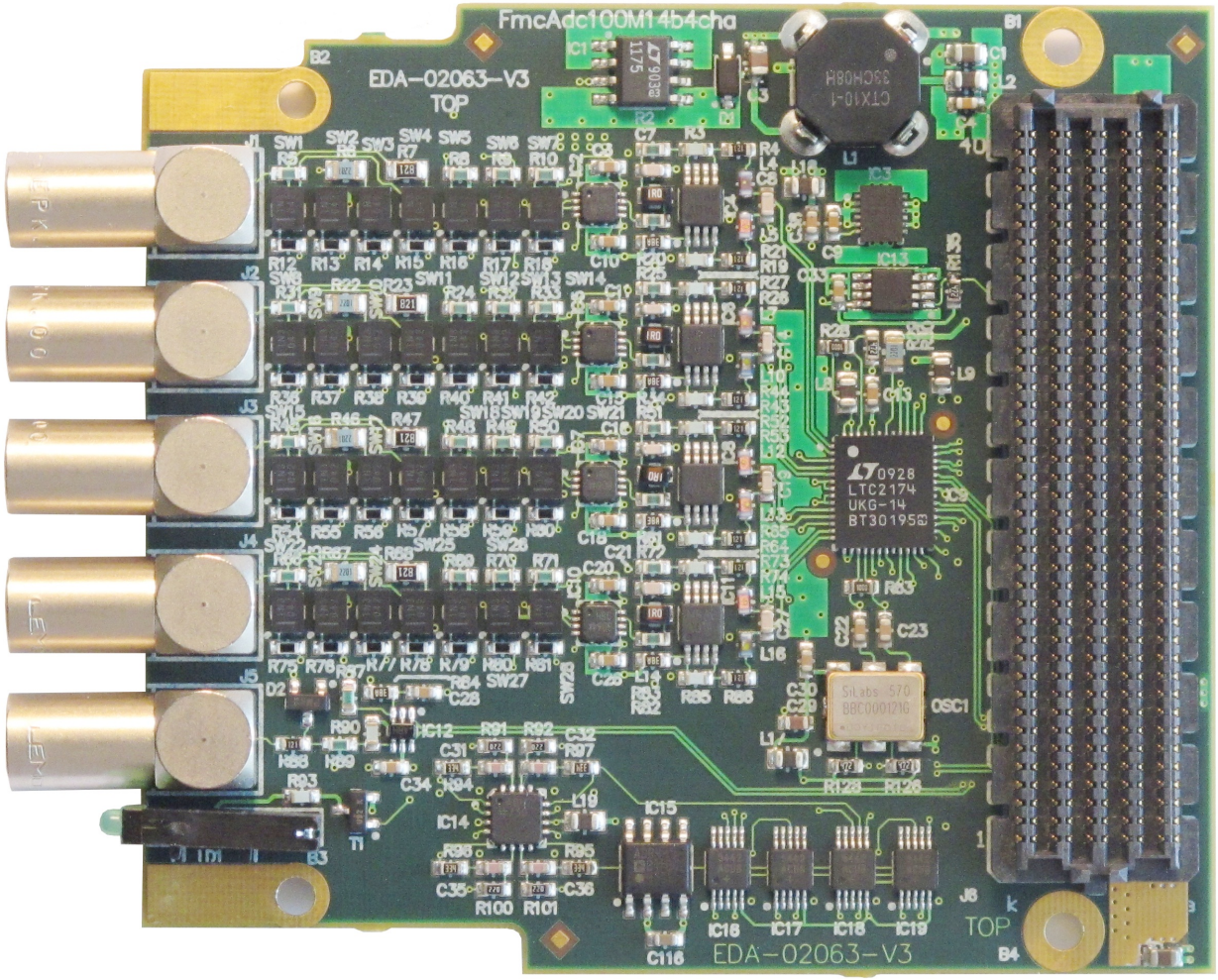
Stimulates collaboration between CERN groups

- VME64x: BE-BI & BE-CO
- TDC: TE-ABT, TE-CRG & BE-CO

VME64x FMC carrier



FMC mezzanine: 100 MSPS 14-bit 4-channel ADC



CERN non-FMC projects in OHR – some examples

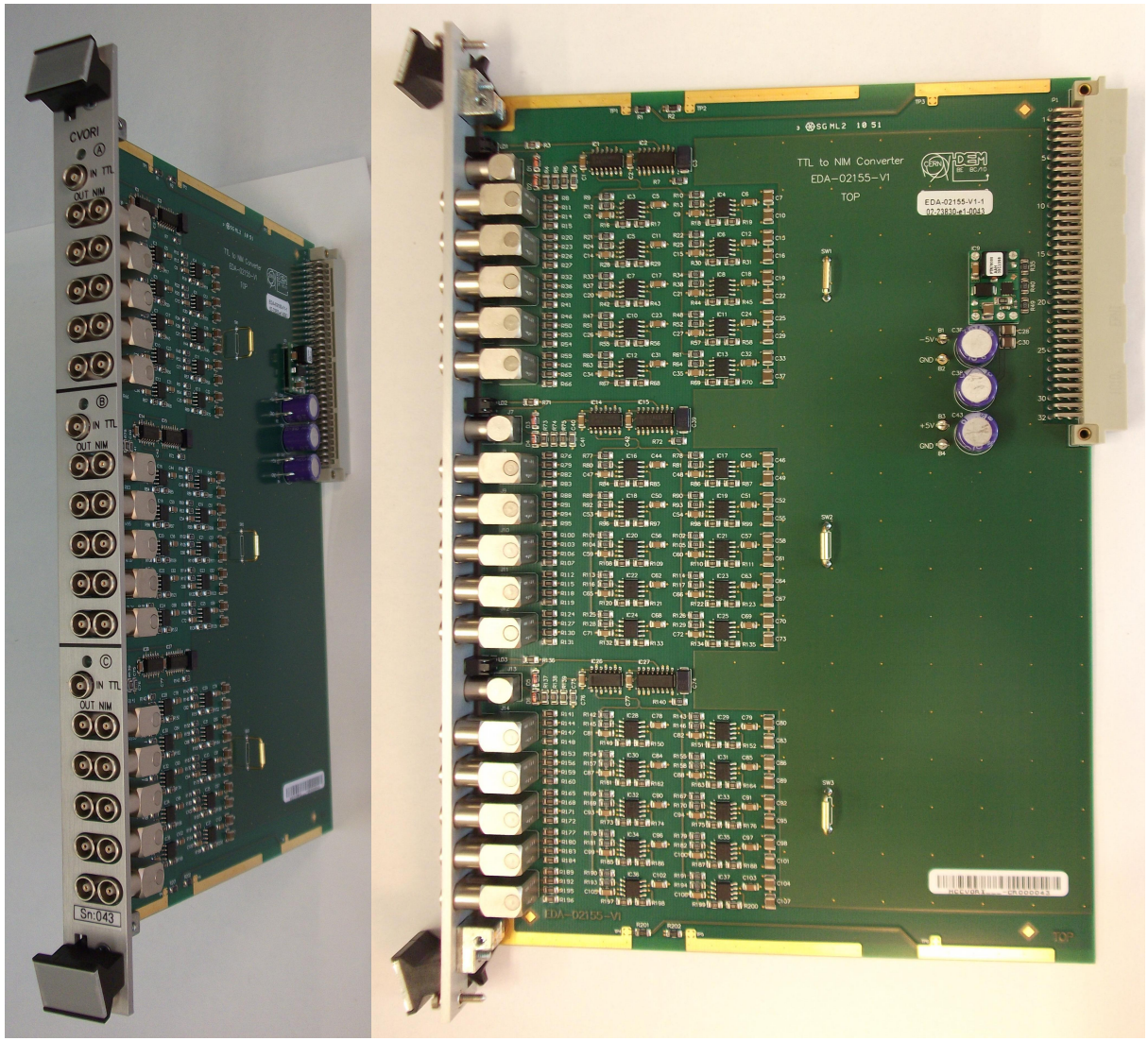
Hardware

- TTL to NIM level converter (VME)
- White Rabbit timing network switch
- Small footprint ARM-based computer

IP modules, Software and Tools

- Wishbone cores: DDR3 controller, VME64 core, serialiser
- RISC Processor core
- Time-to-Digital Converter core
- NanoFIP WorldFIP interface
- Production test environment (Python based)

TTL to NIM converter



CERN Open Hardware License – ohwr.org/cernohl

Provides a solid legal basis

- Developed by Knowledge and Technology Transfer Group at CERN
- Open Software licences not usable (GNU, GPL, . . .)
- Defines conditions of using and modifying licenced material

Practical: makes it easier to work with others

- Upfront clear that anything you give will be available to everyone
- Makes it clear that anyone can use it for free

CERN Open Hardware License – ohwr.org/cernohl

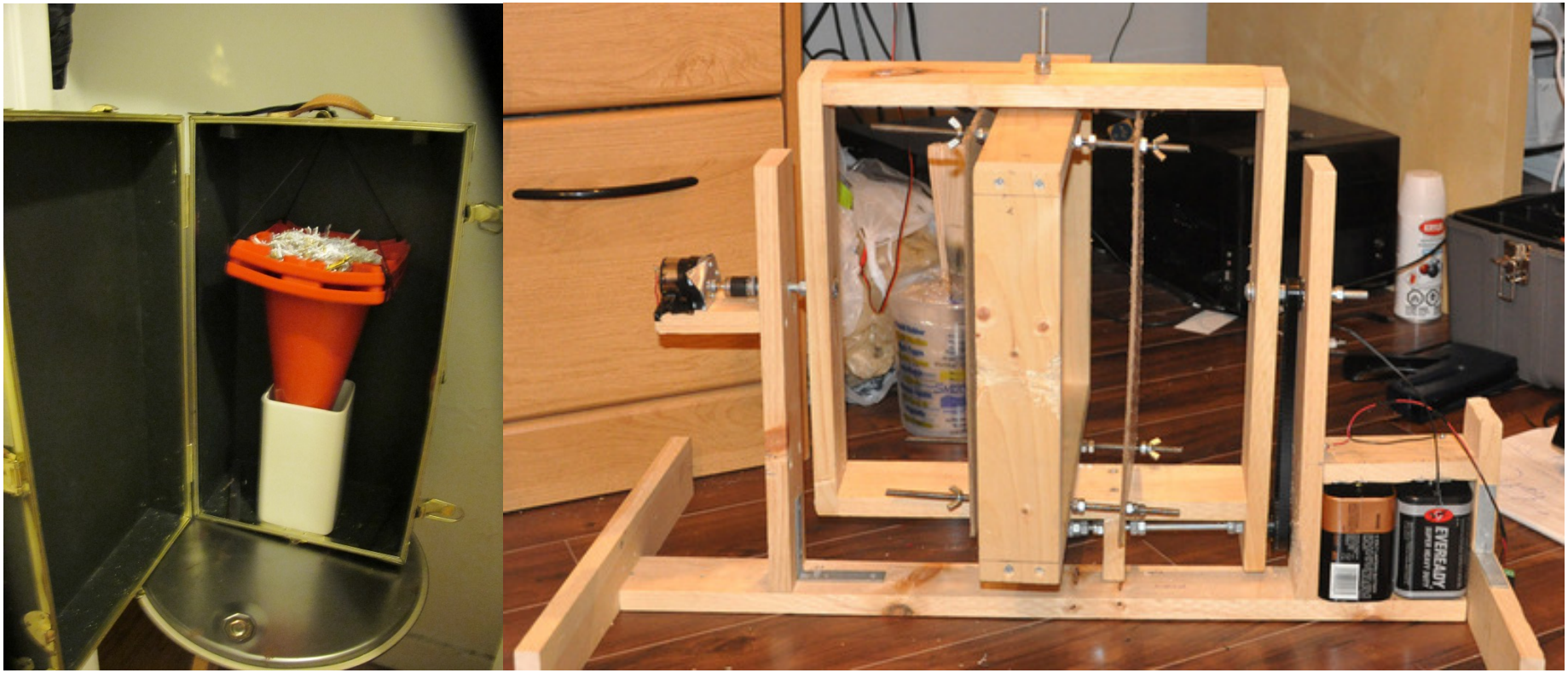
Same principles as Open Software

- Anyone can see the source (design documentation)
- Anyone is free to study, modify and share
- Any modification and distribution under same licence
- Persistence makes everyone profit from improvements

Hardware production

- When produce: licensee is invited to inform the licensor

Example of mechanics licenced with the CERN OHL



Worm farm and rotocaster

Outline

Case study – SPEC – Simple PCI Express Carrier

We started with a complex design

- Our first FMC carrier design
- Wanted to have lots of timing things on it
- Wanted it to be very flexible: one design does it all

And got results

- We built a few prototypes
- Actually a bit overdesigned, too complex and expensive

Case study – SPEC

PCIe FMC Carrier (PFC)

Case study – SPEC

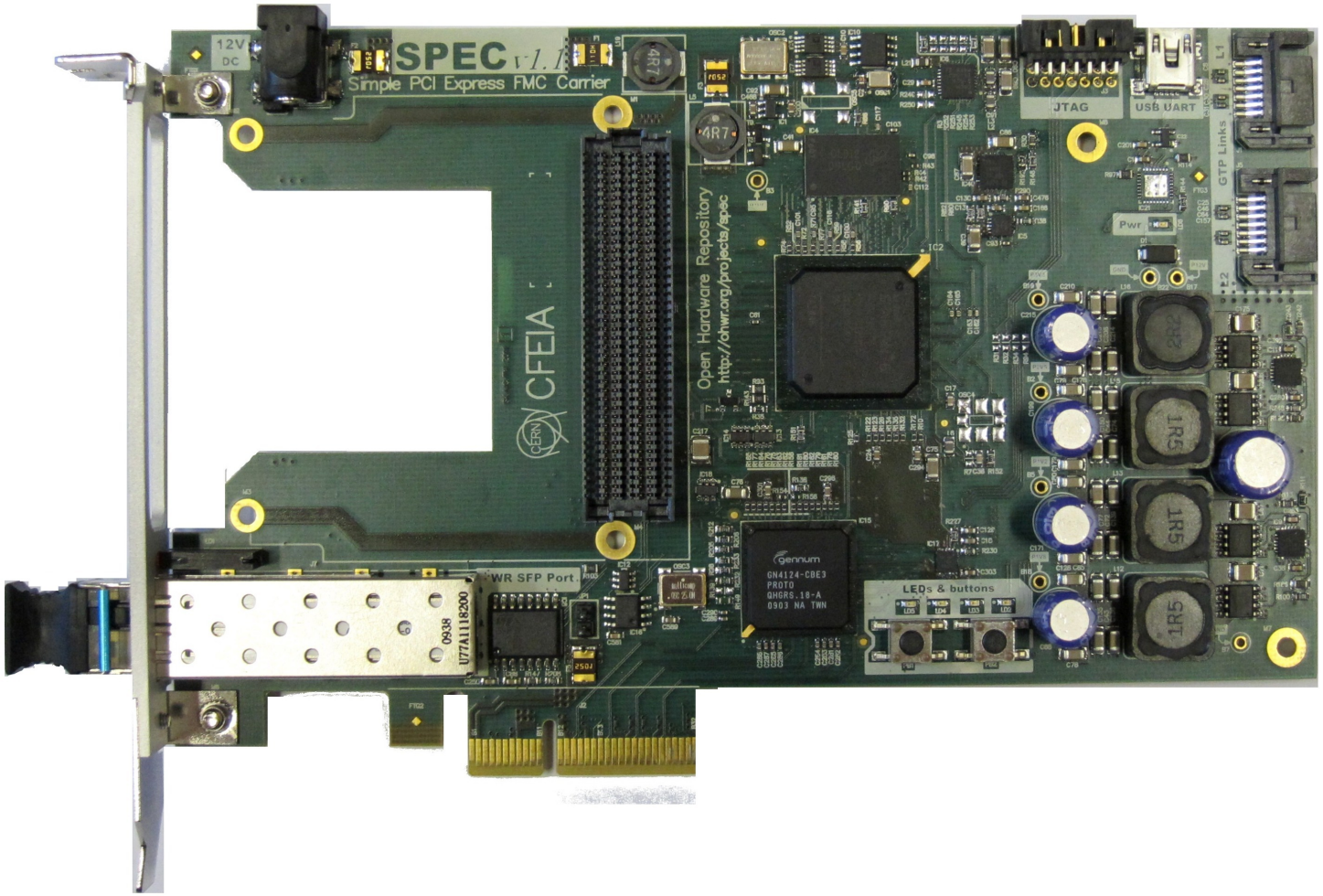
Too complex, so we wanted to have a simpler board

- Simple PCI Express Carrier (SPEC)
- Basically remove components from old design
- Optimise with new knowledge and re-layout

Industry got in

- We didn't have time to do the work
- Hired a small **company** ($<$15 persons)
- Review, review, review (specifications, schematics, pcb)
- CERN's design office generated final production files
- Used ohwr.org for all documentation

Case study – SPEC: Simple PCI Express FMC carrier



6-layer PCB instead of 12 on the PFC

Case study – SPEC

Make it a testable product

- Developed an FMC connector test card
- Developed a re-usable test environment (using Python)
- Developed go/no-go test suite

Redesign: V1, V1.1, V2, (V3,) V4

- 52 Issues registered and tracked in ohwr!

First series of 70 boards (production, guarantee)

- Solid specification, IPC norms for PCB fab and assembly
- Price Enquiry to 7 **companies** *having already PCIe products*. First delivery in December 2011.

Case study – 100 MSPS 14-bit 4-channel ADC

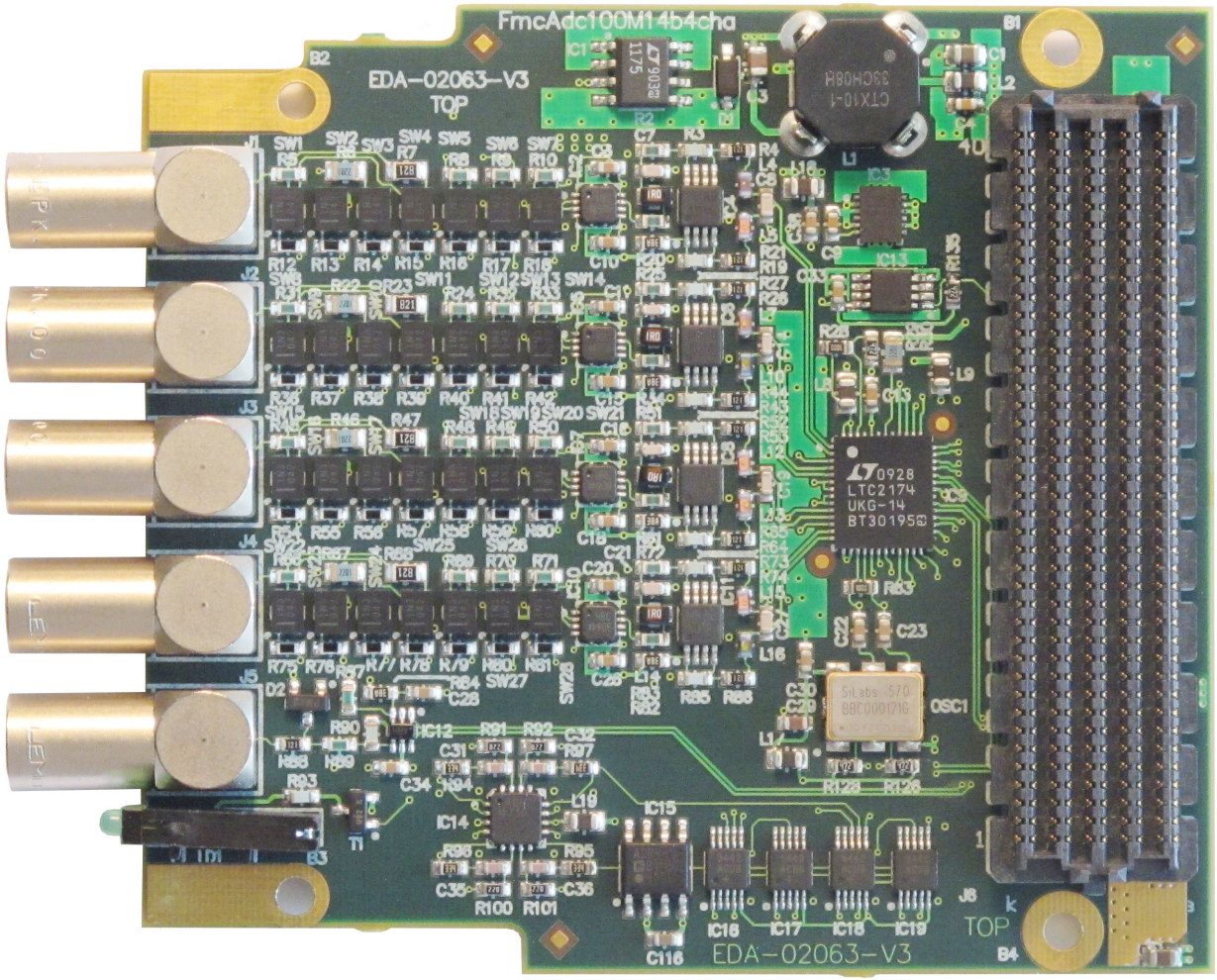
Design

- Design by CERN student
- A small specialist **company** designed the front-end
- Review, review, review
- Design process well documented (mails, documents)
- 46 Issues documented
- 4 prototype versions, produce V5

CERN Price Enquiry for 40 boards (production, guarantee)

- Price Enquiry to five companies *that produce ADC boards*
- Useful design feedback (schematics and PCB layout) from **company**. Delivery in January 2012.

Case study – 100 MSPS 14-bit 4-channel ADC



Case study – 100 MSPS 14-bit 4-channel ADC

Potential users who contacted us

- BPM Linac4 (CERN BE/BI)
- Frame grabber for BSRT emittance meter (CERN BE/BI)
- PSB pick-ups (CERN BE/BI)
- Septum. Booster Trajectory Measurement (CERN TE/ABT)
- OASIS general purpose (CERN BE/CO)
- Italian Hadron Therapy Centre, BPM system (CNAO)
- Agata experiment (INFN, PH/UCM)
- Culham Centre for Fusion Energy (CCFE)
- Advanced Photon Source (Argonne National Laboratory)
- Radio Telescope (Oregan State University)

Experience with Industry

Product Design

- Needs additional effort to make CERN designs a Product
- Particular effort in reducing Bill of Material
- Automated test bench
- Precise production documentation

Industry and the OH concept

- Open Hardware is new and not always understood
- Need to explain companies the opportunities and risks
- Companies think they compete with assembly companies. We ask only companies that can also support (guarantee, repair, improve)
- Needs time from us and guts from companies

Experience with Industry

October 2011

Companies used (usually paid for)

- 12 European companies, 1 US company
- 11 projects

Types of work

- Hardware: development, production
- Software: VHDL firmware, drivers
- Usually small projects ($<$2 months work), speeds up projects, gets in specialist knowledge
- Small companies can play a large role

Experience with Industry

Examples of re-use of work

- Two companies will modify SPEC carrier design
  - larger FPGA (for software radio DSP)
  - PXIe bus instead of PCIe; possibly PXI too (for CERN EN)
- A company re-uses White Rabbit spec for own product
- A company may use nanoFIP for renovating trains

Generates interaction

- One company will help another with product development
- Companies will work together – building an ecosystem
  - One sells a carrier, others sell mezzanines
  - One sells a WR switch, others sell WR nodes

Outline

Why we use Open Hardware

Does it hold its promises?

Get a design just the way we want it – Yes

With own designers and with outside help (industry, institutes).

Peer review – Yes

From different groups. Also by industry.

Design re-use – Yes

- SPEC and ADC100M have users and lots of interest.
- SPEC design is being copied and re-used in other designs.

Healthier relationship with companies – Yes

- Are much more free to use small companies.
- Not tied to any single company.

Conclusions

- The electronics that we support cannot be black boxes.
- Open Hardware has many advantages.
  - Anyone can help in developments and make improvements.
  - Allows to work differently with industry (design work, smaller companies).
  - Not tied to a single company for production and support.
- CERN Open Hardware Licence provides a legal basis.
- Using standards (VME64x, PCIe, FMC, Wishbone) attracts users and improves re-usability.
- OHR site is practical for engineers and is stimulating.
- OHR site contains many re-usable IP modules.
- Many designs being developed and several are already produced by industry.
- Almost three years of experience show it works!