THE UPGRADE PATH FROM LEGACY VME TO VXS DUAL STAR CONNECTIVITY FOR LARGE SCALE DATA ACQUISITION AND TRIGGER SYSTEMS

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OUTLINE

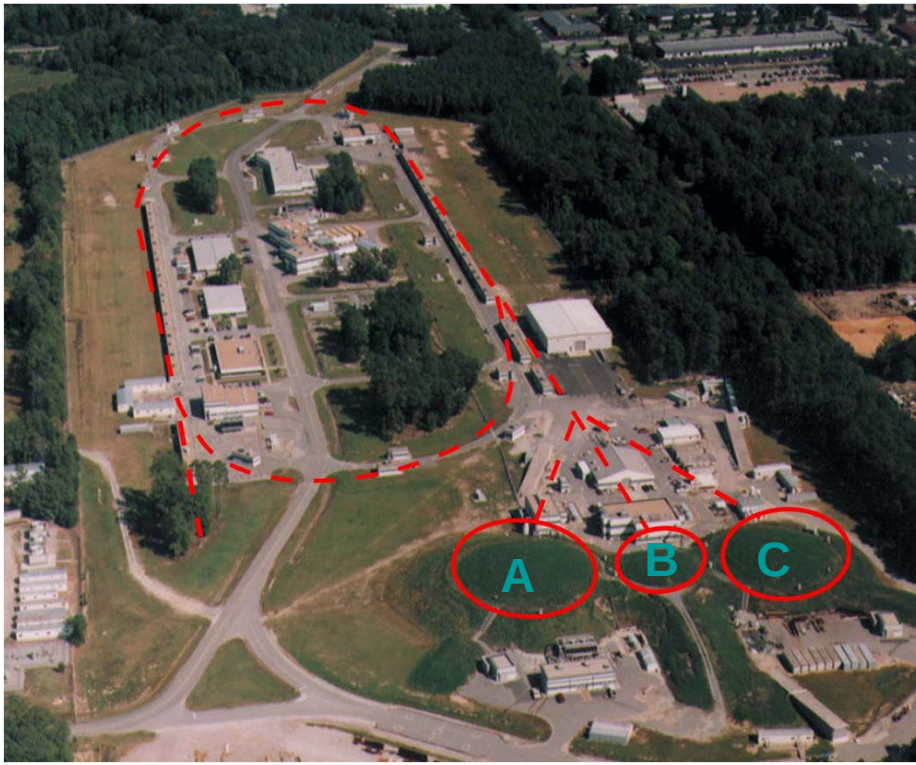
- Jefferson Lab Facility Today
- A Brief History
  - DAq Electronics & Trigger Hardware for 6GeV Experiments
- Jefferson Lab's 12 GeV Upgrade
  - DAq & Trigger Electronics - Design requirements
  - VXS 250MHz pipelined DAq Electronics & Trigger Hardware
  - System Topology and Circuit Board Development
  - Test verification tools – Hardware/Firmware
  - Latest results
  - Summary

JEFFERSON LAB TODAY

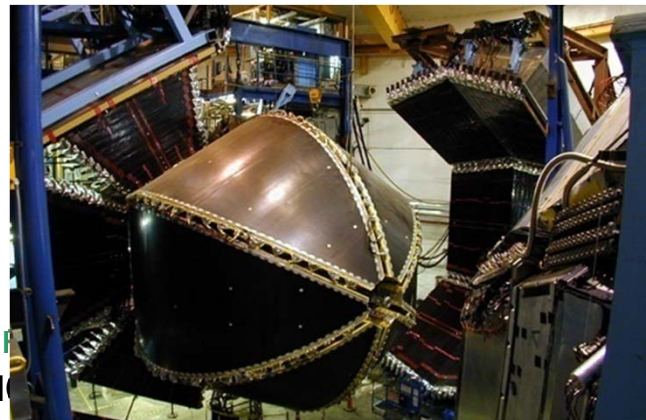
>1200 active member international user community engaged in exploring quark-gluon structure of matter.

Superconducting electron accelerator provides 100% duty factor beams of unprecedented quality, with high polarization at energies up to 6 GeV.

Newport News, VA

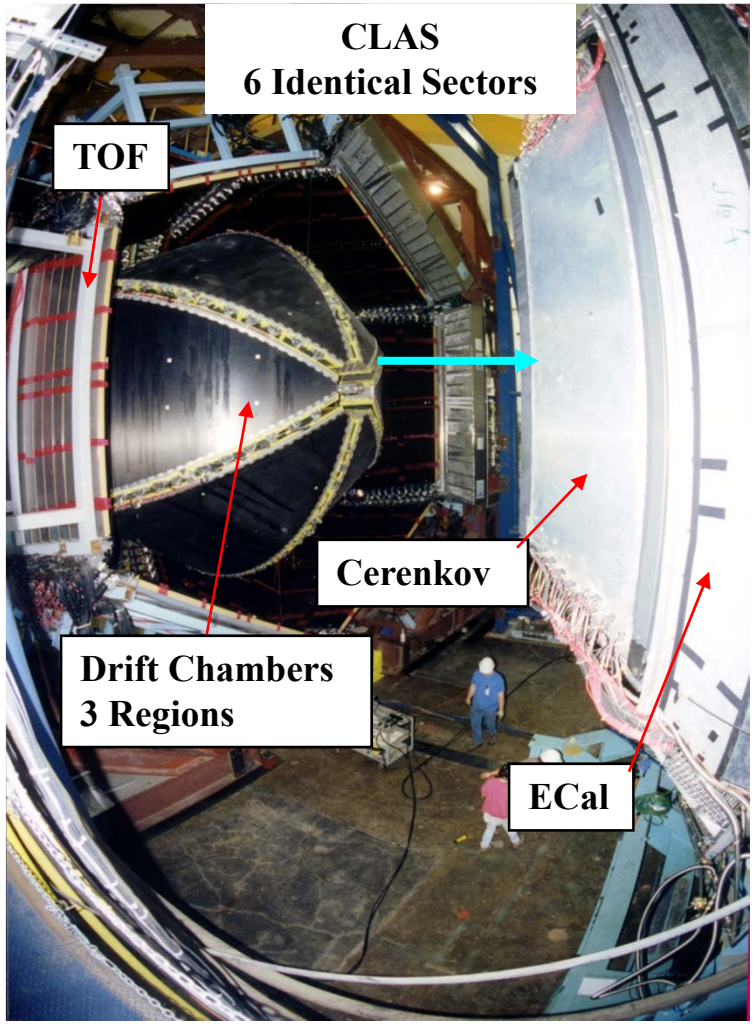


CEBAF's delivery of beam with unique properties to three experimental halls simultaneously. Each hall offers complementary capabilities.

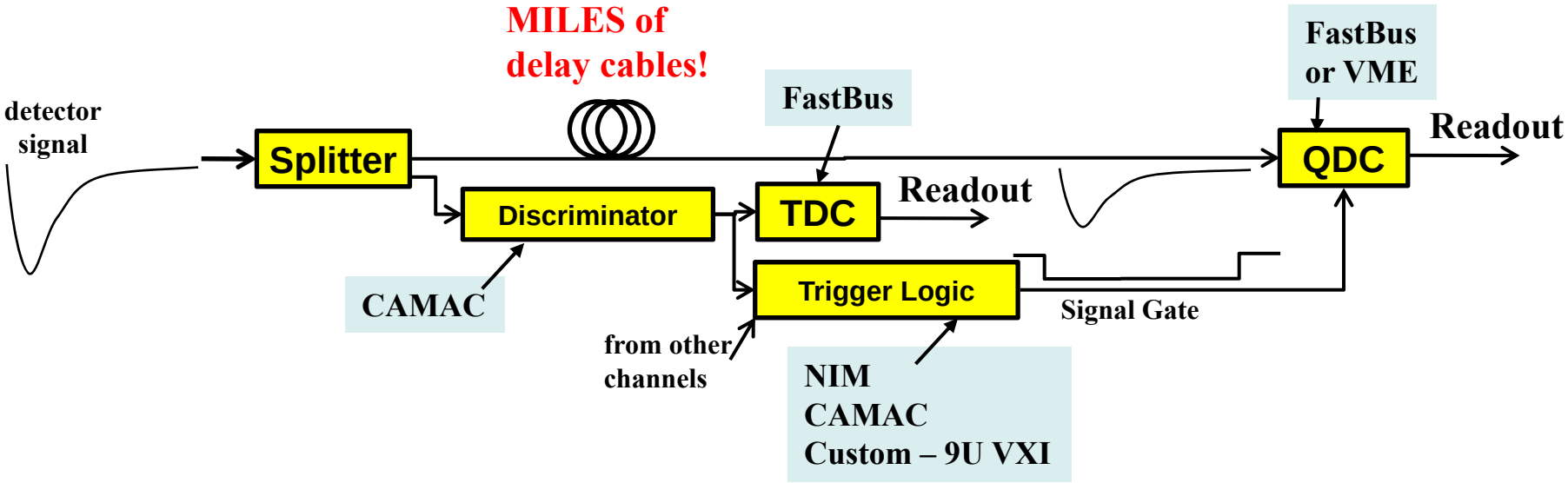


Example 6GeV Experiment
CLAS Detector & Trigger

- **Photon & Electron Experiments with polarized targets, polarized beam**
- **High Luminosities → a few x10^{34}cm^{-2}s^{-1}:**
- **DAQ event rate designed to ~10KHz**
- ***4000 Series Xilinx FPGA based Level 1 Hardware***
  - **Pipeline design, Dead-timeless, (5ns pipeline clock)**
  - **Low latency (~150ns)**
- **Fast Level 1 for ADC Gate, TDC Start**
  - **TOF, Cerenkov, Electromagnetic Calorimeter**
  - **Pattern recognition programming**
  - **Sector based logic for L1 trigger 'equations'**
  - **Cluster finding for Inner Calorimeter**
- **Up to 32 Front End Read_Out_Controllers (ROC)**
  - **Motorola ROC with VxWorks**
  - **Front-End Detector Readout Hardware**
    - ***FASTBUS, VME, [TDC; ADC; Scalers]***



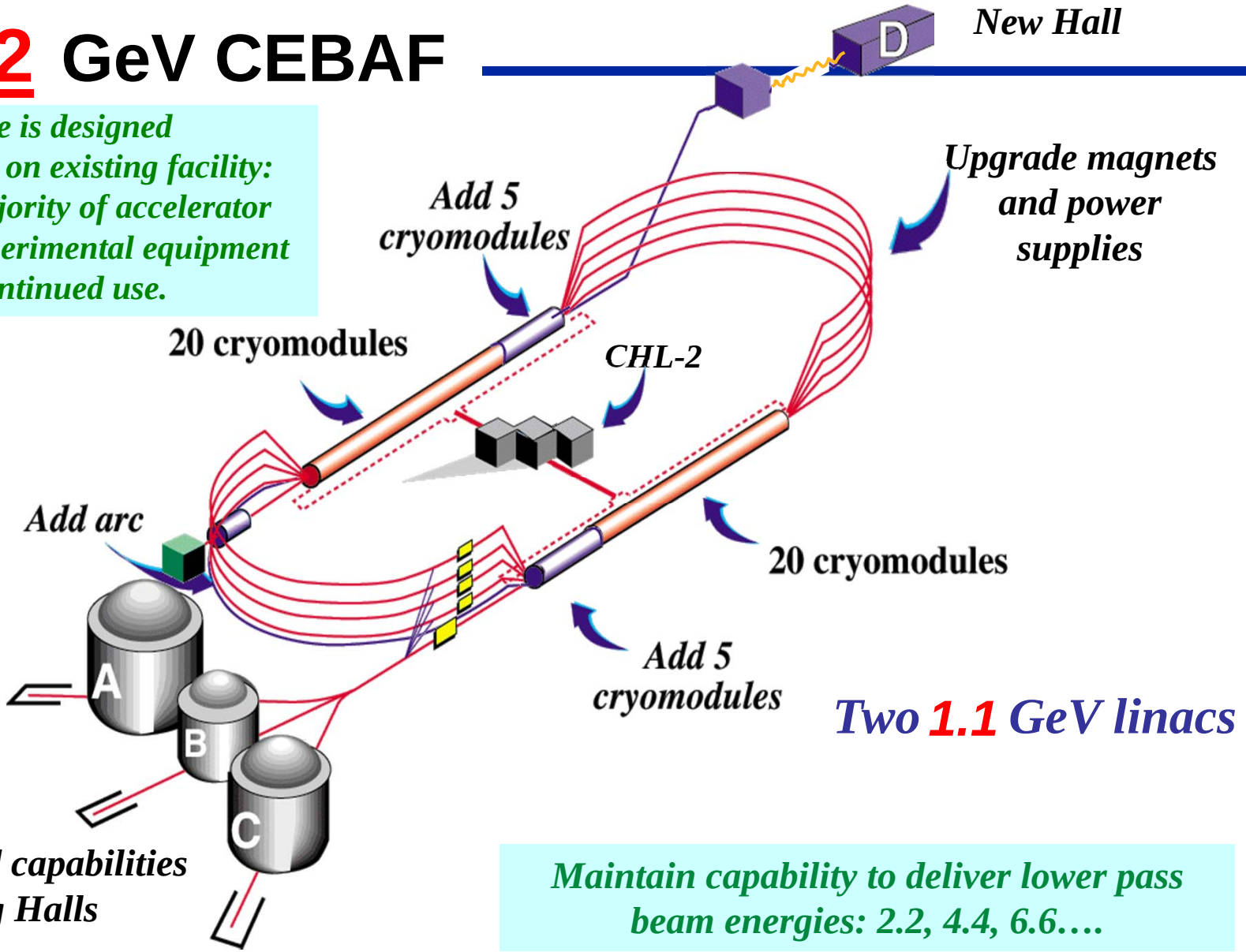
Legacy Method of Signal Capture



- Requires multiple modules to acquire time and/or charge
- Detector signals must be delayed to allow time for trigger decision to form 'gate'
- Very limited trigger logic resolution or very complex/expensive to build
- Gated readout modules typically have large conversion times, creating dead-time

12 GeV CEBAF

Upgrade is designed to build on existing facility: vast majority of accelerator and experimental equipment have continued use.



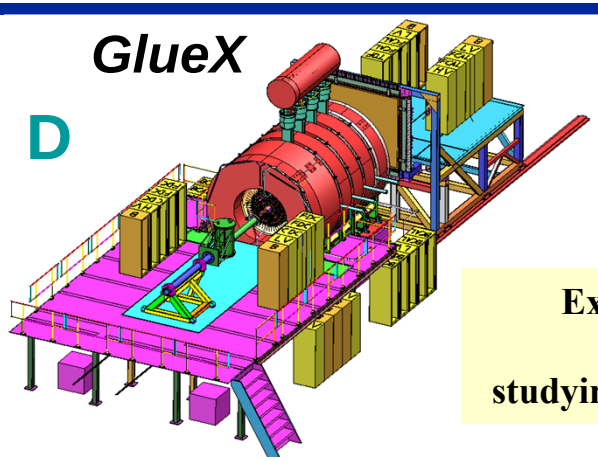
Two 1.1 GeV linacs

Enhanced capabilities in existing Halls

Maintain capability to deliver lower pass beam energies: 2.2, 4.4, 6.6….

New Capabilities In Halls A, B, & C, & New Hall D

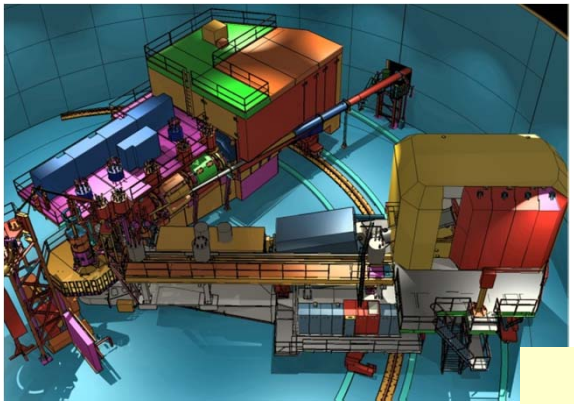
D



9 GeV tagged polarized photons and a 4π hermetic detector

Exploring origin of confinement by studying exotic mesons.

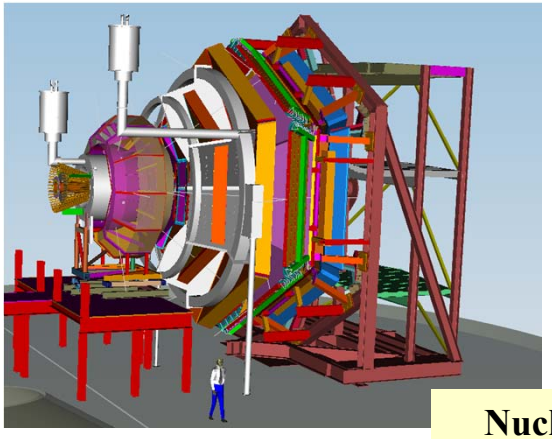
C



Super High Momentum Spectrometer (SHMS)

Precision determination of valence quark properties.

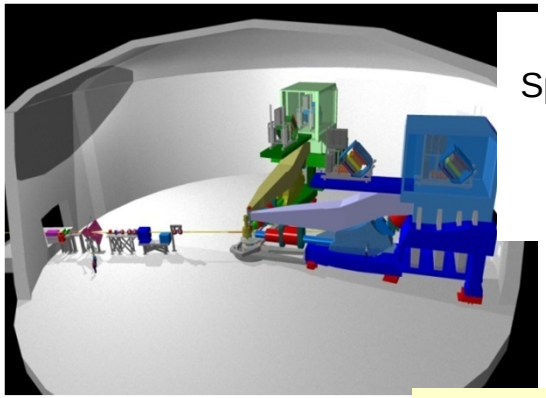
B



CLAS upgraded to higher (10^{35}) luminosity and coverage

Nucleon structure via generalized parton distributions.

A



High Resolution Spectrometer (HRS) Pair, and large installation experiments

SRC, FFs, Hypernuclear, Standard Model studies (PV, Moller)

DAq and Trigger Electronics
For
12GeV Experiments

Requirements

Main Trigger Design Requirements

- 200kHz average Level 1 Trigger Rate, Dead-timeless, Pipelined, 2ns bunch crossing (CW Beam)
- L1 trigger supports sstreaming subsystem hit patterns and energy summing with low threshold suppression
- Scalable trigger distribution scheme (Up to 128 crates)
  - Hall D: 25 L1 Trigger crates, 52 total readout crates
  - Hall B: 38 L1 Trigger crates, 56 total readout crates
- Low cost front-end & trigger electronics solution
- Reconfigurable firmware – Hall B will use different programmable features than Hall D
  - Firmware can be remotely loaded to FPGA from VME

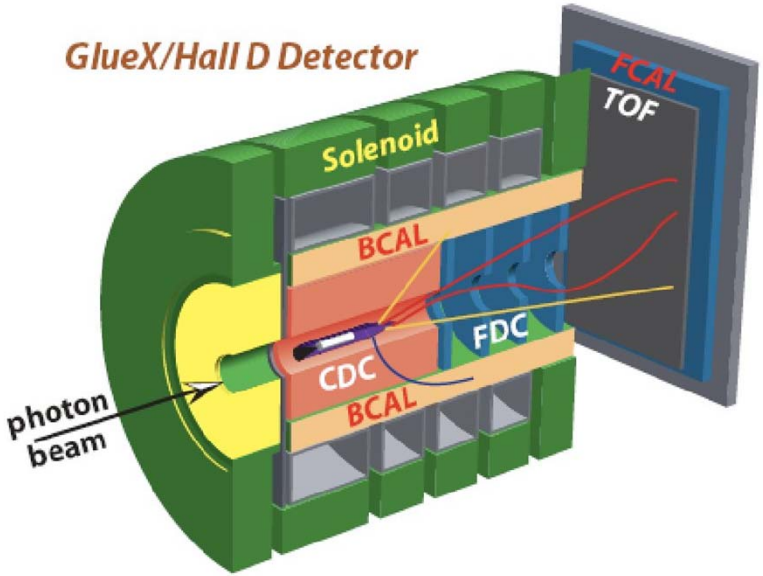
CLAS12 Requirements

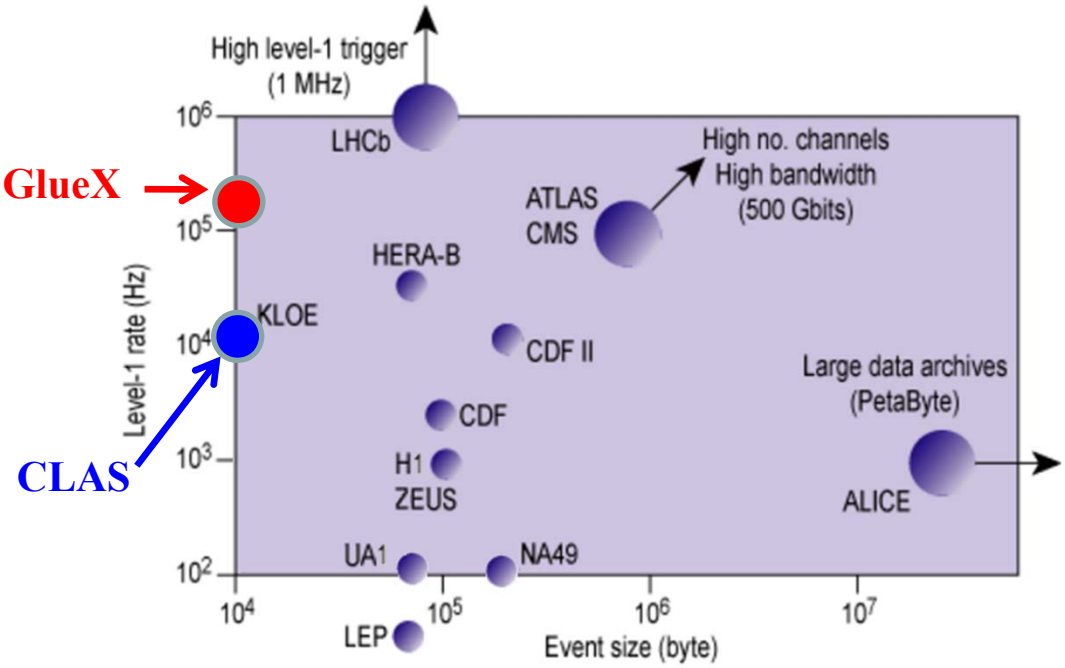
- **Data Acquisition: at least 10kHz event rate, at least 100MB/s data rate, ‘dead-timeless’**
- **Electronics: all new equipment to achieve required performance**
- **Trigger System: reliable electron identification, multi-particle events**

CLAS12 Data Acquisition System

- 3724 channels of 12bit 250MHz Flash ADCs
- 3724 channels of 85ps and 35ps resolution pipeline TDCs with discriminators collecting data from:
  - 2 Calorimeters per sector – PCAL, ECAL
  - 2 Cerenkov counters – HTCC, CC/sector
  - Time-of-flight detectors – CTOF, TOF/sector
- All electronics is compatible with free-running DAQ concept
- 24192 channels from Drift Chambers (TDC w/1ns LSB)
  - Drift Chamber Readout Board with Tracking Trigger Features
- Central tracker readout system
- >50 VME/VME64X/VXS crates equipped with Readout Controllers and Trigger Interface Units
- JLAB Trigger System Modules
  - Benefit from Hall D 200KHz Trigger rate design requirement
- JLAB CODA DAQ software

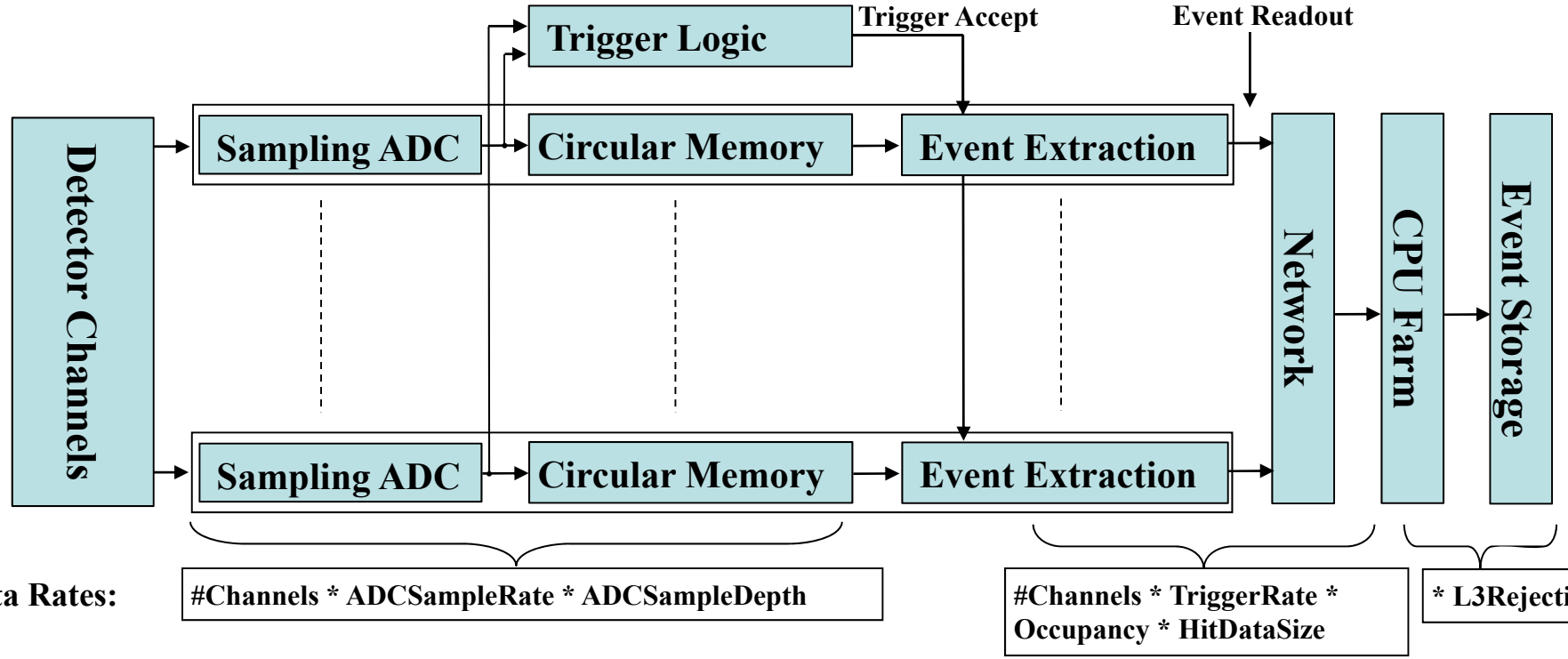
Comparison to CLAS in Hall B





	Hall D-GlueX	Hall B-CLAS
Channel Count:	~20k	~40k
Event Size:	~15kB	~6kB
L1 Rate:	200kHz	10kHz
L1 Data:	3GB/s	60MB/s
To Disk:	L3, 20kHz, 300MB/s	L2, 10kHz, 60MB/s

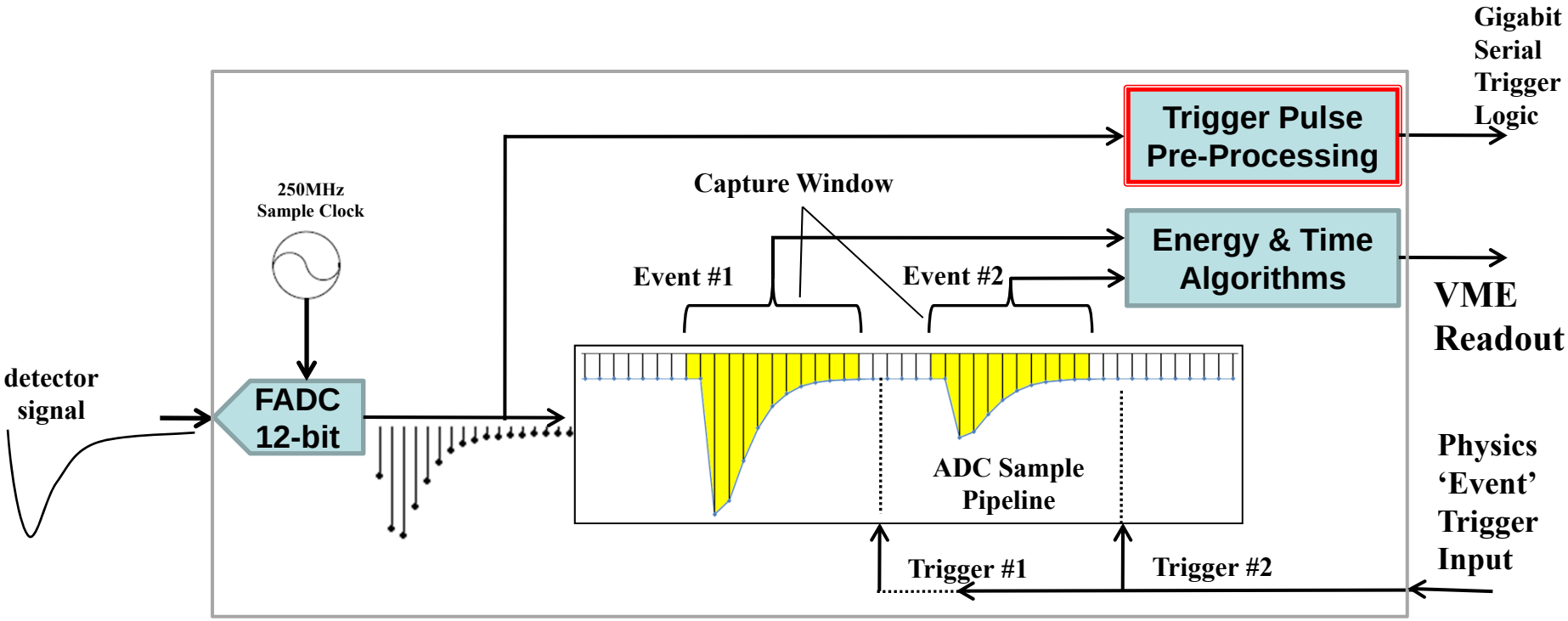
Pipelined DAQ & Trigger Architecture



- All channels are continuously sampled and stored in a short term circular memory

- Channels participating in trigger send samples to trigger logic. When trigger condition is satisfied, a small region of memory is copied from the circular memory and processed to extract critical pulse details such as timing & energy. This essentially makes the event size independent of ADC sampling rate, depth, and number of processed points.

Modern Method of Signal Capture

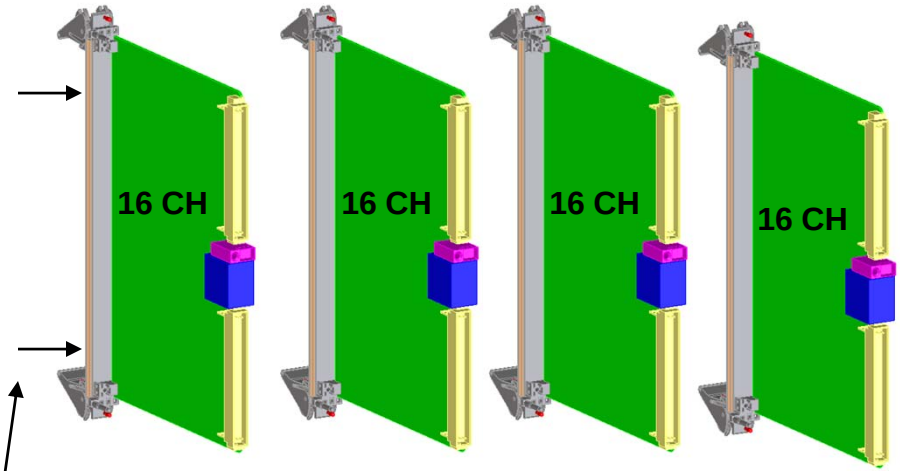


- **250MHz Flash ADC stores digitized signal in 8μs circular memory.**
- **Physics "Event" extracts a window of the pipeline data for pulse charge and time algorithms**
- **Trigger output path contains detailed information useful for cluster finding, energy sum, etc.**
- **Hardware algorithms provide a huge data reduction by reporting only time & energy estimates for readout instead of raw samples**

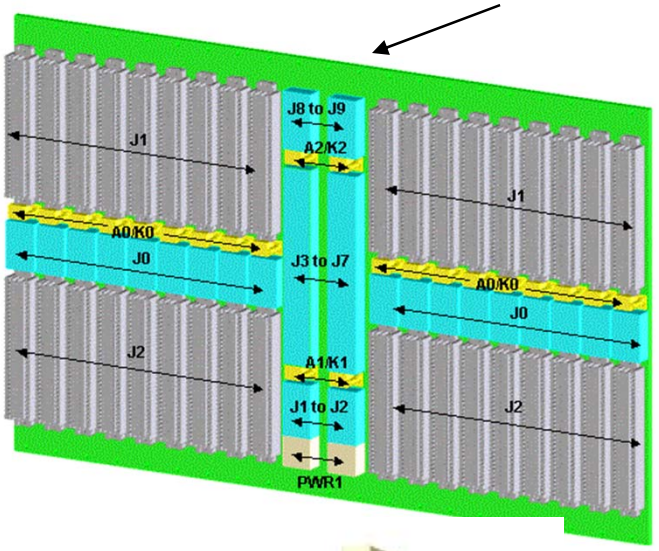
Quick VITA 41 *VXS Review

VXS "Payloads" (JLAB FADC)

(*VME with Serial Extensions)



VXS Backplane

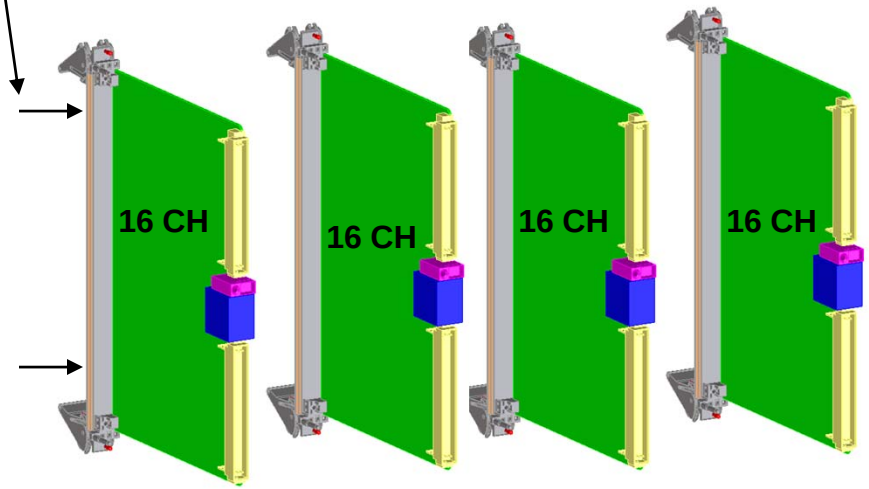


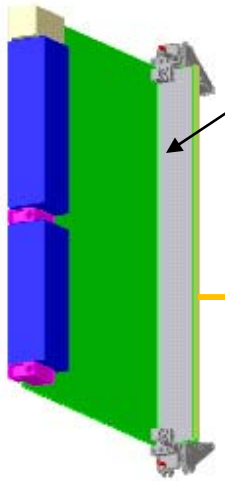
VME64

High Speed Serial

VME64

Detector Signals





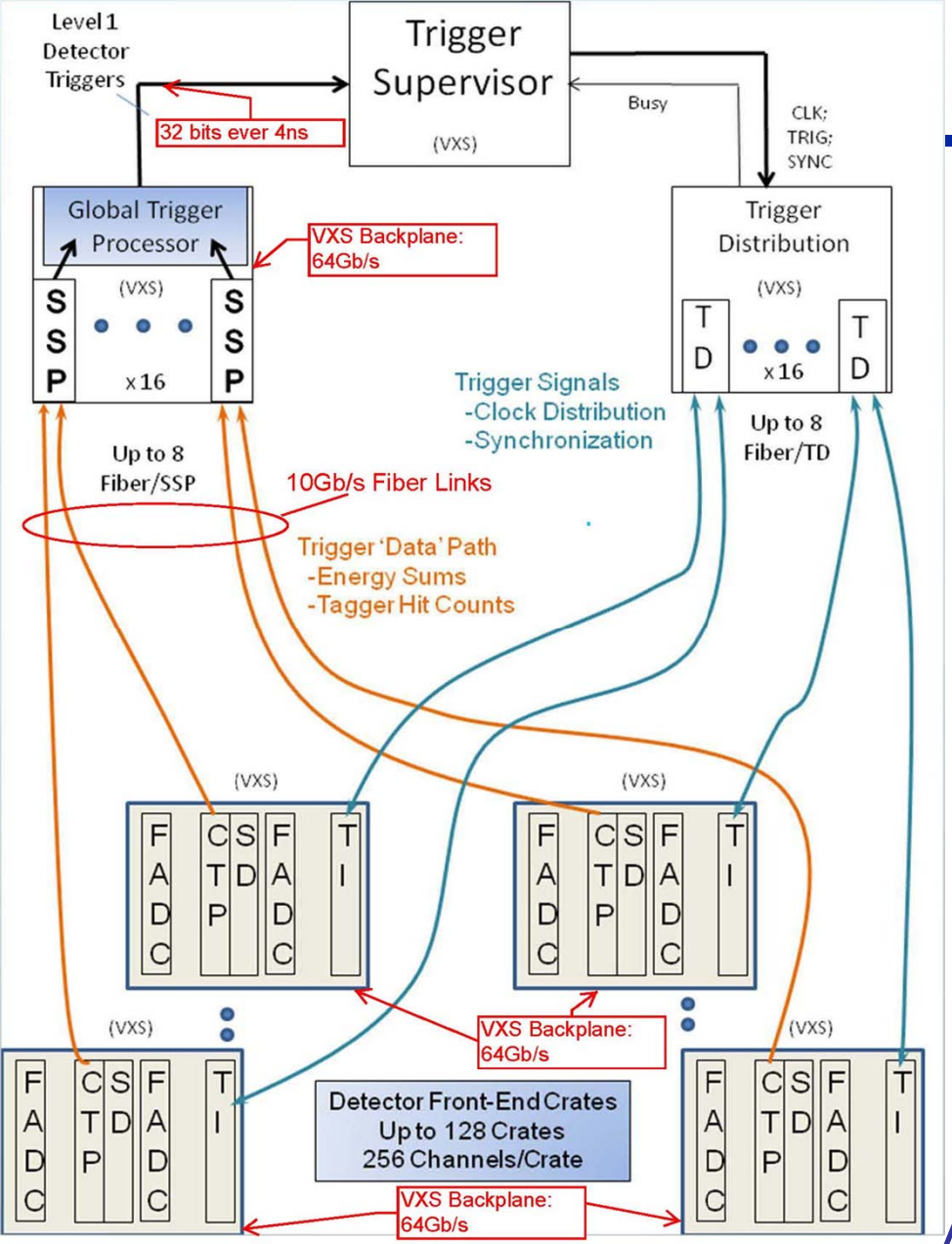
VXS "Switch" Card
Crate Trigger
Processor

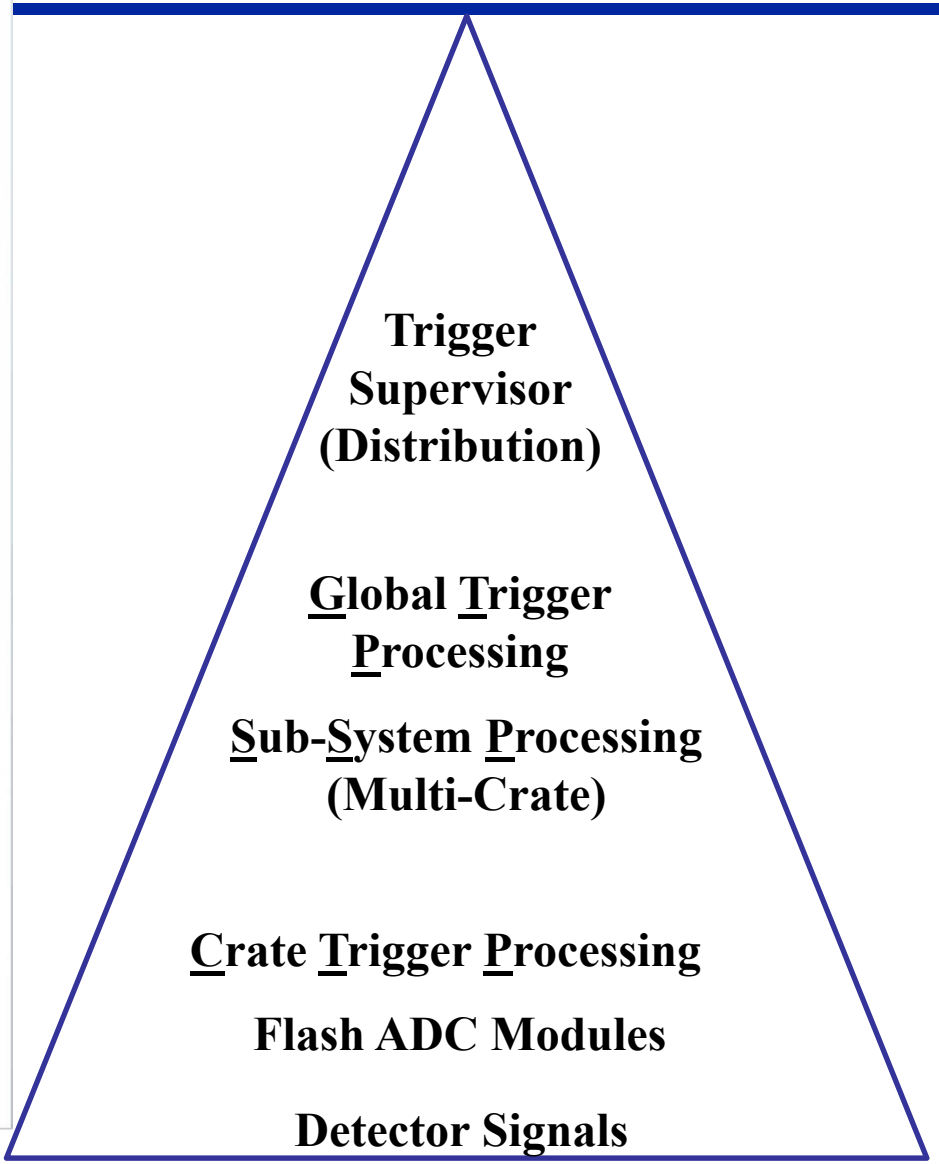
8Gb/s
Fiber

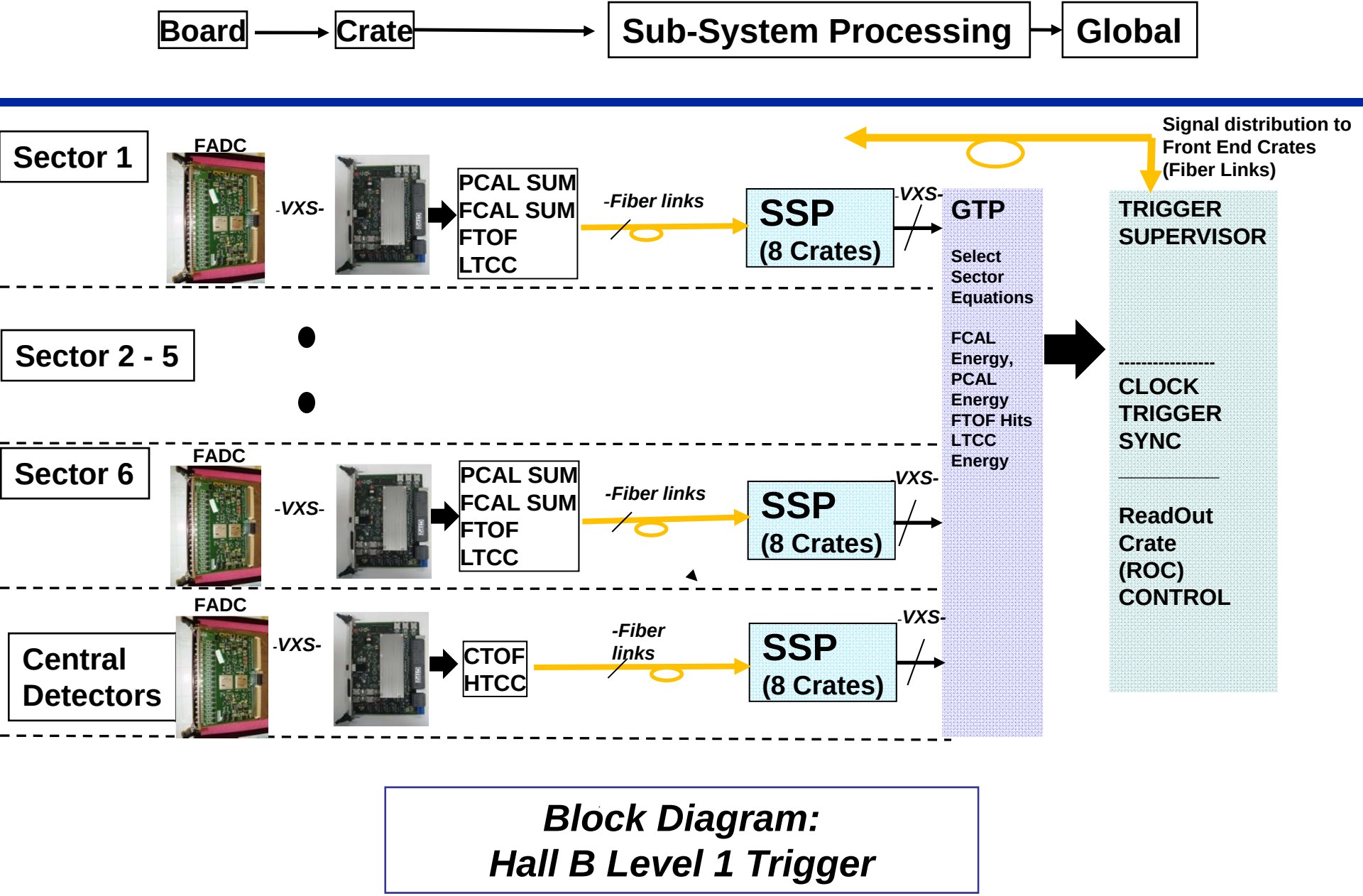
Crate Sum to Trigger

System Topology
&
Circuit Boards

System Block Diagram







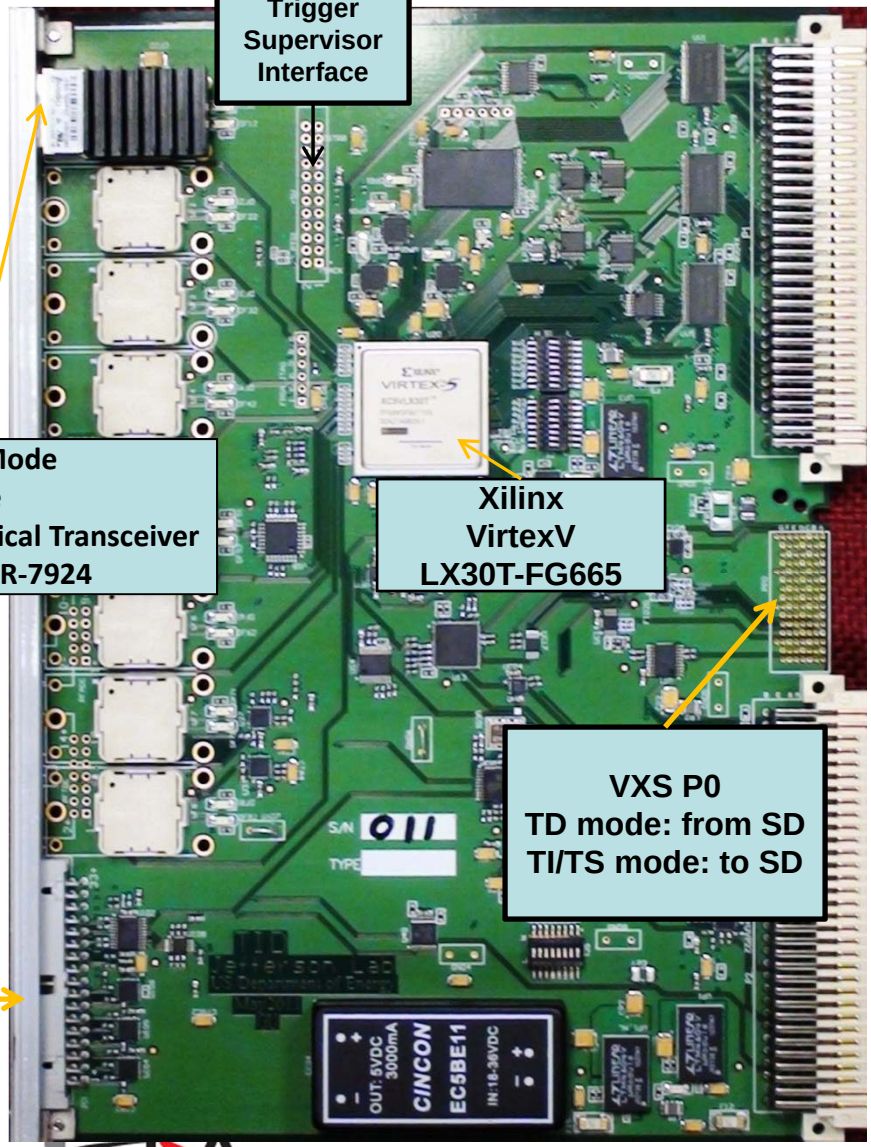
Block Diagram:
Hall B Level 1 Trigger

Flash ADC 250MHz

- 16 Channel, 12-bit
  - 4ns continuous sampling
  - Input Ranges: 0.5V, 1.0V, 2.0V (user selectable via jumpers)
  - Bipolar input, Full Offset Adj.
  - Intrinsic resolution – σ = 1.15 LSB.
  - 2eSST VME64x readout
  - Several modes for readout data format
    - Raw data
    - Pulse sum mode (Charge)
    - TDC algorithm for timing on LE
  - Multi-Gigabit serial data transport of trigger information through VXS fabric
  - On board trigger features
    - Channel summing
    - Channel coincidence, Hit counters
  - 2 Pre-production units extensively tested
  - Automatic Test Station is complete
  - Engineering Run – 40 Delivered!
    - 18 Hall D
    - 17 Hall B
    - 685 Boards for all Halls
  - Production Procurement FY12 (>$2M).

Trigger Hardware Status - TI

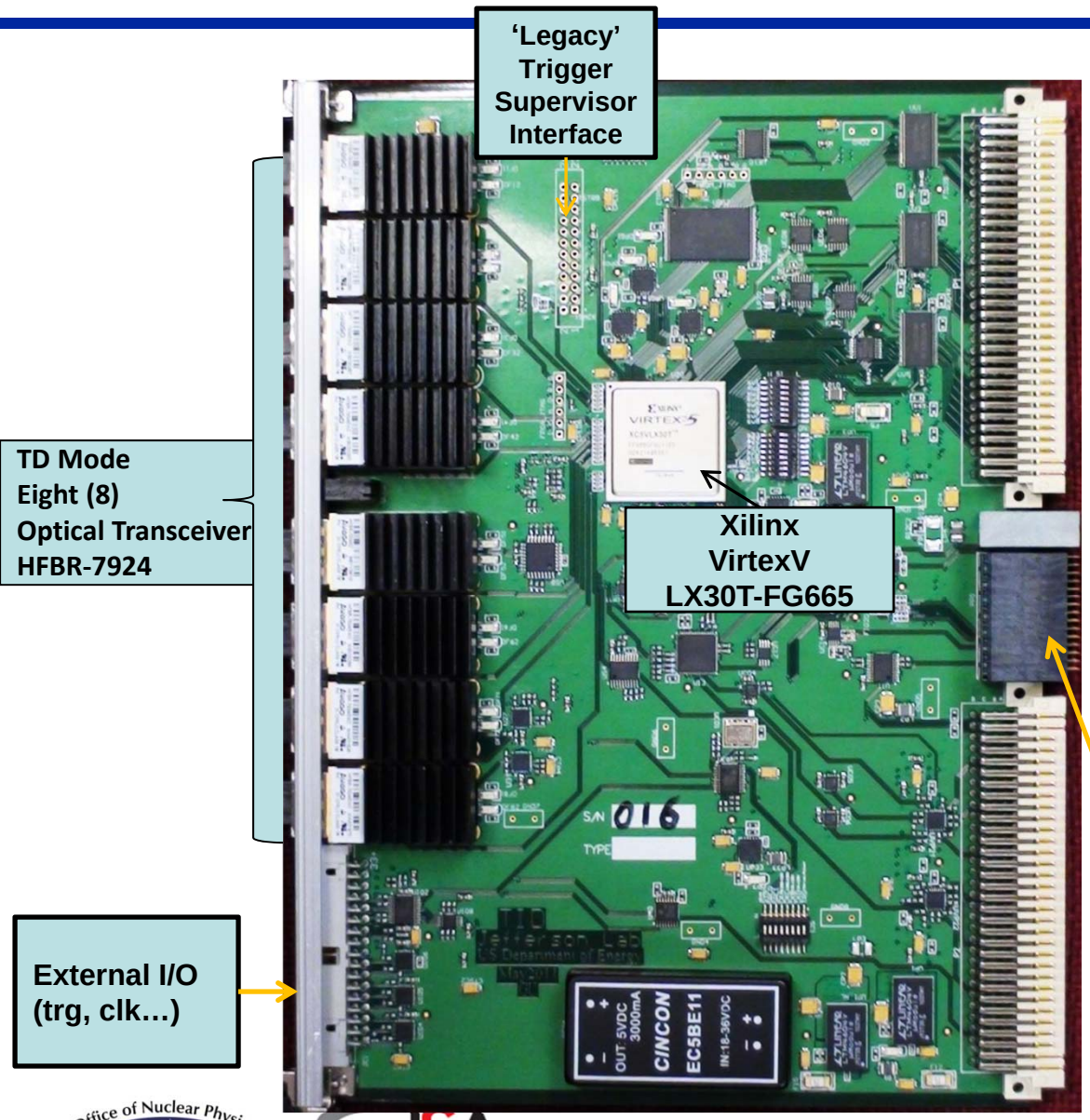
W. Gu
DAQ Group
23-Sept-2011



- Direct link to Trigger Supervisor crate via parallel fiber optic cable
- Receives precision clock, triggers and sync from TD
- Connects directly to SD on VXS backplane
- Board design supports both TI and TD functions, plus can supervise up to eight front end crates.
- Manages crate triggers and ReadOut Controller events

Trigger Hardware Status - TD

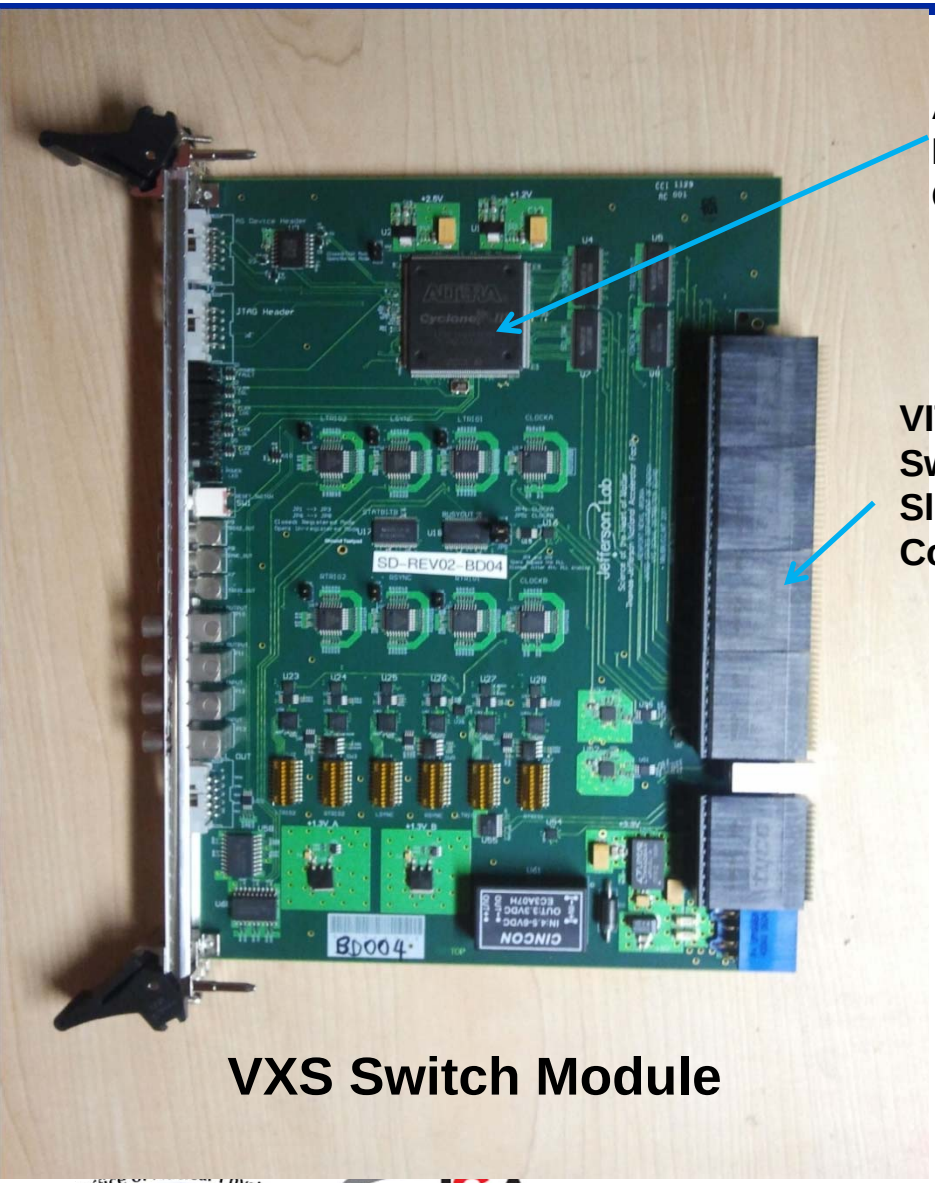
W. Gu
DAQ Group
23-Sept-2011



- Distributes from Trigger Supervisor crate to front end crates (TI)
- Distributes precision clock, triggers, and sync to crate TI modules
- Board design supports both TI and TD functions, plus can supervise up to eight front end crates.
- Manages crate triggers and ReadOut Controller events

Crate Level – Signal Distribution (SD)

N. Nganga
23-Sept-2011

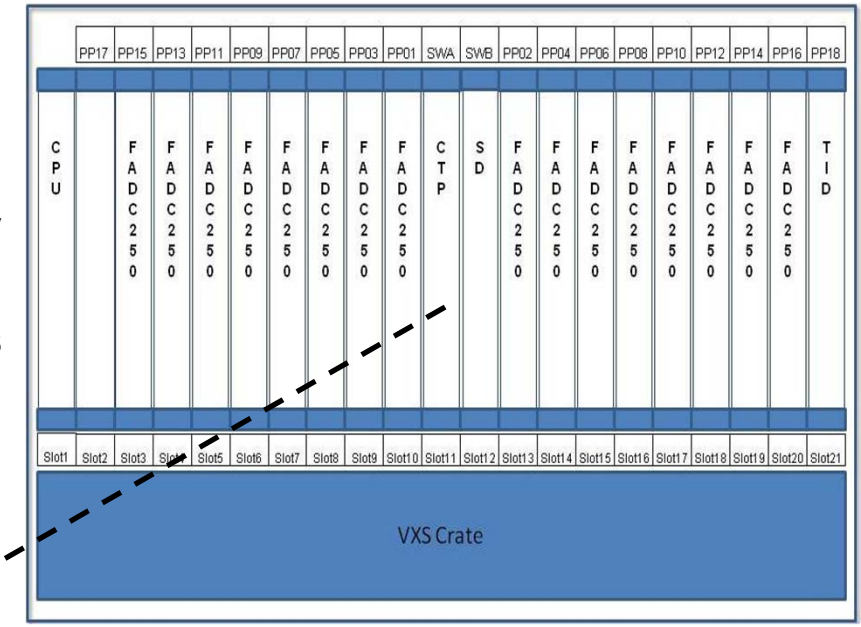


VXS Switch Module

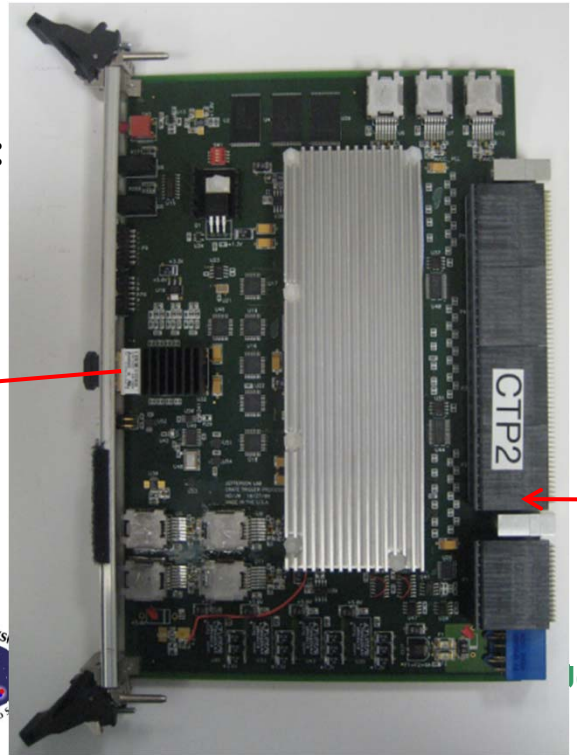
- The effect of Jitter attenuation has been tested and found to be most effective when clock signal jitter is >5ps and(or) when the input signal is >100MHz.
- SD boards have been used in the two-crate tests since the beginning of Summer 2011 without glitches.
- PCB manufacture and Board assembly was ~$1000 per board
- SD components are estimated at $1200 per board (price break dependent).

Crate Trigger Processor

- 4 Fully assembled are tested and in the lab!!
- 2 newest units include VirtexV FX70T that supports higher serial speeds. (5Gbps) Matches FX70T on FADC250
- Crate Trigger Processor computes a crate-level energy sum (or hit pattern)
- Computed crate-level value sent via 8Gbps fiber optics to Global Trigger Crate (32bits every 4ns)



CTP Prototype:



MTP Parallel Optics

8Gb/s to SSP

VXS Connectors Collect serial data from 16 FADC-250

- Significant verification testing will be performed with 2 crate DAq station.
- Hall D requires 23 units
- Hall B requires 21 units

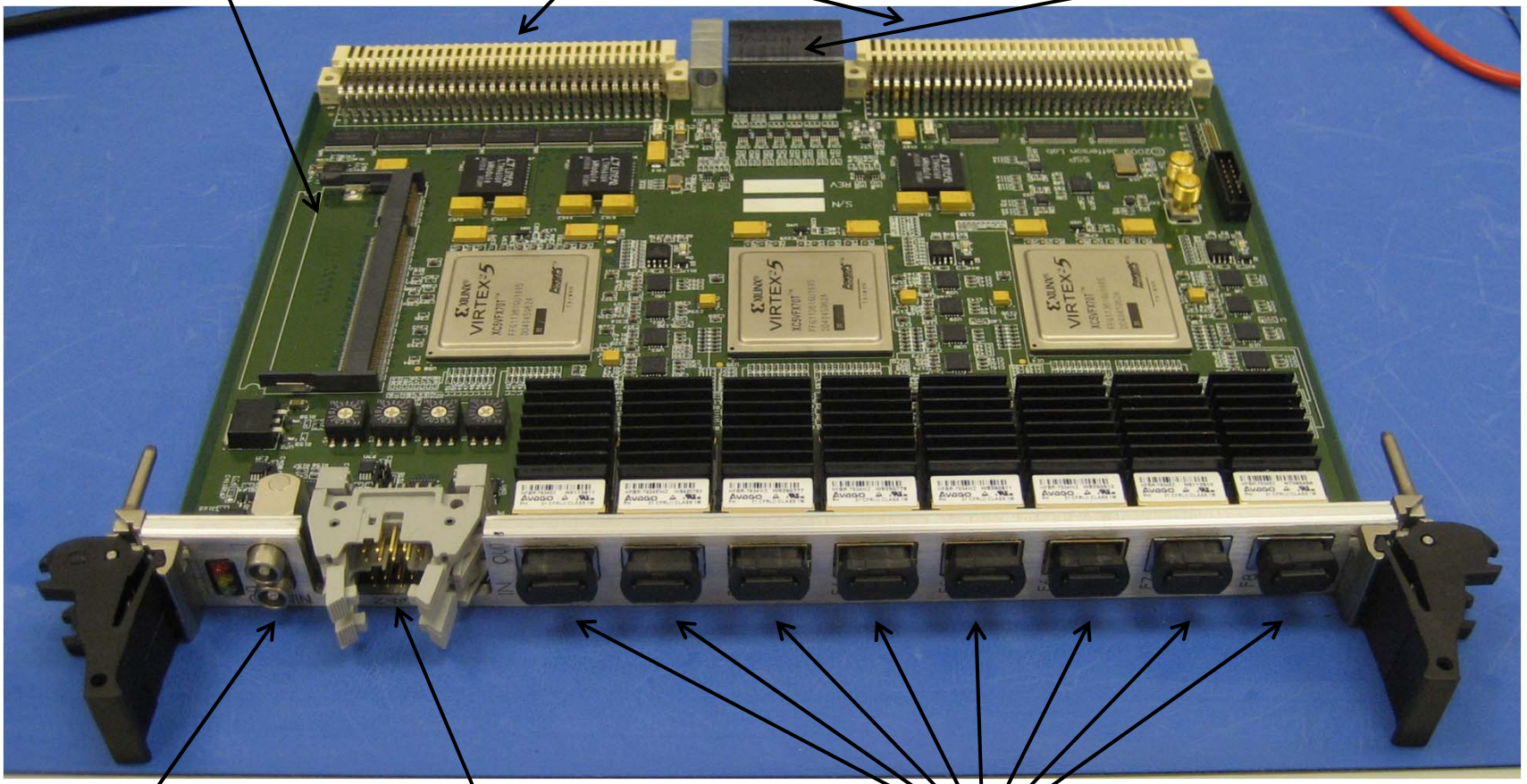
SSP Prototype

Ben Raydo
9-Sept-2010

Optional DDR2 Memory Module (up to 4GByte)

VME64x (2eSST support)

VXS-P0 (up to 16Gbps to each GTP)



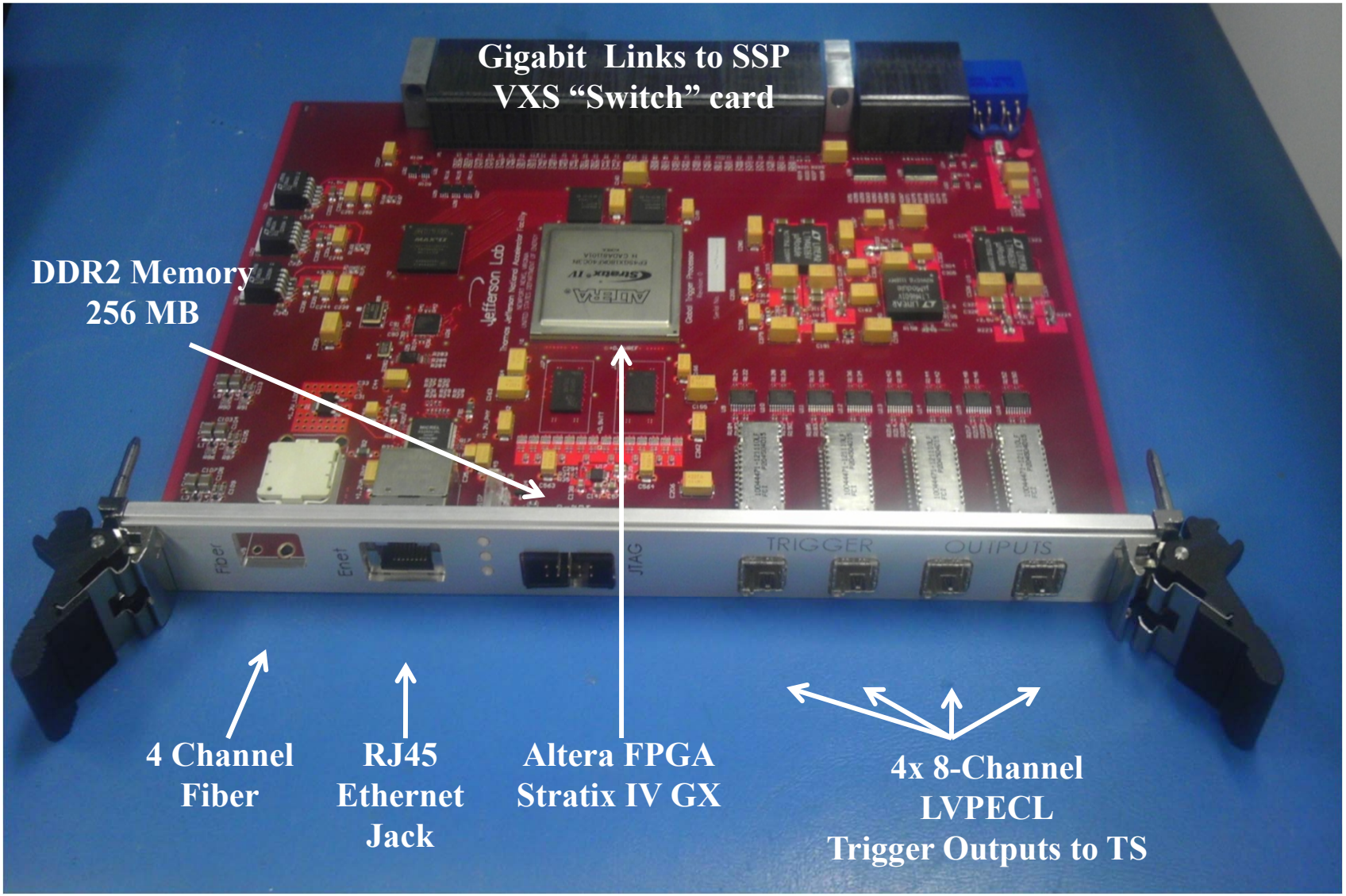
2x NIM (bidirectional)

4x ECL/PECL/LVDS In
4x LVDS Out

8x Fiber Ports (10Gbps each to CTP)

GLOBAL TRIGGER PROCESSOR
1st Article Board

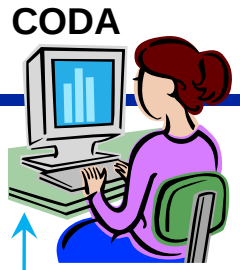
S. Kaneta
2011



High Speed Circuit Board and Firmware Designers Paradise, But

- FPGA Selection is critical
  - -Gigabit Transceiver design/test effort is significant for VXS
  - -MUST invest in firmware development/verification tools
  - -MUST invest in test equipment for jitter analysis, VXS extension boards, prototype test circuits
  - -Consider investment for circuit board routing tools and post routing simulation tools
- MUST prohibit (tightly control?) design scope “creep”
- Significant firmware development time/verification effort
- MUST consider technology ‘upgrade’ before production
  - e.g. Virtex-5 or Virtex-7

- Parallel Fiber Optic cables (MTP connectors, OM3 rating)
- Backplane vendor selection and ‘crate’ power supply requirements
- Thermal analysis
- Long term maintenance and repair issues

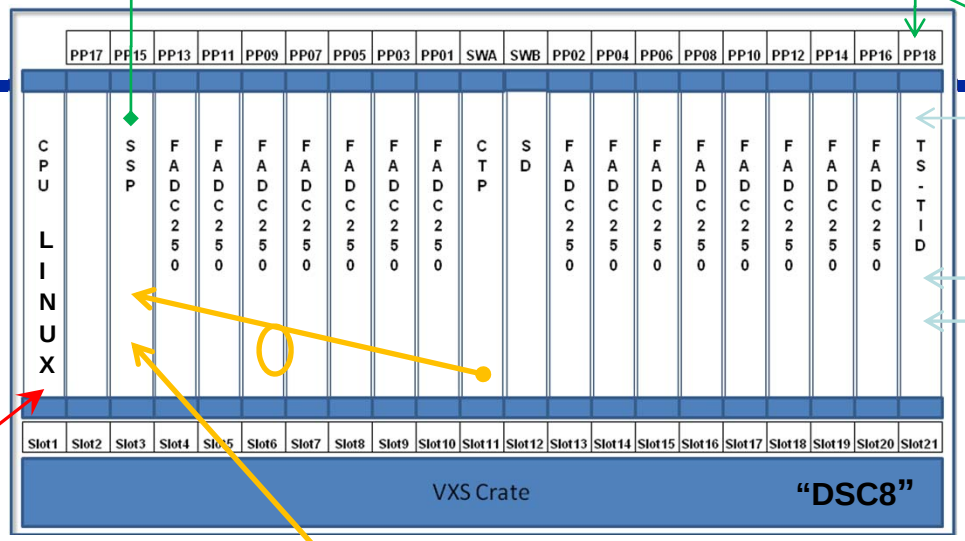


Dell 2GHz Xeon
Dual core 1U

Network Switch

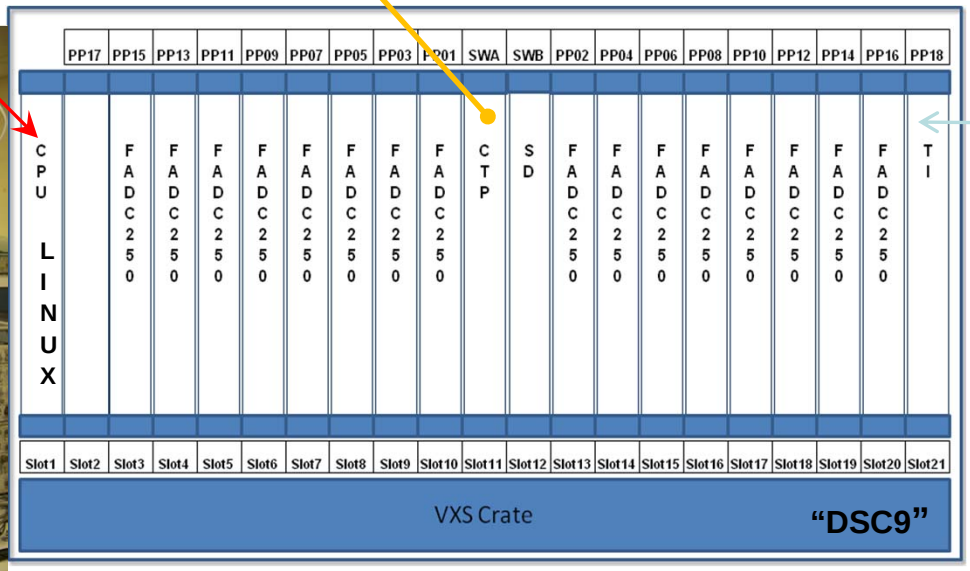
Ethernet

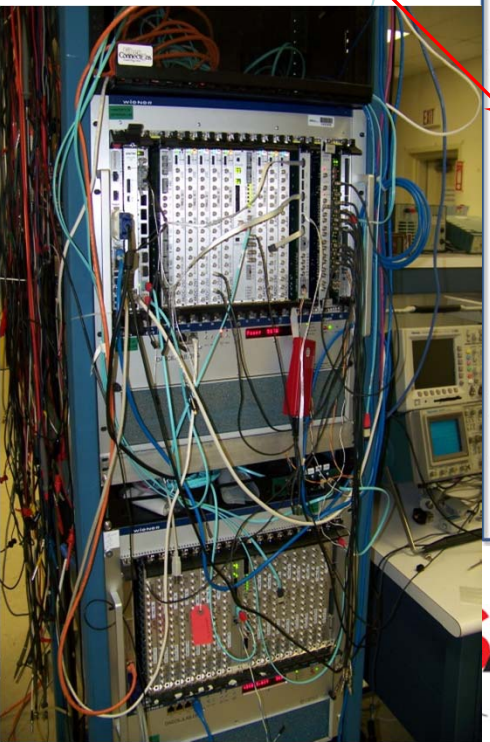
Two crate Trigger Signal
From SSP to TI(TS)



150m fiber
through MTP
patch panel

50m fiber
through MTP
patch panel

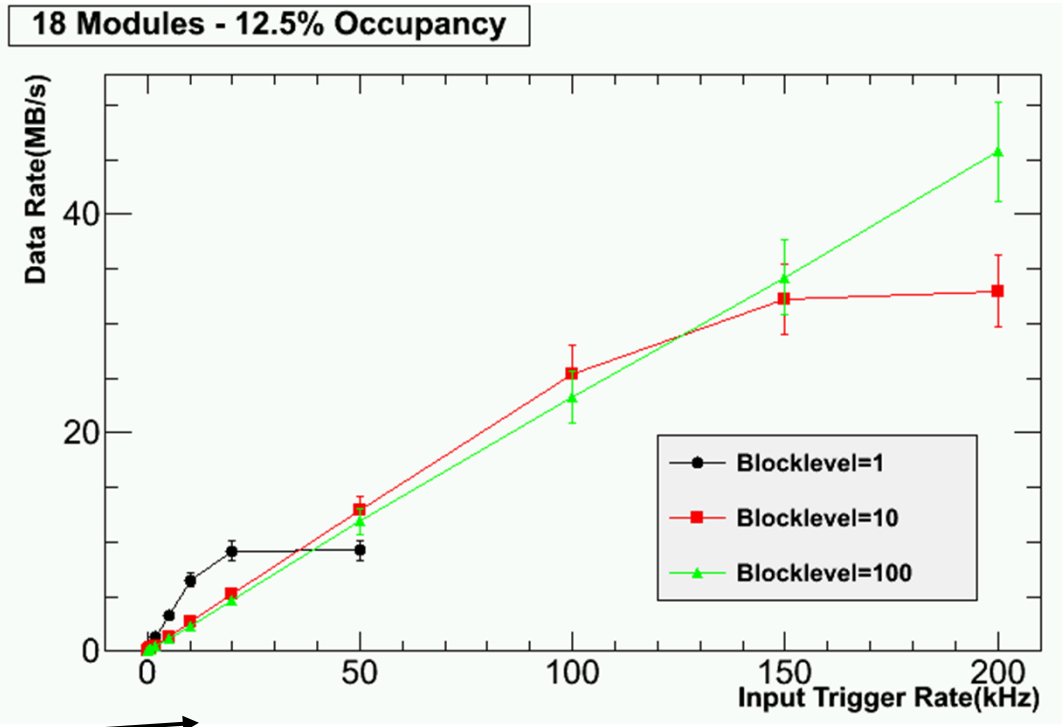




Two DAq Crate Testing: FY11

Two DAQ Crate Testing: FY11

- Pre-Production and 1st article boards have been delivered
- Significant effort for circuit board fabrication, assembly and acceptance testing
- System testing includes:
  - Gigabit serial data alignment
    - ✓ 4Gb/s from each slot
    - ✓ 64Gb/s to switch slot
    - ✓ Crate sum to Global crate @8Gb/s
  - Low jitter clock, synchronization
    - ✓ ~1.5ps clock jitter at crate level
    - ✓ 4ns Synchronization
  - Trigger rate testing
  - Readout Data rate testing
  - Bit-Error-Rate testing
    - -Need long term test (24/48 hrs)
  - Overall Trigger Signal Latency
    - ✓ ~2.3us (Without GTP and TS)



200KHz Trigger Rate!

Summary

- VXS solution for 12GeV DAq and Trigger Electronics has been proven
- VXS offers an elegant high speed link from each payload slot
  - We use these Gigabit serial links for L1 Trigger Decisions
  - We use the 2nd switch slot for low skew deterministic signal distribution
- Industry FPGA sources provide technology for multi-gigabit transceivers
  - Perfect match for VXS signaling
  - FPGA devices offer significant capabilities for trigger algorithms and readout data reduction
- Be Advised: Design challenges demand significant costs for:
  - Engineering labor; Computer Aided Engineering/Drafting (CAE/CAD tools)
  - FPGA firmware development/verification tools
  - Test equipment
  - Prototype fabrication and assembly: >1000 pin count BGA, etc
- Two full crate DAq testing has been successful and has been an excellent development foundation for software drivers, and commissioning diagnostic tools.

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