The FAIR Timing Master: A Discussion of Performance Requirements and Architectures for a High-precision Timing System

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Overview

1. What FAIR needs
2. Gathering Requirements
3. Choosing a Processor Core
4. Machine & Interlock Handlers
5. Conclusion
6. Q & A

FAIRy Tales: Once upon a timing master...

- What FAIR needs

What FAIR needs

The FAIR Timing Master

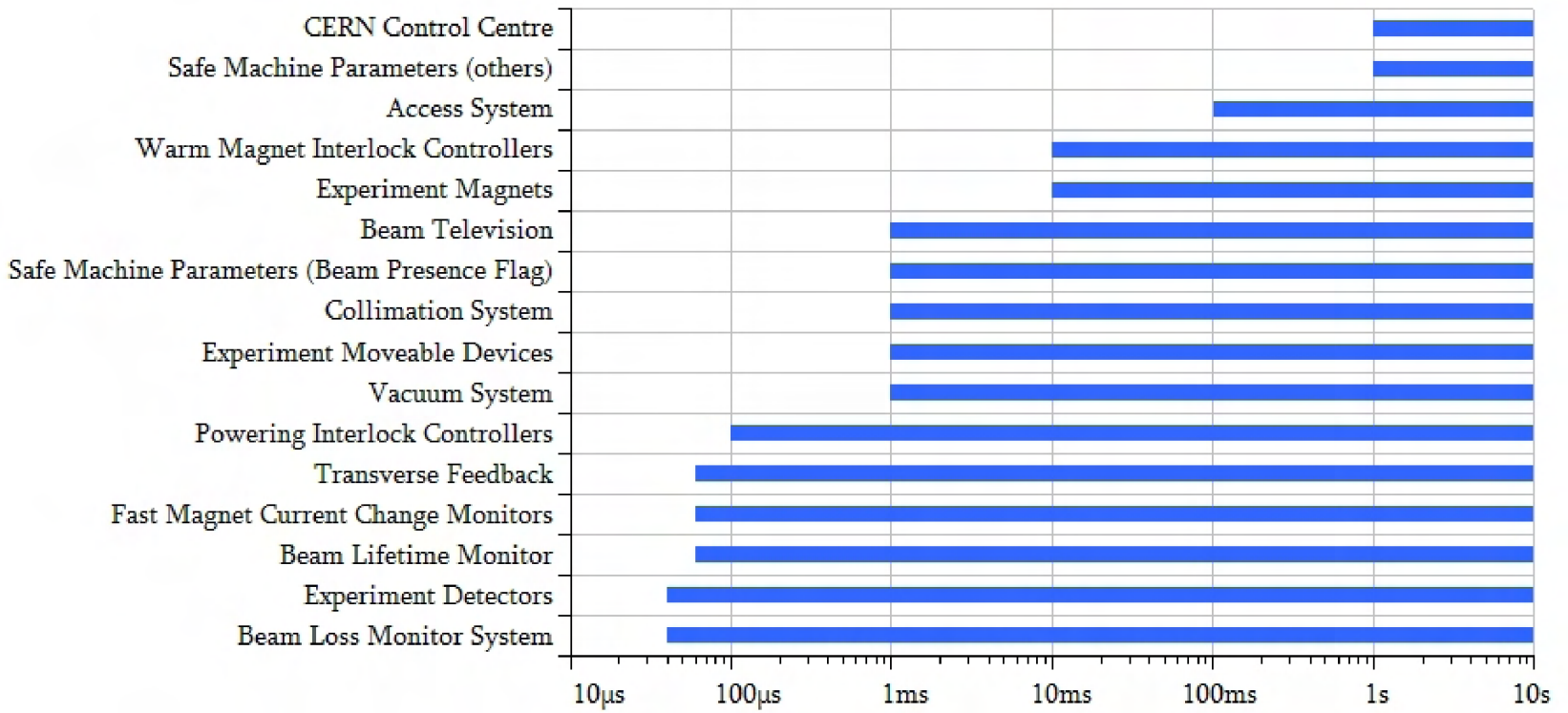
- 2000+ Timing Nodes
- Control Messages
- Absolute Time Synchronisation
- Determinism
- Fast Interlock Handling

Take your time

- Gathering Requirements

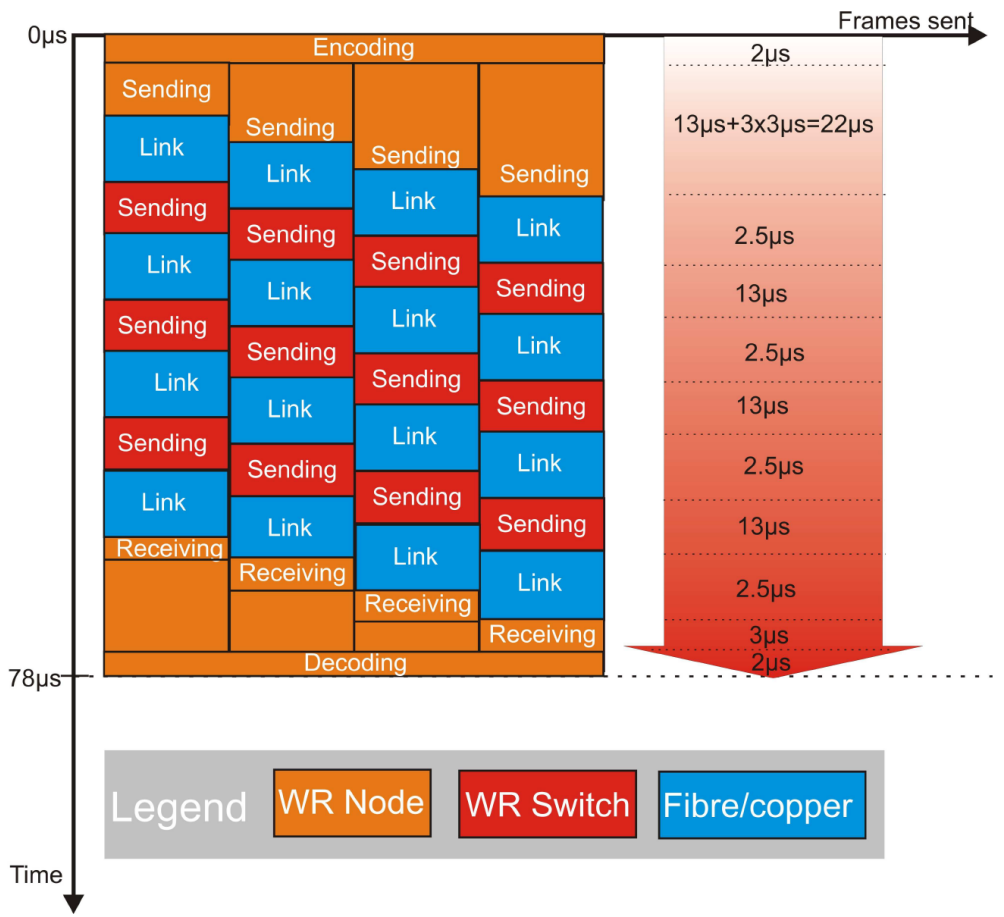
Gathering Requirements

CERN: Response Times of Machine Protection Systems



Gathering Requirements

WhiteRabbit Command Message Delay (cut-through)



Where did you get that brain?

- Choosing a Processor Core

Choosing a Processor Core

High End Multicore CPU

- 3+ GHz
- No RTOS for multicore
- Suffers from IO bottleneck
- ISR in ms range

Choosing a Processor Core

MCU RTOS Latency Comparison (µs)

	Interrupt Latency		Context Switching	
	max	**avg ±**	**max**	**avg ±**
Idle System				
RTL	13.5	(1.7 ± 0.2)	33.1	(8.7 ± 0.5)
RTEMS1	14.9	(1.3 ± 0.1)	16.9	(2.3 ± 0.1)
RTEMS	15.1	(1.3 ± 0.1)	16.4	(2.2 ± 0.1)
vxWorks	13.1	(2.0 ± 0.2)	19.0	(3.1 ± 0.3)
Loaded System				
RTL	196.8	(2.1 ± 3.3)	193.9	(11.2 ± 4.5)
RTEMS1	19.2	(2.4 ± 1.7)	213.0	(10.4 ± 12.7)
RTEMS	20.5	(2.9 ± 1.8)	51.3	(3.7 ± 2.0)
vxWorks	25.2	(2.9 ± 1.5)	38.8	(9.5 ± 3.2)

Choosing a Processor Core

SoftCPU LM32

- 32 Bit RISC
- 150 MHz
- ISR /
- IO latency < 50 ns
- extendable

Talk to my agent

- Machine & Interlock Handlers

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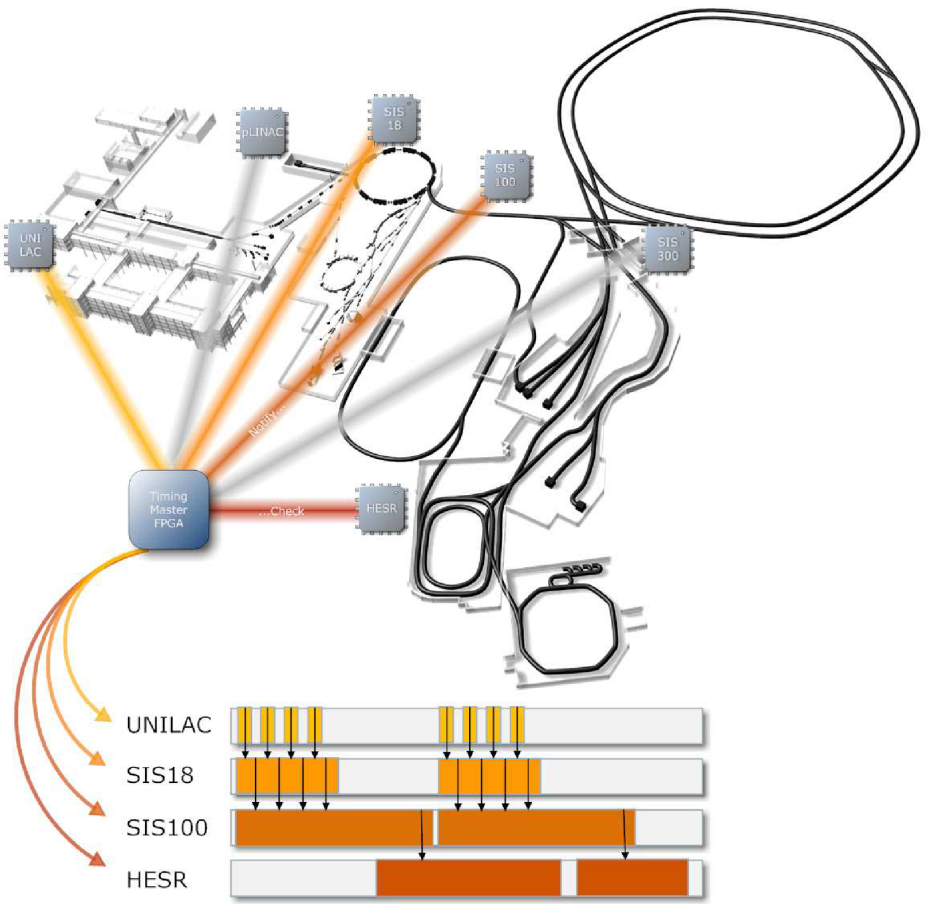
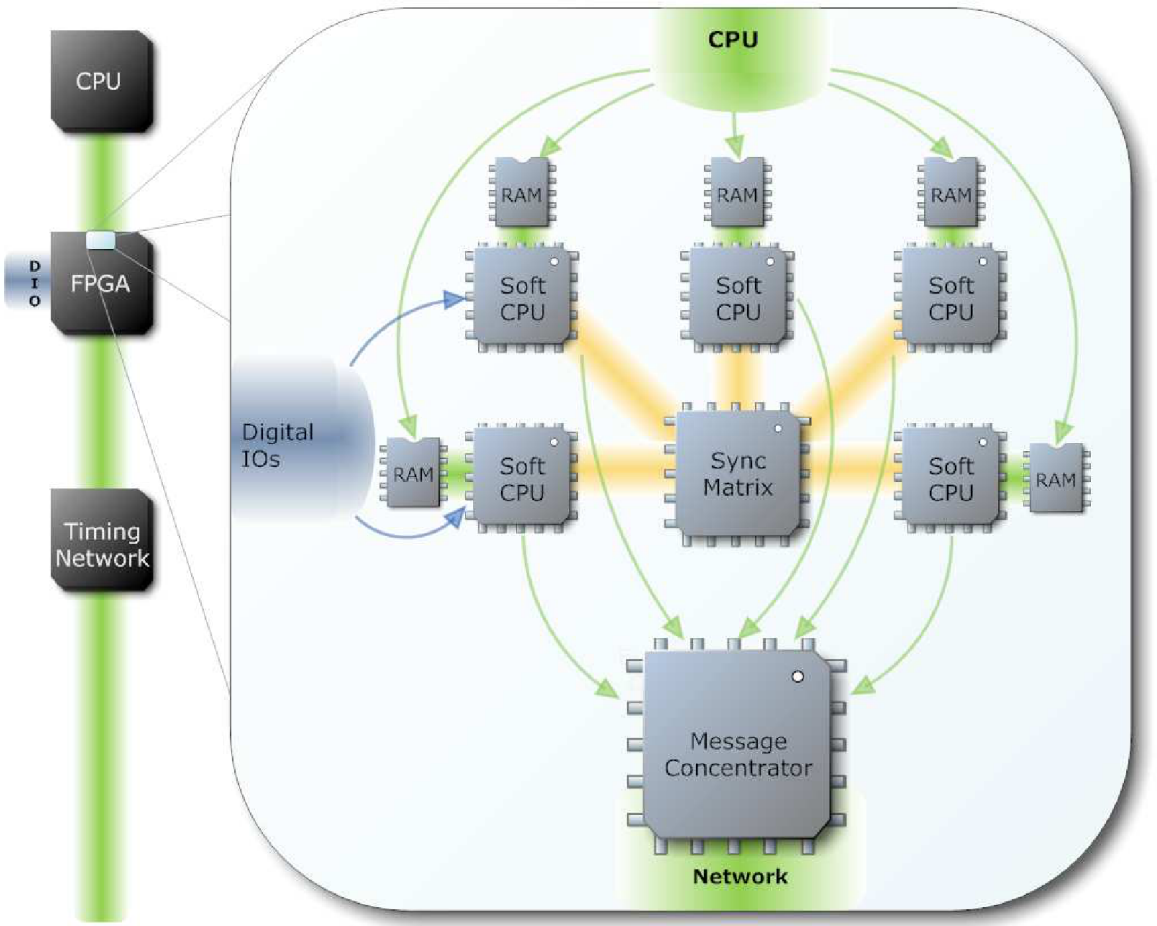
Machine & Interlock Handlers

Sequences in FAIR Production Chains



Machine & Interlock Handlers

MultiCore SoftCPU

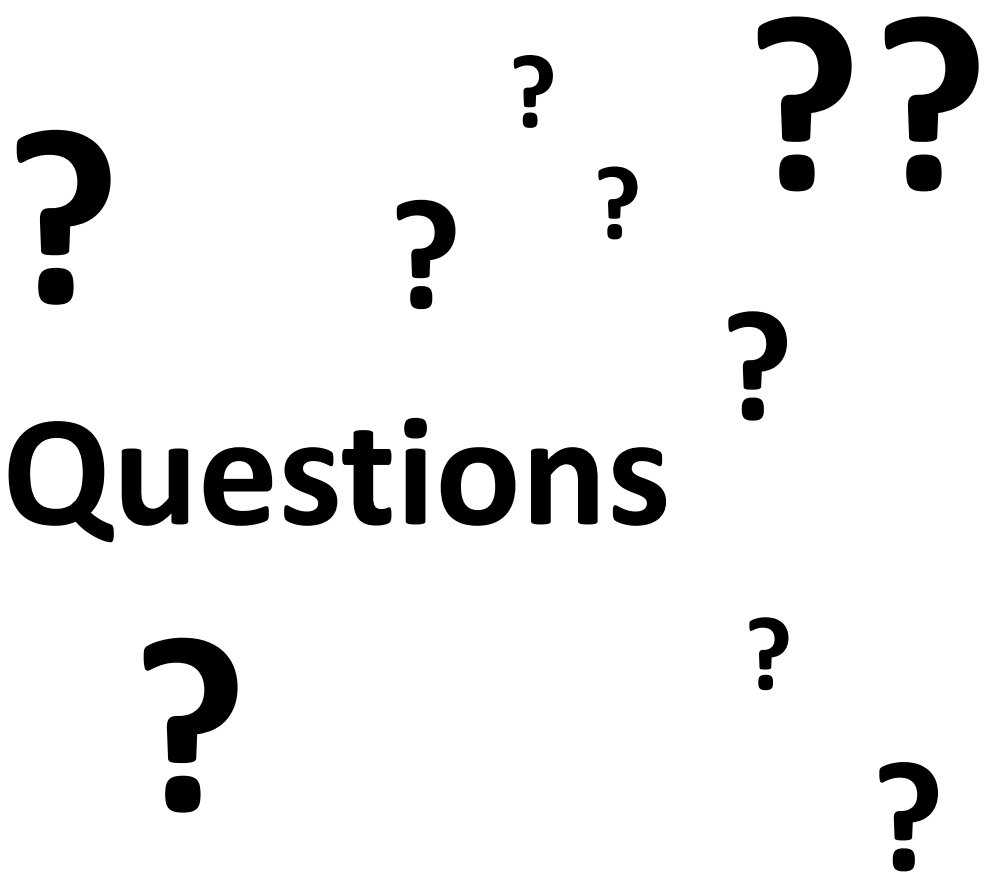


Conclusion

The architecture should have...

- Multicore SoftCPU
- Own DPRAM block per SoftCPU
- Custom Instructions for fast Sync & IO
- Sync / Message matrix
- Message Concentrator to WhiteRabbit
- On the fly parameter & firmware change

Questions and Answers



Thank you

For your time and attention

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