FIRST OPERATIONAL EXPERIENCE WITH THE LHC BEAM DUMP TRIGGER SYNCHRONISATION UNIT

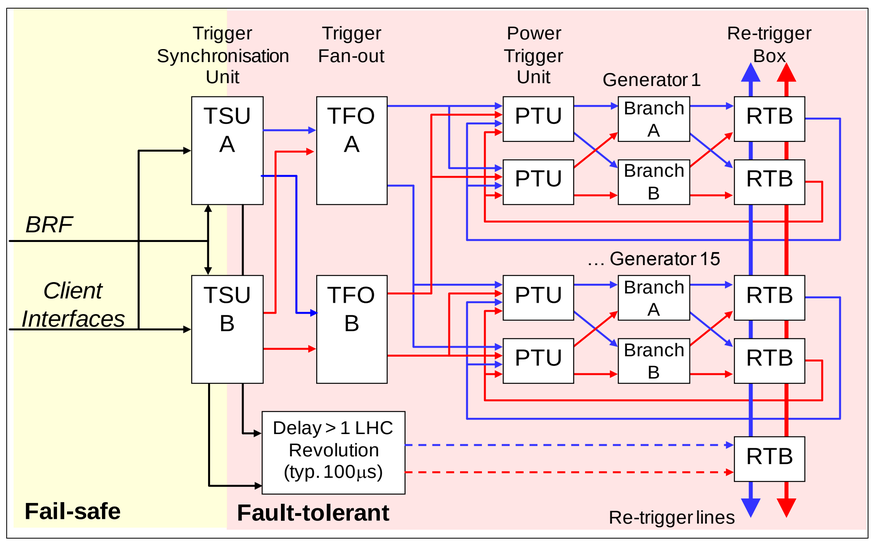
A. Antoine, C. Boucly, N. Magnin, P. Juteau, N. Voumard,
CERN, Geneva, Switzerland

icalepcs 2011

Abstract

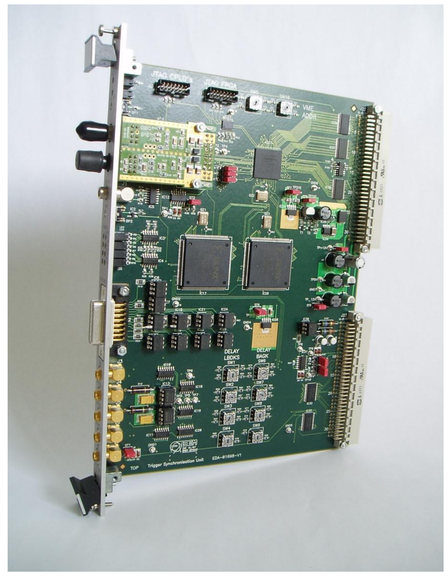
Two LHC Beam Dumping Systems (LBDS) remove the counter-rotating beams safely from the collider. Dump requests can come from 3 different sources: the machine protection system, the machine timing system or the LBDS itself. These dump requests are synchronized with the 3 µs beam abort gap in a fail-safe redundant Trigger Synchronization Unit (TSU) based on a Digital Phase Locked Loop (DPLL), locked onto the LHC beam revolution frequency with a maximum phase error of 40 ns. The TSU synchronized trigger pulses outputs are then distributed to the high voltage generators of the beam dump kickers through a redundant fault-tolerant trigger distribution system. This paper describes the outcome of the external review and the new tools designed to increase diagnosis and monitoring functionalities, and, a more automated validation Process of the hardware and embedded firmware. Additionally, the lessons learnt on the project life cycle for the design of mission critical electronic modules is presented.

Trigger synchronisation & distribution system (TSDS)



- LHC Beam dump triggering system entirely redundant.
- Trigger synchronisation units (TSU) used a discreet phase locked loop (DPLL) to be continuously locked on the beam revolution frequency (BRF) and produce dump trigger pulse trains synchronised with the beam abort gap.
- The firing of the beam dump is initiated when a dump request from any client is sent to the TSU.
- When a dump request is recorded, the TSUs synchronous output triggers are enabled to allow the DPLL synchronous pulse train output to fire the trigger fan out (TFO) units and to initiate the beam dump trigger chain.

TSU



Trigger synchronisation units review

•Requirements review

A high level hierarchy that identifies all hardware and software modules with their corresponding functionalities has been created and cross-checked through a ***validation matrix*** with the list of all functional requirements

- All requirements are taken into acount
- All requirements are covered by at least one sub-module
- Links between modules are coherent
- Hardware architecture is correct
- Architecture sometime too complex for the required functionalities

•Design review

A low level hierarchy has been created and a ***requirement coverage matrix*** issued to synthesize the results with a basic OK/NOK status result for every requirement associated with a criticality level

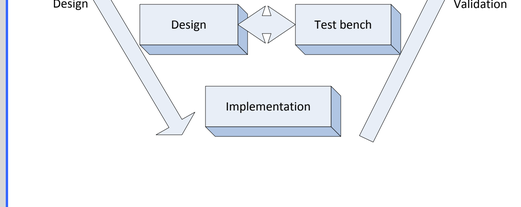
- 11 requirements out of 200 identified as not properly implemented
- Certain internal failures generate async. trigger on only one TSU
- Possibility to generate dump triggers during arming sequences
- Dump trigger can occur at power-on due to undefined flip-flop state
- state machine is under uncontrolled conditions in LOCAL mode

•Hardware and software review

An ***in-depth analysis*** of the TSU electronic circuit has been completely checked with respect to modern state-of-the-art hardware design techniques and its embedded VHDL software have been fully simulated and their reactions to incorrect operational conditions analysed in detail

- Great performance under normal/internal failure conditions
- VHDL simulations passed
- No protection of powering circuits against internal failure
- Under-sized or inappropriate type of capacitors
- Missing protection on board interfaces
- Homogenization of circuit family and circuit types

V-Cycle



- Project separates in two teams with the ***same goal*** but ***a different function***:
  - To design the final product (Left)
  - To design the test bench (Right)
- Minimize design common mode errors
- Improve reliability and robustness of the final products

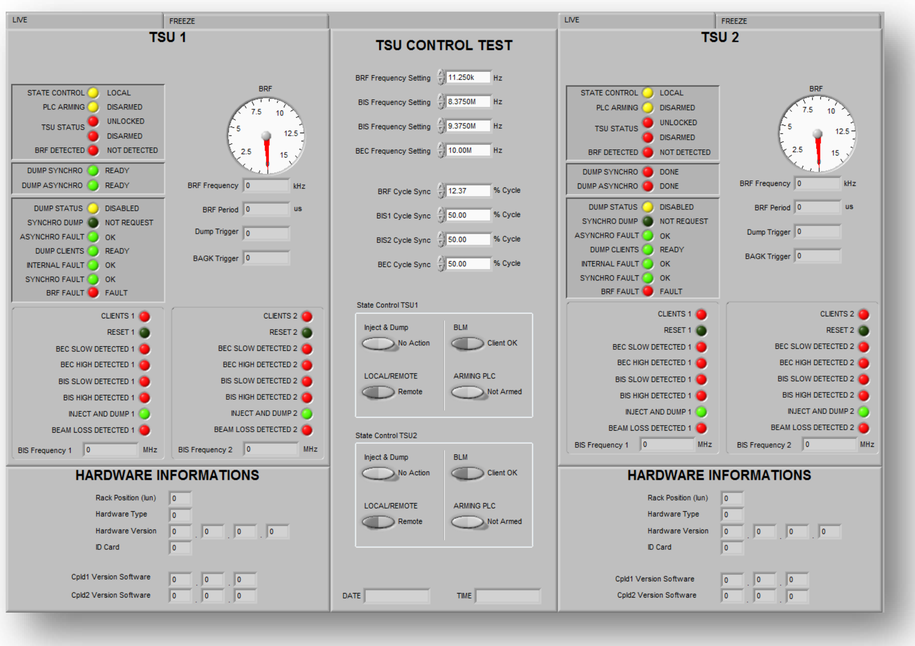
New tools

TSU automated test bench

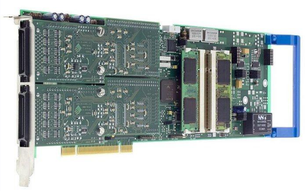
TSU hardware and embedded software functionalities validation before operational deployment (Base on NI-PXI 8184 embedded controller running LabVIEW Real-Time)

Emulation of all input signals

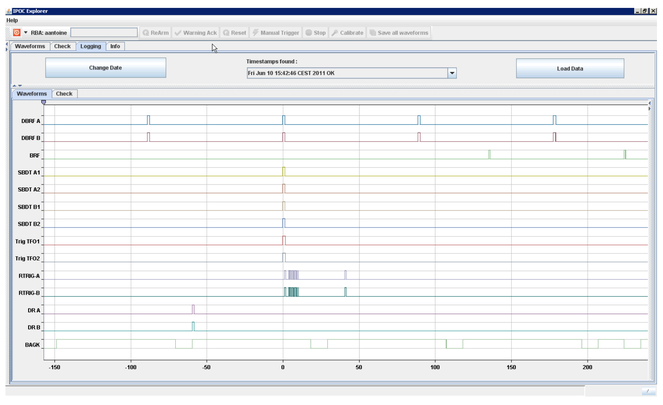
Analysis of output signal



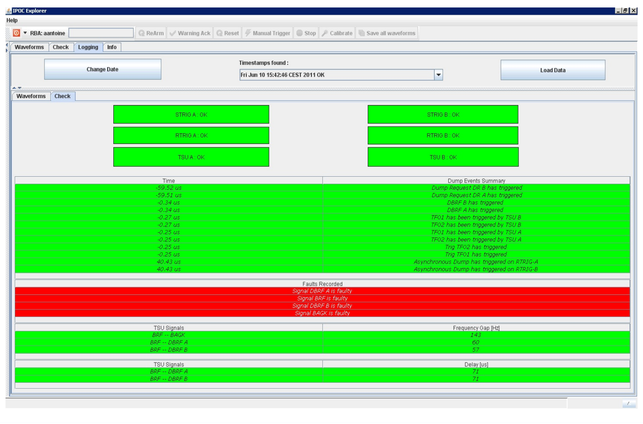
TSU IPOC (TSU internal post operational check)



Based on a PCI 32 bit 125 MS/s digital I/O module from SPECTRUM with acquisition software running on a LINUX front-end



Monitoring function developed to get a better understanding of the entire LBDS triggering process



Logic analyser function to perform after each dump a check of the correct sequence of triggering and re-triggering pulses, the correct delays between the different signals, the sanity of the signals, the correct frequency and phase offset between distributed and internally generated re-phased beam revolution frequency

Summary

The first operational experience and the external review led to the creation of three new functions. An automated test bench, a TSU IPOC monitoring function with an on-line graphical interface and a TSU IPOC logic analyser. Additionally, the external review has given us a new methodology in project design improving the reliability of final products, the V cycle. The last release of the TSU units, taking into account all critical and major design errors highlighted by the external review, is now ready for deployment after a successful completion of the automated test process. A new hardware design release will be started in 2012 to improve the robustness of the interfaces.