The LHC Safe Machine Parameter Controller Test Bench

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Abstract

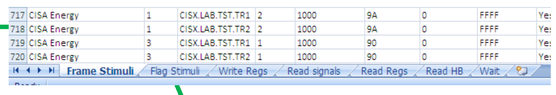
This paper outlines the core concepts and realisations of the Safe Machine Parameters Controller (SMPC) test-bench, based on a VME crate and LabVIEW program. Its main goal is to ensure the correct function of the SMPC for the protection of the CERN accelerator complex. To achieve this, the tester has been built to replicate the machine environment and operation, in order to ensure that the chassis under test is completely exercised. The complexity of the task increases with the number of input combinations. This paper also outlines the benefits and weaknesses of developing a test suite independently of the hardware being tested, using the "V" approach.

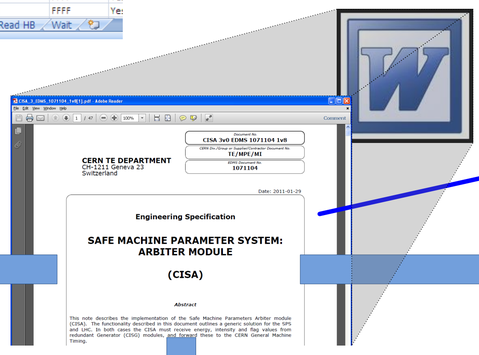
The diagram below shows how the "V" approach is used for the SMPC testbench

The test bench software has been built to facilitate the addition, modification or suppression of tests. The tests are not defined in the program itself but in an **Excel file** from the specification.

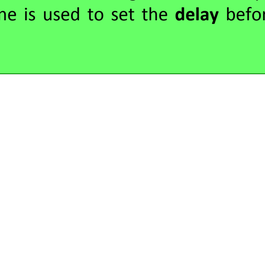
This file contains each possible elementary test divided in steps. A step is defined as a set of actions which are realised at the same time. **Eight actions** (all optional) are defined, each one in a separate worksheet:

- Three **write**: for the hardware it can be frames or flags, for the software it is registers,
- Four **read**: for the hardware it can be frames or flags, and for the software registers or History Buffer records,
- One is used to set the **delay** before starting the next step.





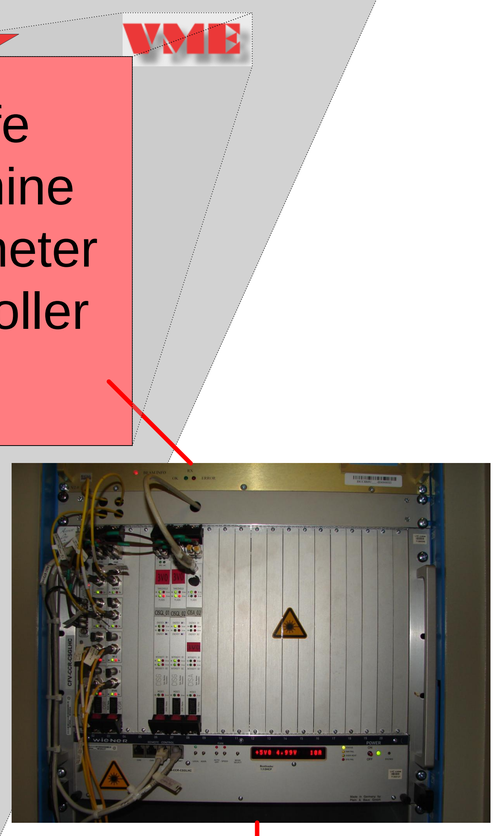
To ensure avoiding any misunderstanding, misinterpretation or hole of the specification, an effort has been carried out to generate a documentation which is out of ambiguity, using the Predicate Logic or Formal Methods (FM). FM are used to describe the behaviour of a system, independently of its nature (Hardware, software, abstract…), even if it exists several ways to write them, depending on the target where the logic is foreseen to be established. They appear like a logical language, similar to a programming language, and which allows giving an exhaustive description of how the system has to work.



Virtual **S**afe **M**achine **P**arameter **C**ontroller

Tests Database

Safe **M**achine **P**arameter **C**ontroller



The virtual SMPC is built directly from the specification (as the real SMPC).

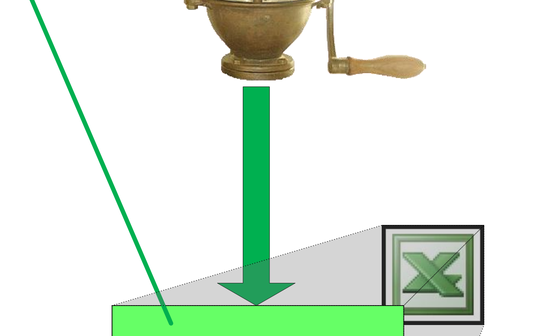
It consists of a LabVIEW subprogram which reads the test steps and transforms them into an array in which each cell is a combination of all states of all SMPC inputs for a specific time. The time granularity is 1ms, Thus a 5 seconds test generates an array of 5000 cells.

The outputs signals and the FPGA memory are simulated and calculated for each test step, and then sent to the Comparison module.

SoftWare Control

LabVIEW

LabVIEW Front Panel User Interface



HardWare Control

LabVIEW
FESA
SMPTester

The SMPC is composed of three types of electrical boards, Receivers (CISR), Generators (CISG) and an Arbiter (CISA) all based on the same basic PCB design, but having different functionality thanks to different VHDL code in FPGAs.

For the LHC, there are two redundant CISR (CISRA and CISRB), each one decoding a pair of energies and a pair of intensities. These CISR pass information to 2 redundant CISG (CISGLA and CISGLB).

The CISG use energies and intensities from the CISR, in conjunction with flags directly received from LHC beam instrumentation, and other information provided by Ethernet, to derive energy, intensity, and a set of flags and values representing the LHC machine state. Some of these flags are transmitted directly to the extraction Beam Interlock System (BIS) ensuring the safe transfer of beam between the SPS and LHC machines.

Data from both CISG is sent to the arbiter board (CISA) which assembles the redundant information and determines the overall state of the system, before transmitted to the information to client systems through the LHC General Machine Timing (GMT) .

Each board has a pair of Field Programmable Gate Arrays (FPGAs). A "control FPGA" tasked with the execution of critical operations, in which the SMP mission-critical functions are implemented. And a "monitor FPGA" which does not interfere with the critical part, but receives information from it, formats and makes it available for observation and interpretation through the Java software supervision.

In normal operation, this crate is installed in the control room in CERN Prevessin.

C&D

Comparison & Diagnostic:
All the information gathered from the SMPC is compared with the one of the virtual SMPC.
The results of the comparison code Is viewable on the LabVIEW fonrt panel image following the colour code green=ok, red=failed.

The "V" approach is based on the desire to have the SMPC entirely reproduce to specification requirements.

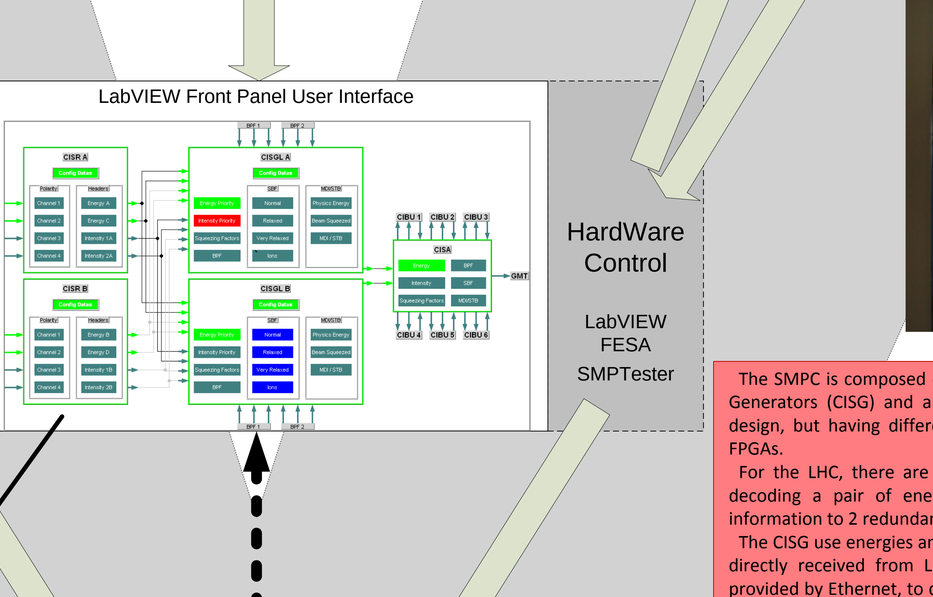
The SMPC was developed from the specification and, in parallel, a set of tests were implemented to validate the behaviour described in the specification, without taking into account how the SMPC was built. As a normal test system, the SMPT allows the validation of the behaviour of the SMPC with respect to the specification. This parallel development has the added advantage of highlighting any kind of ambiguity in the specification itself.

The SMPT is monitored by a LabVIEW program to realise the actions required by tests. The front panel of the program represents the hardware state of each SMPC board, including their connections, and their internal states. A colour-coding is used to display the state of each element:

- dark gray for elements which are not tested,
- dark blue for elements which are currently or are going to be under test,
- green for elements successfully tested
- red for elements whose test has failed.

Three users' actions are possible:

- "**Ctrl click**" on an object (rectangle, label or frame) to launch this specific test. On picture 3, the SBF label of CISGLB was clicked to obtain the blue objects,
- "**Ctrl shift click**" to launch this specific test and all dependant ones. On picture 3, this has been done on the Energy object of the CISA which has induced the test of all green objects
- "**Shift click**" to show the diagnostic of a test which has been executed, this opens a window showing a breakdown of the test steps.



CERN accelerator complex