NSLS-II booster power supplies control

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INTRODUCTION

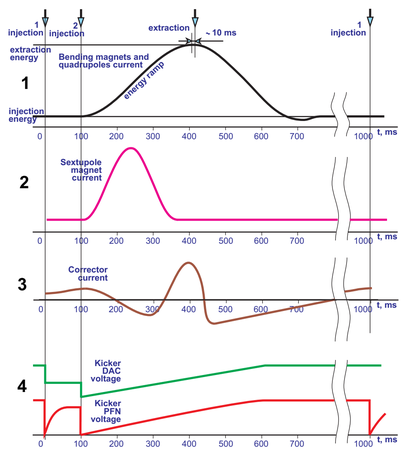
NSLS-II 3rd generation light source [1] is currently being constructed at Brookhaven National Laboratory, USA. It will be a storage ring operating at 3 GeV. To provide an effective continuous operation of the storage ring a full-energy booster [2] is proposed. The booster will accelerate electron beam from 200 MeV to the nominal energy with average beam current of 20 mA. The booster will be capable of multi-bunch and single bunch operation. Maximal number of bunches in one accelerated train is 150.

Two modes of the booster operation are planned: 1 Hz cycle with two beam injections with a 100-ms interval and 2 Hz cycle with one beam injection. The energy ramp period is 300 ms in both modes.

The required relative accuracy of the main PSs (dipoles, quadrupoles) control is 10–4 for the current plateaus (at beam injection and extraction) and 10–3 for the ramp.

Power supply control should be synchronous with other accelerator subsystems to perform its functions. The synchronization is done through timing system [3]. The PS control equipment receives a trigger pulse from the timing system and uses 10 kHz signal from Event Receivers, which is synchronous to the main RF oscillator. This synchro signal allows providing the required relative accuracy of PSs at the ramp.

OPERATION OF BOOSTER POWER SUPPLIES



Typical current diagrams for different PSs at 1 Hz cycle.

Change of bending magnet current in accordance with change of the beam energy. Depth on the plot in the region of 700 msec represents closure of magnetic loop for the dipole magnets.

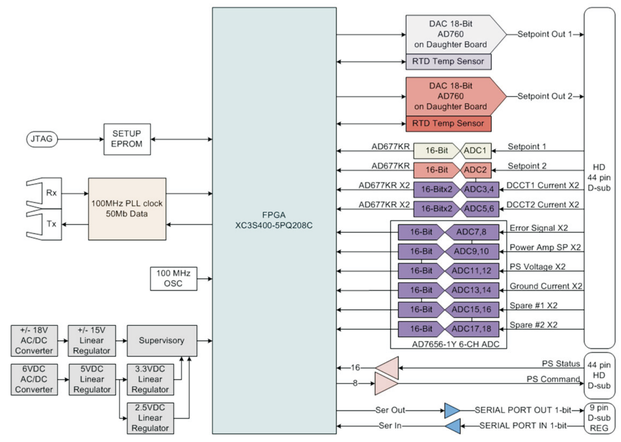
Sextupole current compensating chromaticity deviation due to eddy current and magnet saturation effects.

Bipolar change of corrector current. The corrector ramp function should be changed in real time at each booster cycle to provide an effective beam orbit correction.

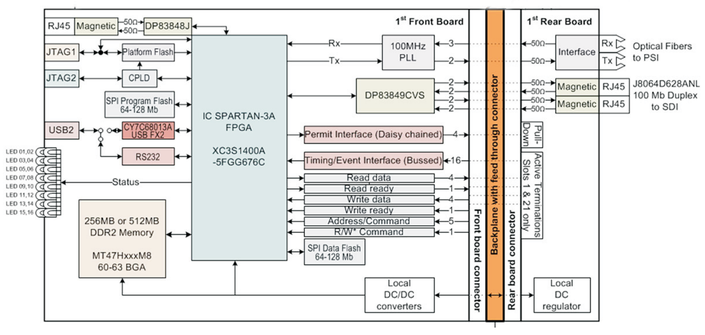
DAC and PFN signals for the injection kicker. Use of PSC allows change of DAC voltage during 100-ms interval synchronously with beam injections in hardware.

HARDWARE

A special set of devices was developed at BNL for the NSLS-II magnetic system Power Supplies (PSs) control [4]: Power Supply Controller (PSC) and Power Supply Interface (PSI). PSI is placed close to current regulators and is connected to the PSC via fiber-optic 50 Mbps data link.



Block-scheme of PSI.



Block-scheme of PSC.

PSC communicates with EPICS IOC (Input/Output Controller) through a 100 Mbps Ethernet port.

The main function of IOC includes ramp curve upload, ADC waveforms data download, and various process variables control. The PSC provides storage for up to 16 ramping tables for both DAC channels, and a 20-second waveform record for all ADC channels. The 100 Mbps Ethernet port enables real time display for 4 ADC waveforms.

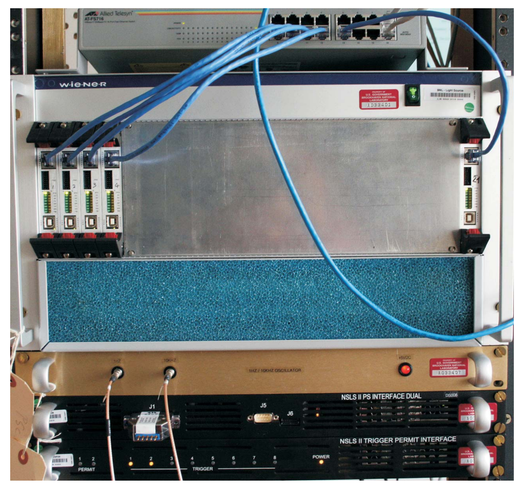
PSI Includes:

- one or two precision 20-bit DACs,
- three channels of precision 16-bit ADC for each DAC,
- six channels of 16-bit ADC for each DAC,
- sixteen digital inputs,
- 8 digital outputs.

PSC is equipped with

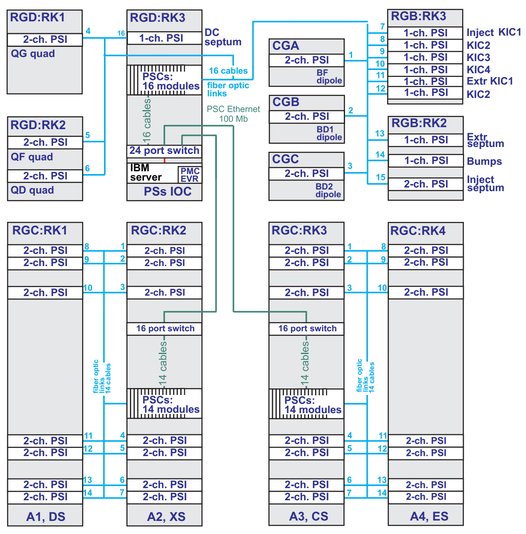
256 Mb DDR2 memory, which provides

- sixteen 40 kb ramp tables for each ADC channel
- 20-second waveform record for all ADC channels.



Set of equipment for the test stand.

BOOSTER POWER SUPPLIES CONTROL STRUCTURE



Block-diagram of the booster power supplies control.

All devices will be placed in racks in the injection service area near the booster tunnel.

There are 58 ramping PSs:

- 3 PSs for 3 groups of dipole magnets,
- 3 PSs for 3 groups of quadrupole magnets,
- 16 sextupole PSs,
- 36 PSs for corrector magnets.

Beam injection and extraction are provided by 9 pulsed and one DC PSs:

- injection and extraction septums PSs,
- extraction bump magnets PS,
- four injection and two2 extraction kickers PSs,
- DC extraction septum PS.

44 sets of PSC-PSI are proposed to be used for PSs control:

- 6 dual-channel sets for bending magnets and quadrupoles,
- 28 dual-channel sets for sextupoles and correctors,
- 10 single-channel sets for injection/extraction magnets.

It is supposed to use one IBM server (PSs IOC) to control all booster PSs. All PSCs will be distributed in three chassis and will be connected via switches in 1 Gbps network. Unlike NSLS-II storage ring PSCs [1], all booster PSCs are directly connected via Ethernet to IOC in the case of the booster control.

PSC OPERATIONAL PARAMETERS

PSC version described in this presentation is designed for the booster control.

commands:

- "Rst" resets all PCS registers to the initial state.
- "EnbI" is used for PSC disabling/enabling.
- "RampEnbl" is used for disabling/enabling of ramping mode.
- "BrkCmd#" breaks current ramp table processing and brings DAC# at "BrkRate#" (see below) rate to "BrkEnd#" state.

settings:

- "Mode" switches mode of PSC operation: Stop/Ramping Mode/Static Mode.
- "DoutMode" switches digital output mode: Static (level)/Pulse.
- "DoutPlsWdt" - pulse width (ms) in digital pulse mode.
- "ClkSrc" - updates clock source: external (from backplane)/internal 10 kHz.
- "ClkDivd" - clock divider factor (0 - /1; 1 - /2; …. 254 - /255) for changing of the ramp time.
- "ActvTbl#" selects DAC# active ramping table (0-15 for DAC1, 16-31 for DAC2).
- "InActvTbl#" selects inactive ramping table for download.
- "BrkRate#" sets DAC# break rate.
- "BrkEnd#" sets DAC# break end setpoint.
- "AdcID#" selects ADC channel for #-waveform reading.

indications:

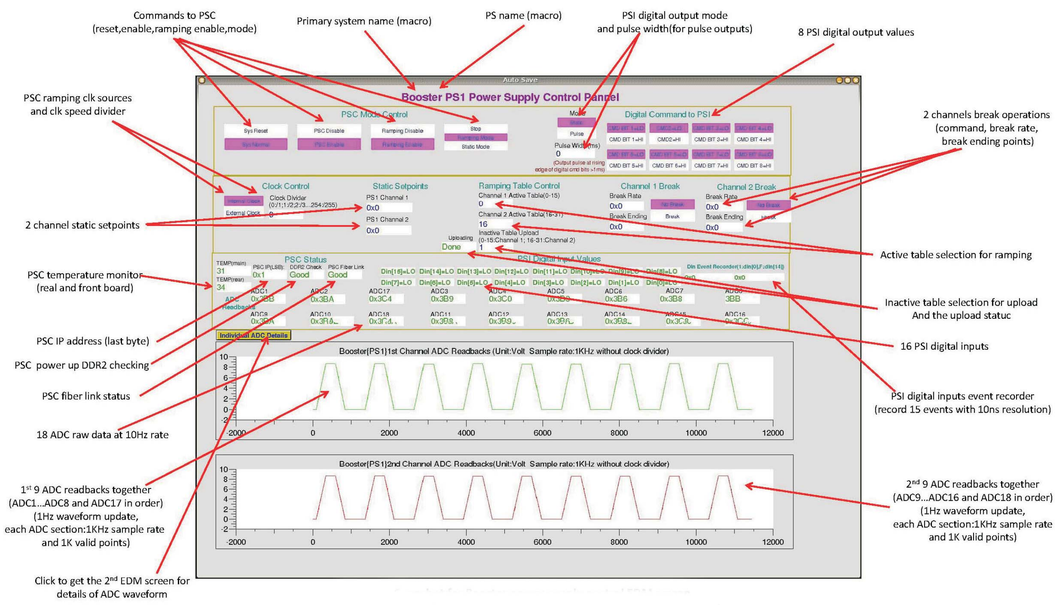
- "PscLoadingRamp" - PSC ramping table download indication (Loading or Done).
- "PscFrountT" - PSC main board temperature.
- "PscRearT" - PSC rear board temperature.
- "PscIP" - last byte of PSC IP address (192.168.1.x).
- "PscDDR2Check" - DDR2 memory check during bootloading (Good/Failed).
- "PscFiberSd" - status of fiber link between PSC/PSI (Good/Failed).

set/redback values:

- Writing eight values of digital outputs and two DAC setpoints (static mode of operation).
- Uploading from IOC determined by "InActvTbl#" ramping table of 40 kbyte data for ramping mode.
- Reading sixteen digital inputs and eighteen ADC values.
- Downloading to IOC of two 10 kHz ADC waveforms selected from ADC1-ADC16 in real time.
- Downloading to IOC of two 1 kHz ADC waveforms for both DACs in real time. Each ADC has 1280 points in the waveform.

PSI is capable of detecting the status change sequence of digital inputs with a 10 ns resolution.

ENGINEERING SOFTWARE

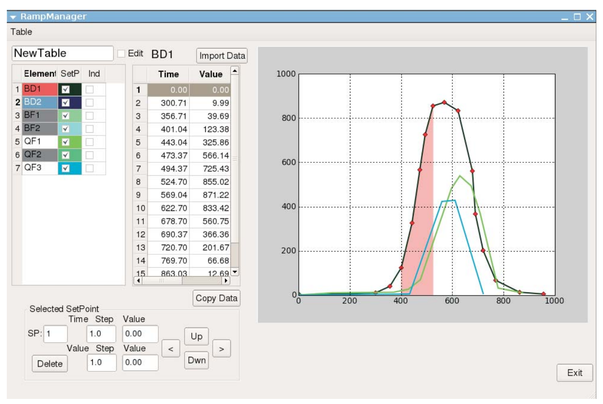


EDM screen is prepared for testing of all PSC/PSI signals and commands.

RAMP MANAGER

A Ramp Manager (RM) application for operation with PSs during commissioning of the booster is being developed now.

- RM will provide
- edition of ramp function tables,
- synchronization of different PSs tables,
- generation of ramp function tables and uploading it to IOC,
- storing/restoring tables,
- visualization of ramp functions and measured waveforms.



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