The Global Trigger Processor: A VXS Switch Module for Triggering Large Scale Data Acquisition Systems

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Introduction

The 12 GeV upgrade for Jefferson Lab's Continuous Electron Beam Accelerator Facility requires the development of a new data acquisition system to accommodate the proposed 200 kHz Level 1 trigger rates expected for fixed target experiments at 12 GeV. As part of a suite of trigger electronics comprised of VXS switch and payload modules, the Global Trigger Processor (GTP) will handle up to 32,768 channels of preprocessed trigger information data from the multiple detector systems that surround the beam target at a system clock rate of 250 MHz. The GTP is configured with user programmable Physics trigger equations and when trigger conditions are satisfied, the GTP will activate the storage of data for subsequent analysis.

Level 1 Trigger

The GTP serves as the central processor for the entire level 1 trigger system. Data are concentrated over a series of summations performed by the Crate Trigger Processor (CTP) and Sub-System Process (SSP) before arriving at the GTP as a continuously changing snapshot of all detectors participating in the level 1 trigger.

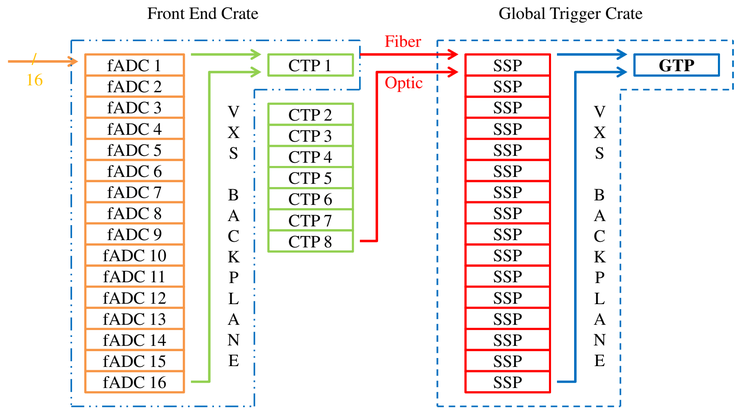

Figure 1: Level 1 Trigger Data Flow

Figure 1 shows the flow of data through the system and shows the scale of the complete trigger hardware. Equations one, two and three show the maximum supported number of front end crates, fADC modules, and analog detector channels, respectively.

16 SSP/System * 8 Crates/SSP = 128 Crates (1)

16 fADC/Crate * 128 Crates = 2048 fADC (2)

16 channels/fADC * 2048 fADC = 32,768 channels (3)

Using these data, the GTP simultaneously calculates up to 32 unique triggers based on equations defined by the user. These equations are configured in the FPGA fabric in a generic form, allowing modification of coefficients and other parameters. The Trigger Supervisor (TS) makes the final decision using the array of trigger signals and facilitates the distribution of triggers via Trigger Distributions modules (TD) to front end crates for permanent storage. Both TS and TD are housed in the Trigger Distribution Crate, none of which are shown in Figure 1.

VXS Elements

Leveraging the experience with VME communication protocols and hardware has helped shorten the time spent to develop the new trigger modules. In particular, VME boards share many elements with VXS payloads including power supplies, PCB stack-ups, board outlines, bus communication circuitry, and front panel hardware.

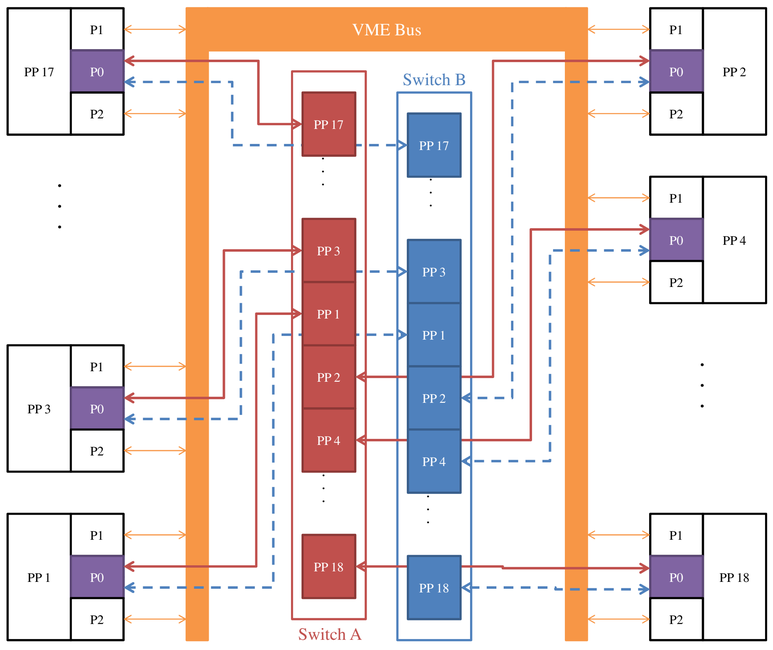

Figure 2: VXS Architecture Including VME[1]

Shown in Figure 2 is the logical configuration of a VXS system and the VME bus[1]. The addition of P0 and its connections to a standard VME board allows communication with both VXS switch cards resulting in a dual star configuration with up to 18 payloads. Note that the two switch cards do not interact directly with VME and must use VXS specific lines.

[1] Diagram is a modified version of one found in VITA's VXS Overview. http://www.vita.com/home/MarketingAlliances/vxs/VXS%20Overview.pdf

Hardware Implementation

The GTP features an Altera Stratix IV GX FPGA allowing interface to 16 Sub-System Processor modules via 32 5-Gbps links, DDR2 and flash memory devices, two gigabit Ethernet interfaces using Nios II embedded processors, fiber optic transceivers, and trigger output signals. The GTP's high-bandwidth interconnect with the payload modules in the VXS crate, the Ethernet interface for parameter control, status monitoring, and remote update, and the inherent nature of its FPGA give it the flexibility to be used large variety of tasks and adapt to future needs.

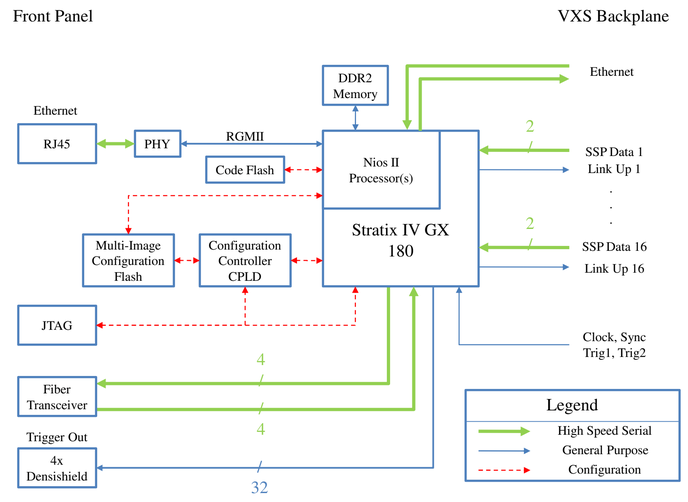

Figure 4: GTP Hardware Block Diagram

The configuration of primary hardware components is shown in Figure 4. The design is driven by its required high speed, memory, and Ethernet interfaces surrounding a high density FPGA. To support both non-volatile and remote FPGA configuration, both a CPLD (complex programmable logic device) with configuration control and reprogramming of Flash devices over Ethernet are used.

Figure 5: GTP Prototype

The GTP prototype is complete as shown in Figure 5 and hardware testing is underway. Many components have passed initial tests. Ethernet is a notable exception as it requires several completely working systems in order to begin evaluation.