INSTITUT MAX VON LAUE - PAUL LANGEVIN

NEUTRONS FOR SCIENCE ®

Network on Chip Master Control Board For Neutron's Acquisition

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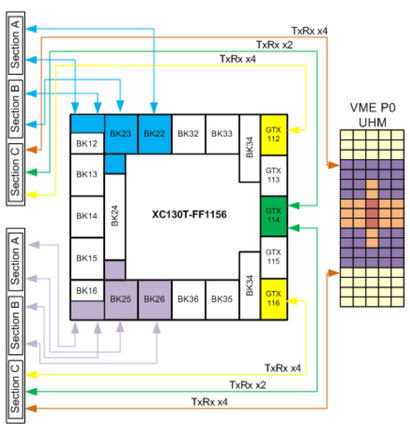
ABSTRACT

The acquisition master control board is designed to assemble the various acquisition modes in use at the Institut Laue-Langevin (ILL). The main goal is to make the card common for all the ILL's instruments in a simple, modular and open way, giving the possibility to add new functionalities in order to follow the evolving demand. It has been necessary to define a central element to provide synchronization to the rest of the units. The backbone of the proposed acquisition control system is the denominated master acquisition board. The complete system also includes a display board and *n* histogram modules connected to the neutrons detectors.

NETWORK ON CHIP (NoC)

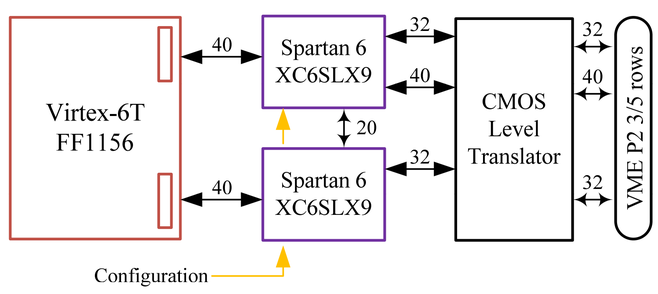
The master acquisition board consists of a VME64X configurable high density I/O connection carrier board based on latest Xilinx Virtex-6T FPGA. The internal architecture of the FPGA is designed as a Network on Chip (NoC) approach. It represents a switch able to communicate efficiently the several resources available in the board (PCI Express EP, VME64x Master/Slave, the DDR3 shared memories controller, the interrupt controller and user's area).

The MPF IO Expansion is based on SAMTEC QFS/QMS edge-to-edge right angle connectors. These connectors provide 156 SE signal contacts and 8 power contacts with up to 4.1[A] @ 85[ºC].

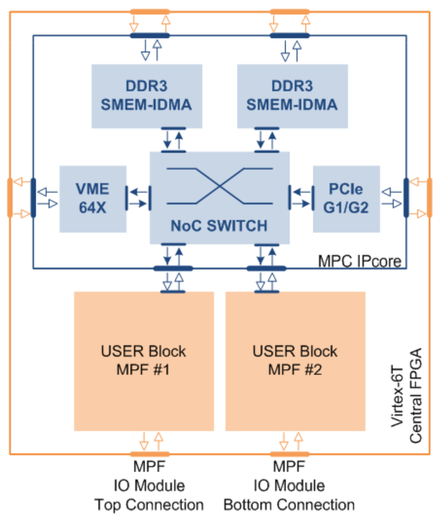


Front panel MPF

The VME P2 user IO (32+32+40 signals on 5-rows connector) is supported through the two Spartan-6 programmable routing infrastructure.



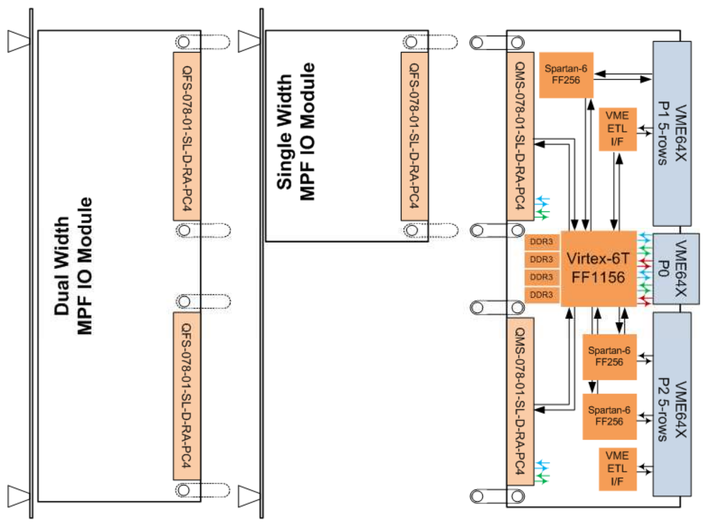
VME64X P2 user's IO



Network on Chip architecture

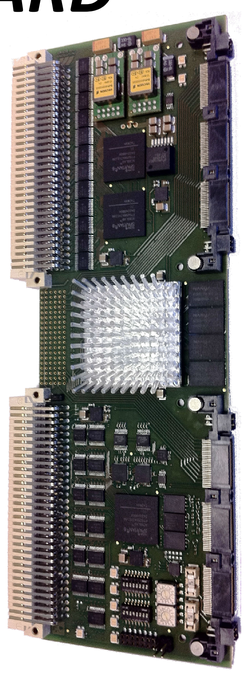
MPC 1200 CARRIER BOARD

Compared to other products based on mezzanine cards extension (i.e., FMC or XMC), the MPC 1200 Multi-Purpose Front IO (MPF IO) edge-to-edge interconnection solution provides:



MPC 1200 IO Carrier Interface

- × Full PCB area utilization
- × Direct access to the VME64X front panel without limitation on the IO connectors type.
- × Full VME component height allowing installation of heat-sink on critical devices.
- × Better physical and galvanic isolation for noise sensitive application.
- × Enhanced air cooling capability keeping modularity and versatility.



MPC 1200 top side

Features:

- × 6U VME64x board with 2eSST support.
- × Based on latest XILINX Virtex-6T 40mn FPGA.
- × Modular IO Expansion with full front panel access (MPF – Multi-Purpose Front IO).
- × 5V tolerant VME64x P2 user IO with Spartan-6 IO Support.
- × On-board DDR3 Memory.
- × Native PCI Express GEN2 support over VME64x P0 and/or front-end MPF.
- × TOSCA II FPGA architecture:
  - — Optimized for XILINX Virtex-6 FPGAs.
  - — PCI Express GEN2 EP/RC.
  - — Network on Chip (NoC) architecture.
  - — Shared Memory.
  - — VHDL source code fully available.

IMPLEMENTATION

- × The master acquisition board has been developed using the user area of the TOSCA II architecture.
- × Each acquisition mode in use at the ILL is developed in a functional and independent block.
- × The front end interface and the P2 signals are configured according to the needs of the instruments.

Acquisition modes

Simple integral count

- Counting time from 100 ns to $(2^{64}\text{-}1)\cdot 10^{8}$ *s*.

Time of flight (ToF)

- Rotation chopper flux pulsed up to 500 Hz.
- Histogram arranged as a function of their arrival time.
- Up to 2048 channels (variable duration).

ROC (Oscillating Radial Collimator)

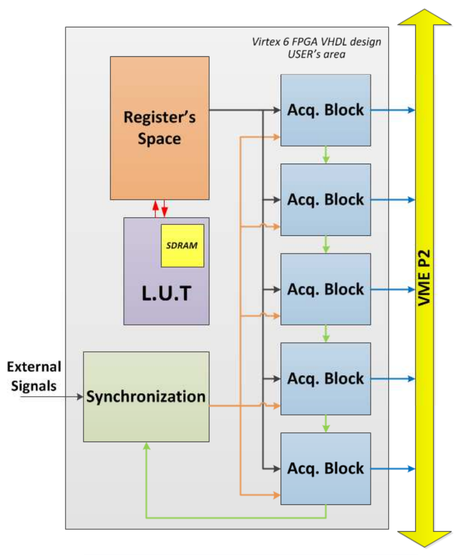
Position Sensitive Detectors.
- Neutron's count coordination depending on the movement of the collimator.

Kinetic

- Soft matter studies with long duration in time.
- Time slice histograms according to the neutrons arrival time.
- Combination ToF + kinetic is possible.

Doppler

- Backscattering spectrometers equipped with a Doppler motion at the monochromator.
- The acquisition card produces a histogram where the neutrons are accumulated into the corresponding equidistant velocity channels.



Master acquisition design