Comparative Evaluation of IEEE-1588 Precision Time Protocol for the Synchronized Operation of Tokamak Device

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Background

- This work was initiated for the validation of Time Communication Network using IEEE1588-2008 of ITER. So, some documents of ITER were referenced and the drivers for IEEE1588 boards were used for the test.
- However, it is <u>at an early stage</u> and much progress has not achieved, yet.

Outlines –

- Introduction of IEEE1588 Precision Time Protocol
- Application in fusion devices
- Comparison with other protocols
- Conclusions



IEEE1588 Standard

- IEEE1588 : Precision Time Protocol (PTP)
- It is a standard for a Precision Clock Synchronization Protocol for networked measurements and control systems using Ethernet communication network
- Two versions released :
 - version 1 : IEEE1588-2002
 - version 1 : IEEE1588-2008
- It is possible to synchronize distributed clocks with an accuracy of less than 1 μsec
- It uses UDP packet communication based on TCP/IP protocol stack
- It works inside LAN (PTP Domain)





IEEE1588 Standard - Features

- Master-Slave Hierarchy
- Best Master Clock Selection Algorithm
- Fault tolerance

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- Hardware time-stamping
- Low cost to implement
- Limitation in v.1 vs. Improvement in v.2 :
 - Slow Sync message rate : 2sec
 - ⇒ Higher Sync message rate : less than 100ms
 - -Traffic congestion : non-optimized message size

⇒ 'Shorter Sync Message'

- Non-linear effect on jitter : cascaded boundary clock
 introducing 'Transparency Clock'
- No correction for asymmetry error : network asymmetry
 ⇒ Introducing 'Correction Mechanism'

Basic Synchronization – Message-based Two Way Transfer

Version 1



- Step 1 : Propagation delay measurement T_{LD}=((T_{S2}-T_{M1})-(T_{M4}-T_{S3}))/2, if T_{LD}= T_{MS} = T_{SM.} symmetric link)
- Step 2 : Offset measurement

Version 2



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Best Master Clock Selection Algorithm

- <u>State Decision Algorithm</u>: to produce a recommended state by comparing all relevant data sets
- Data Set Comparison Algorithm : to select clock from better

Transparent Clock



- Correction Field in TC
 - Original Timestamp : 48bits in sec + 32bits in ns
 - Correction Field : 48bits in ns + 16bits in scaled fractional ns
 - . Sub-ns accuracy
 - . Transparent correction + asymmetry correction

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Use case in ITER

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- ITER is the biggest project in the world to construct a superconducting experimental reactor in cooperation with 7 states
- ITER control system, CODAC, aims at standardization by using the latest, but performance-proven technologies
- They decided IEEE 1588-2008 as a standard for TCN to synchronize time
- Also, they performed evaluation test using several COTS products
- And, they got results as follows :
 - Confirm basic functions
 - Time jitter less than 50ns,rms
- Acronyms :
 - ITER : International Thermonuclear Experimental Reactor
 - CODAC : Control, Data Access, and Communication
 - TCN : Time Communication Network



• Use case in ITER

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Use case in ITER _ Test Results

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Figure 3. Oscilloscope output of the IEEE 1588-2008 compatibility testing where Channel 1 (yellow) represents the 1PPS signal output from the Grandmaster, Channel 2 (magenta) represents the 1PPS output of the 1^{st} PPT slave, and Channel 4 (green) represents the 2^{nd} PTP slave.

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Histogram of Phase Deviation

Evaluation Test in KSTAR

- To verify the basic functions of IEEE 1588 (PTPv2) :
 - Time synchronization
 - Time Accuracy and Jitter
- Setup : a Grandmaster + 3 Slaves





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Evaluation Test in KSTAR Confirm time synchronization using PTPv2



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Evaluation Test in KSTAR

- Measure 1PPS of a Grandmaster and 3 Slave boards
- Measure time differences between slave cards
- (5 Pulses, Period 1us, Width 100ns (repeat 5 times)





KSTAR

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Customized Protocol – e.g. KSTAR Timing Protocol

- **Providing 'Synchronized Time' and 'Synchronized Events'** ۲
- Using home-made timing protocol ۲
- Master time reference to GPS time
- **<u>Dedicated</u>** optical timing network using <u>Star-topology</u>





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¹³Comparison with Other Timing Systems

Customized Protocol – e.g. KSTAR Timing Protocol



Specification	V.2
Timing accuracy	max. 5ns (1 tick)
Timing Jitter	<100ps,max
Output clock	1Hz ~ 100MHz
Trigger/Clock output	8, configurable
Multi triggering sections	8, configurable
Optical communication speed	2 Gbps
FPGA	Spartan-6 (150K logic cells)
IRIG-B GPS time decoding	0
PMC Form-factor, PCI/PCI-x	32/64-bit, 33/66MHz
EPICS device driver in	Vxworks, Linux 2.4x/2.6x





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Comparison with Other Timing Systems

WHITERABBIT

- To provide precise timing and events distribution for high-end real-time system
 - Sun-nanosecond timing accuracy
 - (using compensation of signal propagation delay)
 - Packet loss : 10⁻¹²
 - (forward error correction and introduction of QoS)
- WR timing network : a deterministic field bus based on synchronous giga-bit Ethernet and Precision Time Protocol
- It operates with completely open license on hardware and software
- It is a growing future protocol and currently working prototype is released

Conclusions

Pros and Cons

Generally Spoken Advantages

- Easier and Cheaper implementation
- Suitable for widely distributed facilities
- Non-time critical applications
- Commonly proven technology
- Guaranteed long time

Weaknesses for Tokamak Operation

- Lack of event synchronization
 - Need extra cost to provide synchronized events
 - Synchronized sampling clock signals are also necessary for data acquisition
- Somewhat, insufficient timing accuracy
 - to support high-speed DAQ systems





References

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