NSLS-II Filling Pattern Measurement

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Abstract. A Multi-bunch injection will be deployed at NSLS-II. High bandwidth diagnostic beam monitors with high-speed digitizers are used to measure bunch-by-bunch charge variation. The requirements of filling pattern measurement and layout of beam monitors are described. The evaluation results of commercial fast digitizer Agilent Acqiris and high bandwidth detector Bergoz FCT are presented.

Introduction

In order to minimize intensity-correlated orbit oscillations due to uneven bunch patterns, we need to measure the filling pattern (also named bunch pattern or bunch structure) and then find a way to minimize bunch-to-bunch variation of current (or charge) if the variation exceeds 20%.

NSLS-II Filling Pattern

NSLS-II storage ring contains 1,320 RF buckets at 500 MHz. To alleviate the problems of ion trapping in the stored electron beam, approximately one-fifth of the buckets must be left empty. NSLS-II Injector will support uniform filling pattern in the storage ring. Two basic patterns were considered (two upper plots in Figure 1): uniform fill with the ion-clearing gap of about 20%; multiple uniform bunch trains with mini-gaps between them.

In addition to the nominal uniform fill, consideration is being given to specialized and complex bunch patterns: a single high-current bunch (named "camshaft" bunch, two lower plots in Figure 1) located in the middle of the ion-clearing gap; multiple camshaft bunches whose repetition rate is matched to the pulse format of modern pump lasers.

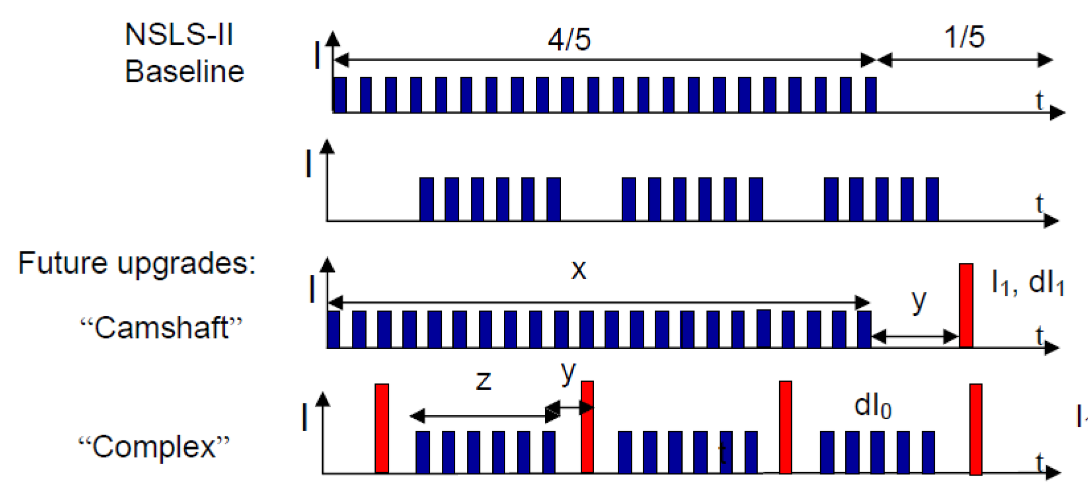

Figure 1: NSLS-II Filling Pattern

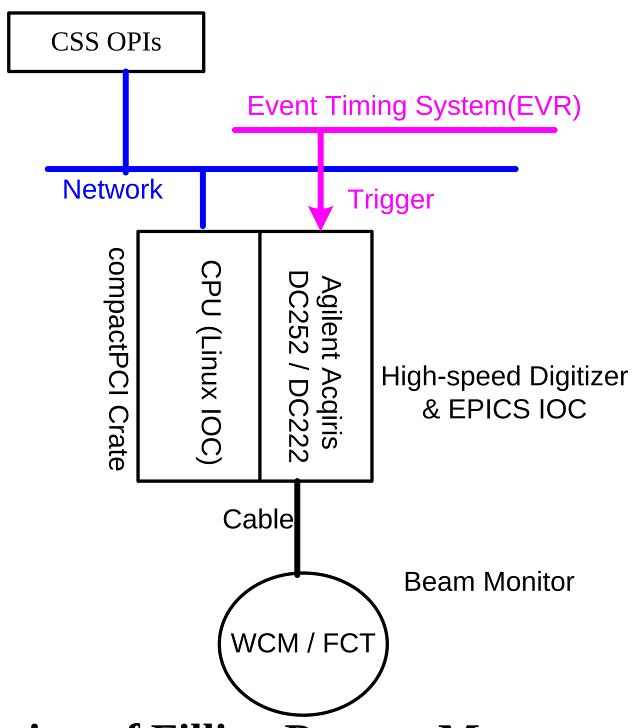

Figure 2: Overview of Filling Pattern Measurement

NSLS-II filling pattern measurement system provides relative bunch-to-bunch charge distribution along with the whole machine. This measurement requires combination of beam monitors (WCM, FCT, etc.), data acquisition (DAQ) and controls (fast digitizer, EPICS software, etc.) and Event Timing system. Figure 2 shows the system architecture.

There will be 3 types of beam monitors distributed around the machine and all of them have very high bandwidth (>1 GHz): 5 wall current monitors (WCM) in Linac, 2 Bergoz FCTs (fast current transformer) in LtB, 1 FCT in BSR, 2 FCTs in BtS and 1 BPM (beam position monitor) button in Storage Ring.

Controls

High-bandwidth filling pattern monitor requires high-speed digitizer to sample its analog output signal. The minimum sampling rate of the digitizer required to discriminate 500 MHz bunch-to-bunch information is 1GS/s.

Hardware

Agilent U1065A Acqiris high-speed compactPCI digitizers (DC252 and DC222, 10-bit resolution, 2 GHz bandwidth, DC252 is 2-channel, 4 GS/s per channel, DC222 is 1-ch with 8GS/s) are selected for NSLS-II filling pattern measurement. Beam monitors associated with controls hardware in each sub-accelerator are listed in Table 1.

Table 1: Filling Pattern Monitors & DAQ Hardware

Sub-accelerator	Beam Monitor	Digitizer
Linac	6 WCMs	3 DC252
LtB	2 FCTs	1 DC252
Booster	1 FCTs	1 DC222
BtS	2 FCTs	1 DC252
Ring	1 BPM	1 DC222

Software

The EPICS driver for Acqiris digitizer is originally developed at SLAC. Several improvements are made at NSLS-II, including a few bug fixes and filling pattern related data processing.

Here's the basic implementation of our filling pattern measurement: the filling pattern EPICS IOCs will provide the following data: number of bunches (max. 150), normalized filling pattern (array data like filling[150]: 0.85, 1.00, 0.96, …), maximum bunch-to-bunch variation (i.e. $\Delta Q = 5\%$), individual bunch charge calibrated against ICT or DCCT or computed from integral voltage signal. If measured $\Delta Q < 20\%$, our job is done; If $\Delta Q >= 20\%$, we need to find out what's the cause and find a way to minimize ΔQ.

Bench Tests

Bench Tests on FCT

We have purchased 5 Bergoz FCTs and performed acceptance tests. We have measured FCT bandwidth using network analyzer. Figure 3 shows that one of the FCTs has ~ 1GHz BW (-3dB).

Bench Tests on Acqiris

We have completed performance evaluation on the ultra fast digitizer Acqiris DC252, including max. sampling rate at 8 GS/s by combining 2 channels to 1 channel (interleaving), effective number of bit (ENOB), etc. The input test signal is 500MHz sine wave, 0.9Vpp.

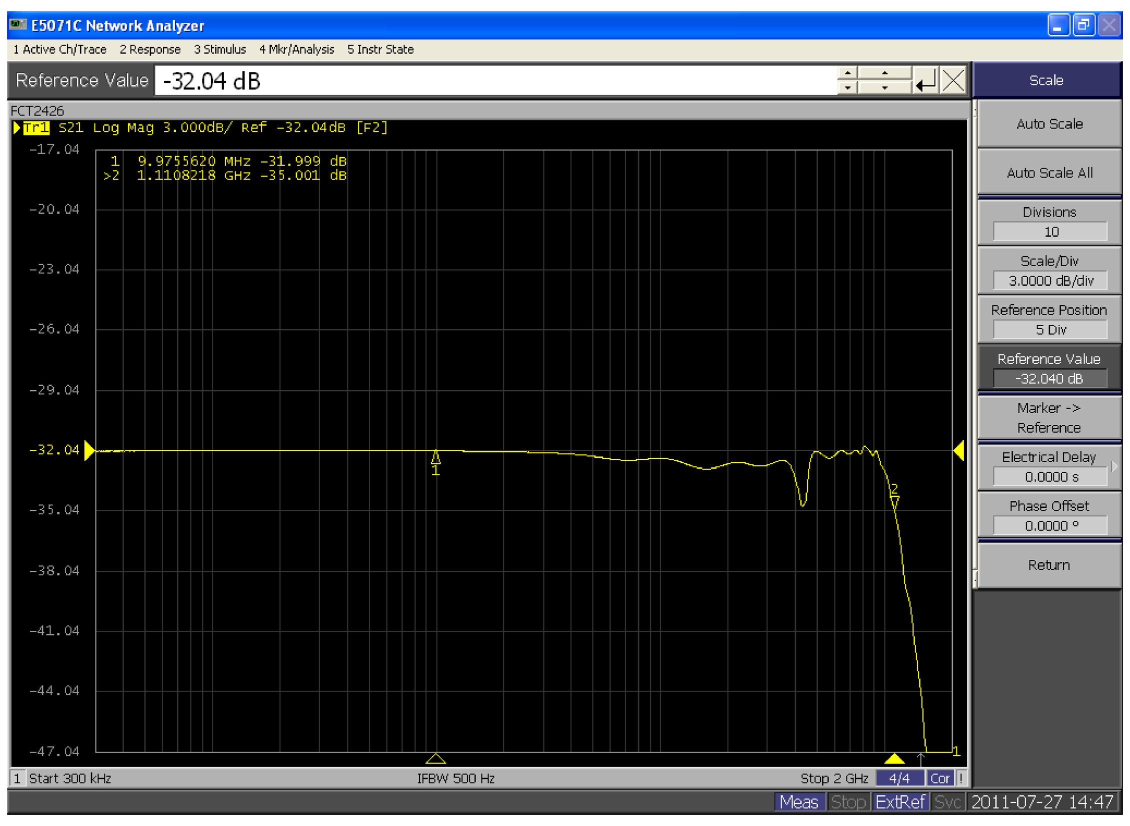

Figure 3: FCT Bandwidth Measurement

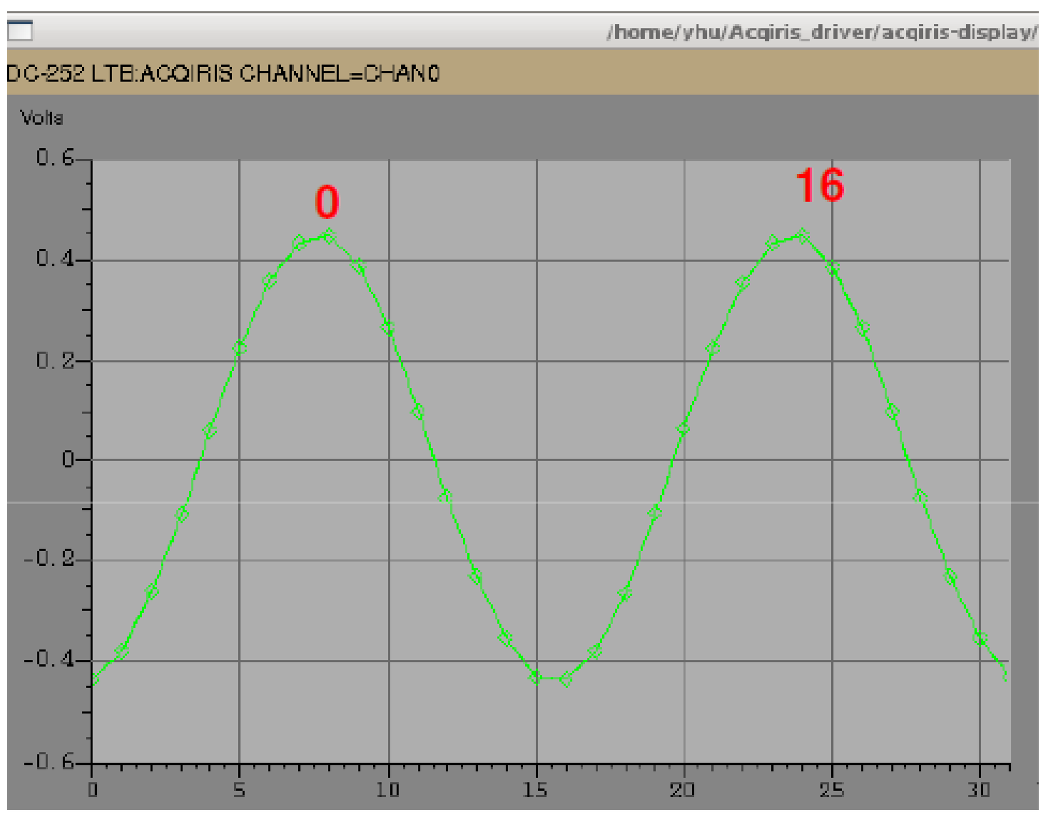

Figure 4: 8GS/s acqiris Digitizer

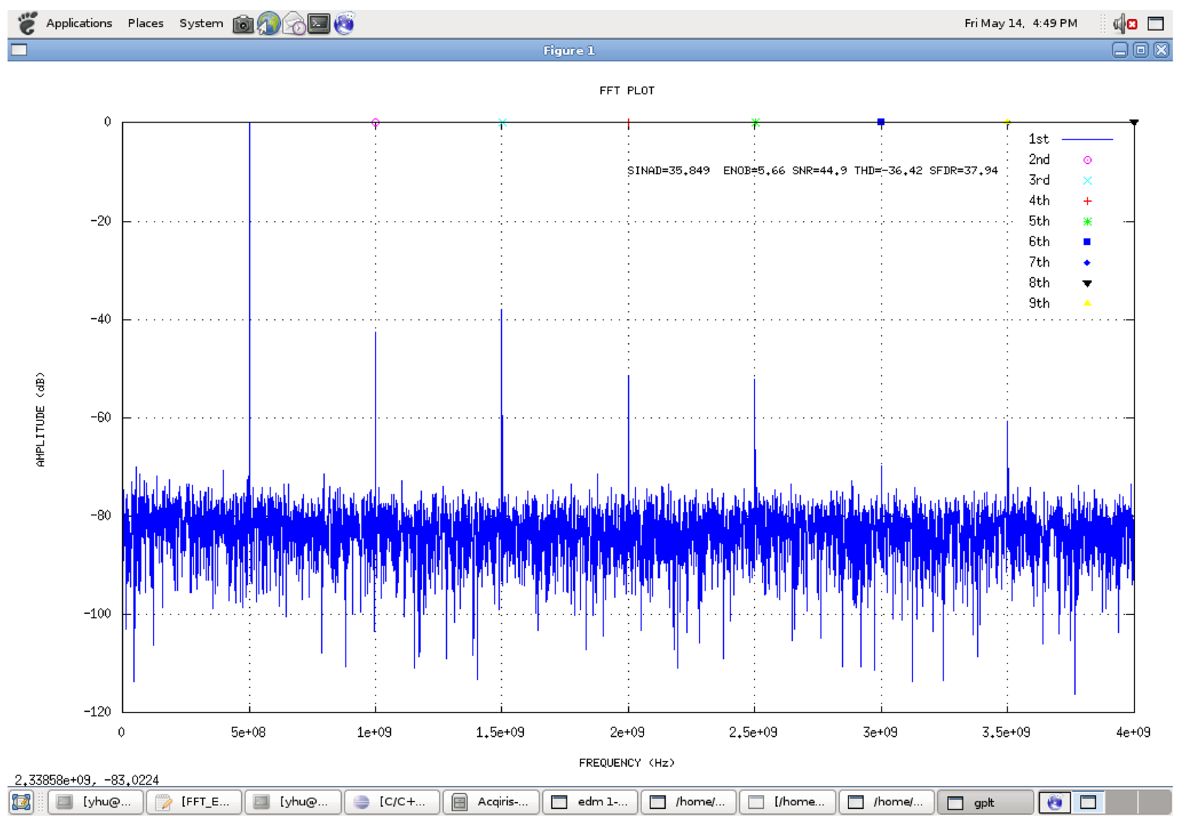

Figure 5: 7-bit ENOB after Sine-wave Data-fitting

Filling Pattern Simulation

In order to test our algorithm software for filling pattern measurement as well as interface to Event timing system, we have setup a test stand to simulate filling pattern as shown in Figure 5.

1) Timing EVG/EVR: provides 2 triggers, one is for triggering digitizer, the other for triggering pulse generator;

2) pulse generator DG645: receive external trigger from EVR and then use burst mode to generate multiple pulses with 2ns width and 10MHz rate;

3) FCT: input signal from DG645 and output to digitizer;

4) Acqiris digitizer: triggered by EVR and acquire FCT signal;

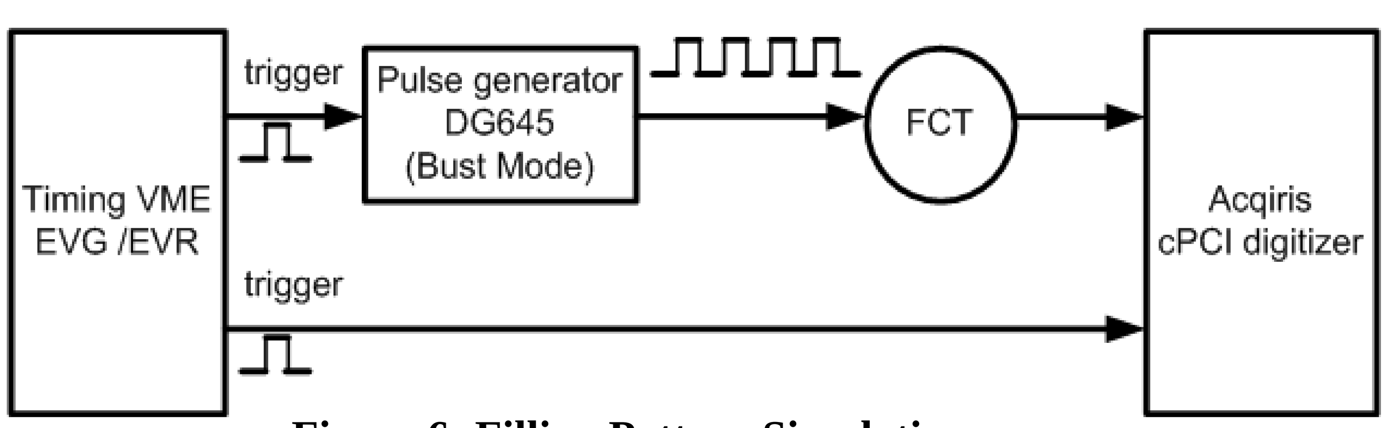

Figure 6: Filling Pattern Simulation

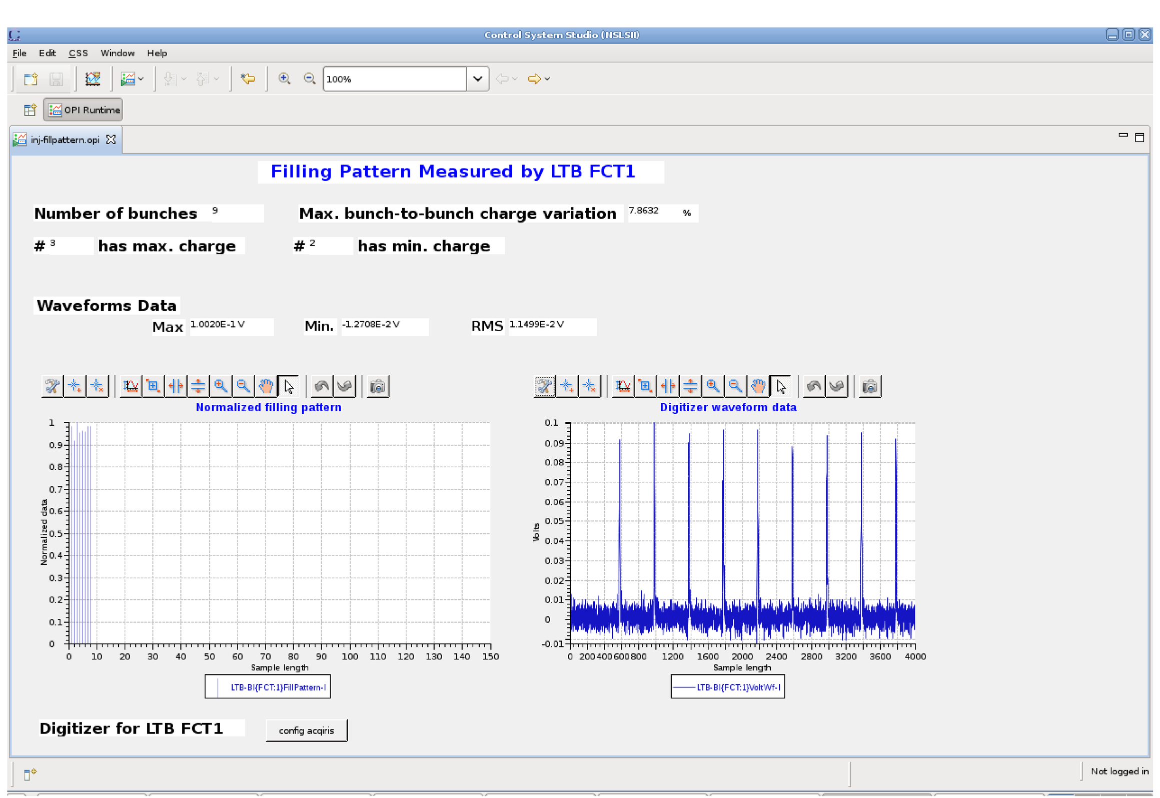

Figure 7: Filling Pattern Simulation Result