Control System for Linear Induction Accelerator LIA-2: the Structure and Hardware

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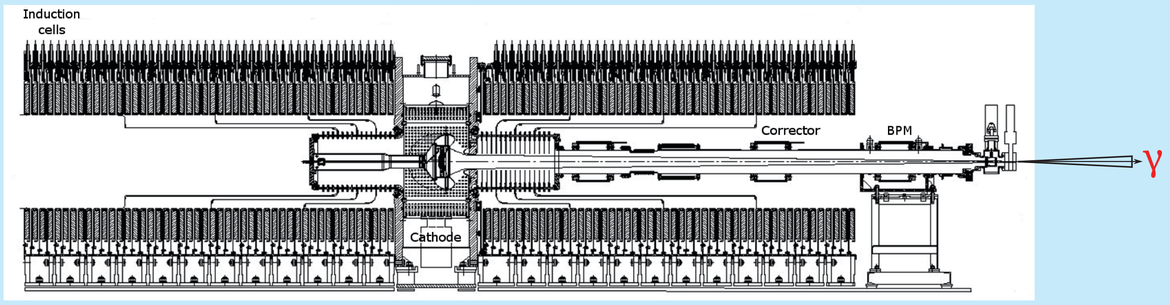
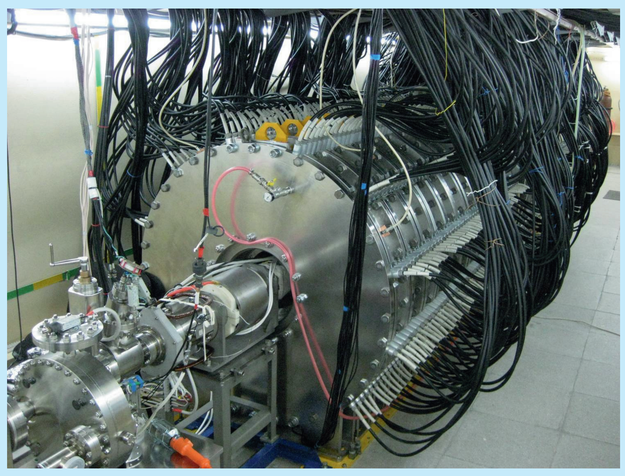
LIA-2 for Flash X-Ray Radiography

LIA-2 was originally designed as an injector for 20 MeV linear induction accelerator, but it can be used as an independent 2 MeV X-ray source for flash radiography with high space resolution.

LIA-2 Accelerating Structure



The accelerating stucture includes 1 MV, 2kA diode with dispenser cathode and 1 MV accelerating section. Both sections include linear chain of 96 induction cells put on accelerating tube.

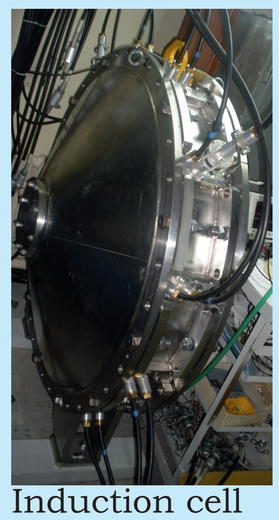


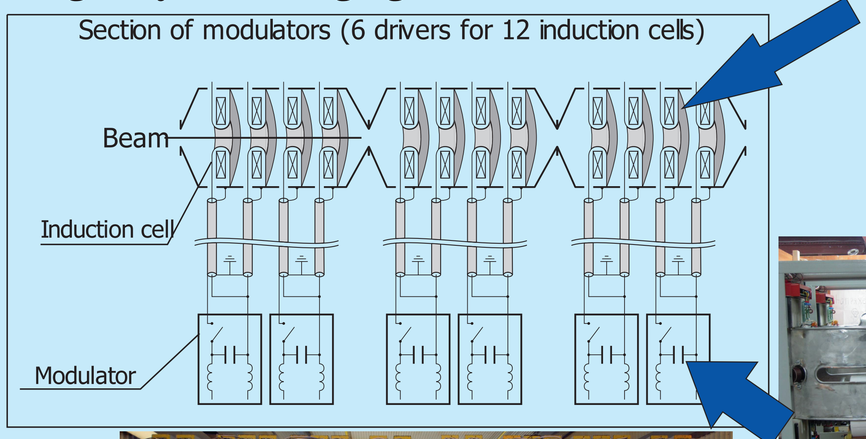
Beam diagnostic system consists of two beam current transformers, capacitor-based pulsed voltage dividers, X-Y strip-line beam position monitor (BPM) and movable Faraday cup.

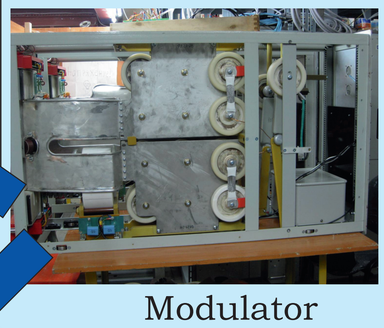
High-voltage System

48 modulators = 8 sections x 6 modulators
First MeV : Sections 1-4
Second MeV: Sections 2-8

Output pulse voltage is 50 kV, duration – 300 ns, output current comes up to 5 kA. Each modulator feeds two induction cells. Forming networks are charged by two charging devices.

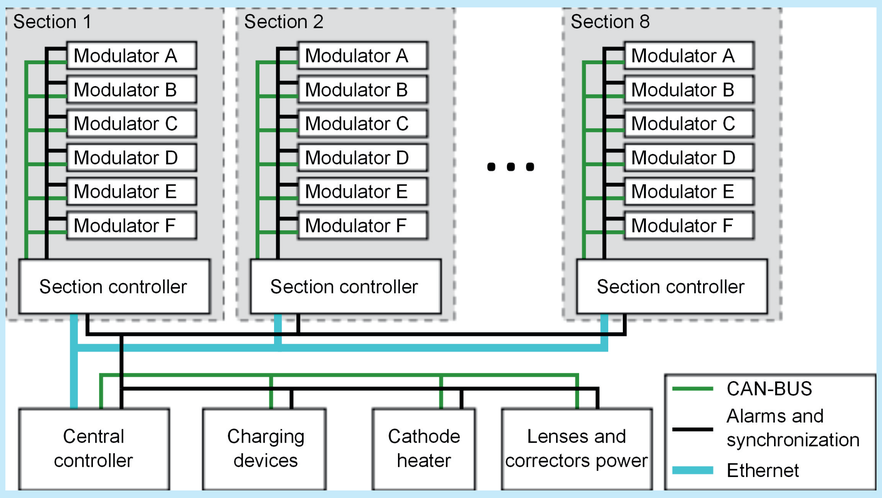

Induction cell




Modulator

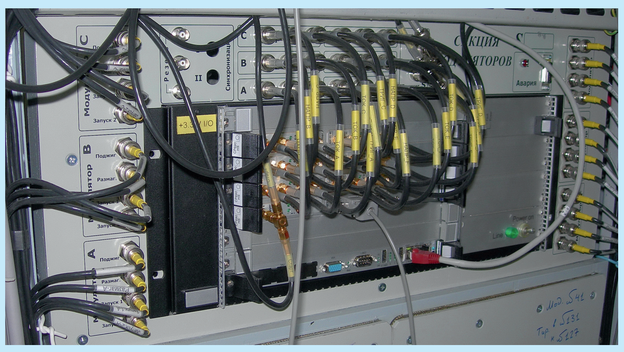
Section 1 Section 8

Control System Structure



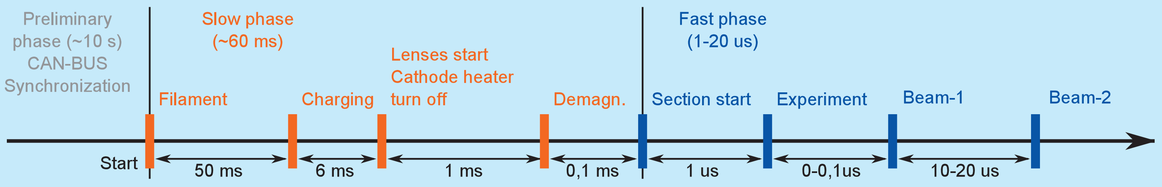
Section controller is installed directly in modulators rack:

- Synchronizes and controls 6 modulators
- Controls inductors currents and voltages

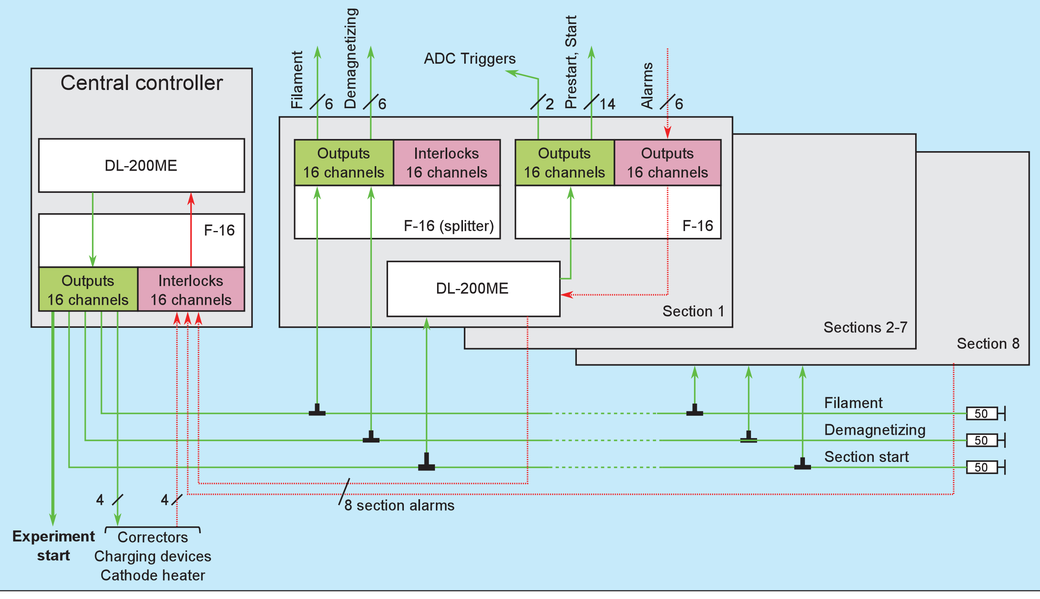


Synchronization and interlock subsystem

Time diagram



Scheme (288 timing channels total)

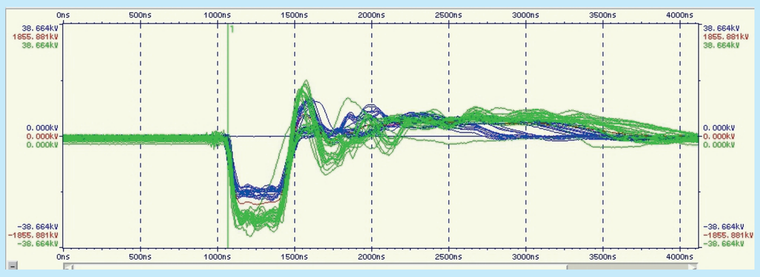


Waveform recording subsystem

More than 200 waveforms recorded, stored and analyzed each shot to provide stability information.

108 "fast" (300-1000 ns) channels including voltages and currents from all inductors, signals from BPM, Faraday cup, voltage dividers and current transformers.

Around 100 technological channels including demagnetizing voltage, charge on forming network, corrector currents.



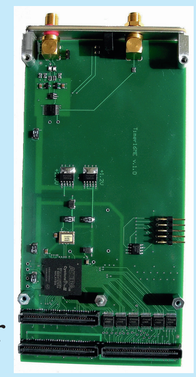
Developed Hardware

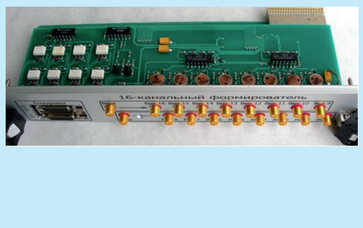
CompactPCI PMC architecture was chosen as a modern widespread standard. Hardware directly interfacing to HV devices is developed and produced in BINP.

DL200-ME

Digital delay line

- two modifications
- 16 output channels
- 5 ns (80 ns) step
- Jitter < 0.5 ns
- 15 bit (23 bit) counter
- 16 interlock channels
- 2 alarm channels



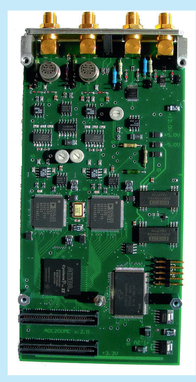


F-16

2x8 splitter/16 forming line

- 16 output channels
- 200 ma output current
- decoupled outputs

Waveform recorders



	ADC200-ME	ADC812-ME
channels	2 simultaneous	8 simultaneous
rate	200 MSPS	5 MSPS
accuracy	12 bit	12 bit
memory	1Mx2x12 bit	256Kx8x12 bit