IFMIF LLRF Control System Architecture Based on EPICS

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Abstract

The **IFMIF-EVEDA** (International Fusion Materials Irradiation Facility - Engineering Validation and Engineering Design Activity) **linear accelerator** will be a 9 MeV, 125mA CW (Continuous Wave) deuteron accelerator prototype to validate the technical options of the accelerator design for IFMIF. The primary mission of such facility is to test and verify materials to prepare for the design, construction, licensing and safe operation of a fusion **DEMO** (Fusion Demonstration Reactor). The LLRF (Low-Level Radio Frecuency) controls the amplitude and phase of the signal to be synchronized with the beam and it also controls the resonance frequency of the cavities. The system is based on a commercial cPCI (Compact Peripheral Component Interconnect) FPGA (Field Programmable Gate Array) board provided by Lyrtech and controlled by a Windows.

Motivation: To build a device support that ***communicates the cPCI FPGA board with the EPICS Channel Access*** and to **integrate the solution to the IFMIF-EVEDA control system.**

RF Local Control System

• Each RF [3] module comprises 2 RF Chains.

•18 RF Chains will be monitor and controlled by 9 RF Module-LCS [2].

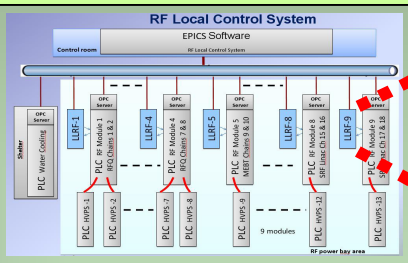

Figure 2. LLRF local control system scheme

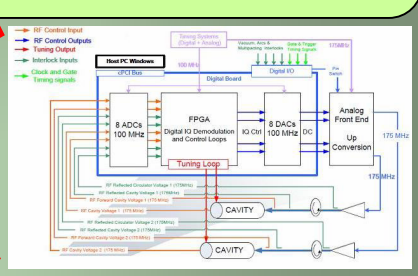

Figure 1. LLRF System general overview

Control System Operation

• The LLRF control system has many operating modes and more than **300 parameters to configure**.

• The control system operation is divided between **Loops board and Diagnostic board**.

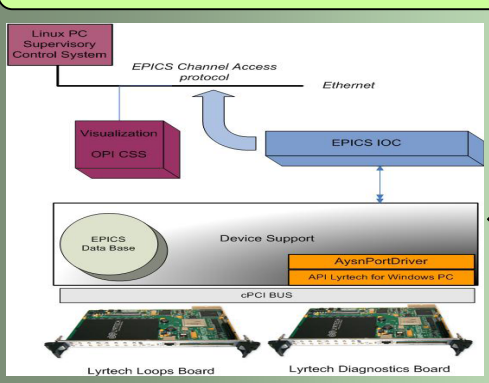

Figure 4. LLRF Control Flow

Correspondence between IFMIF-EVEDA five layers structure and our proposed LLRF EPICS based [1] control architecture.

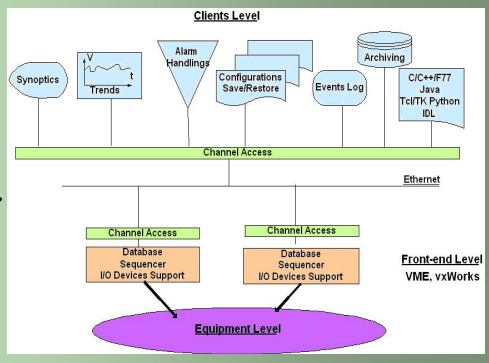

Figure 3. EPICS five layers structure

LLRF Test Bench

• A **RF generator**. The RF generator provides a 175MHz, 18dBm signal to upconvert the DC control outputs of the digital board.

• The **LLRF itself** that is composed of Digital Board: **The digital board** contains one Virtex-4 FPGA, 8 ADCs and 8 DACs, **the front end** that It is in charge of up-converting the DC control outputs from the digital board into RF and the local timing system.

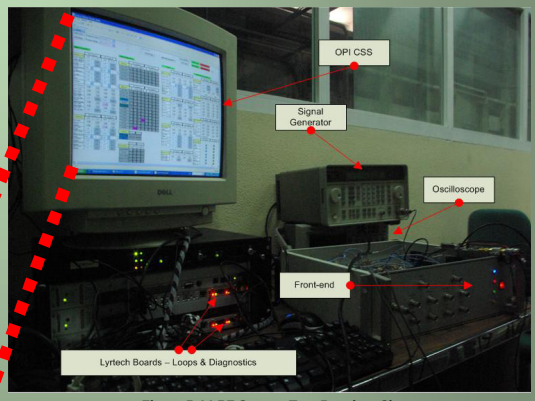

Figure 5. LLRF System Test Bench at Ciemat

OPI CSS

• Friendly and operative GUI.

• **Tune** the system and **control** the parameters.

• **Whole logic** involved have not been developed in the client level but **on the IOC**

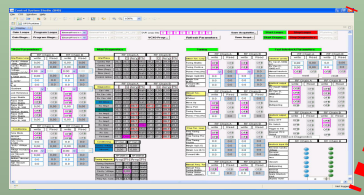

Figure 6. OPI CSS

Conclusion

We have developed a **Device Support for IFMIF-LLRF Control System**. This new software architecture is running properly in a Windows CPU connected in the same chassis of the Lyrtech cPCI board and **solves the operating system dependency**. This new architecture allows both client and server run in different machines. This solution will be used to control the LLRF of two plants in the final accelerator prototype which will be built in Rokkasho, Japan, on the 2013.

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[2] I. Kirpitchev, P. Mndez, M. Weber, A. Ibarra, M.A. Falagan, M. Desmons, A. Mosnier. 5 "RF POWER SYSTEM FOR THE IFMIFEVEDA PROTOTYPE ACCELERATOR". Proceedings of EPAC 2004, Lucerne, Switzerland. CIEMAT, Avda. Complutense 22, 28040 Madrid, Spain and CEA, IRFU, F-91191 Gifsur-Yvette, France, 2008.
[3] International Energy Agency. "IFMIF Comprehensive Design Report, January 2004".

ACKNOWLEDGEMENTS: This work is funded by Ministerio de Ciencia e Innovación del Gobierno de España, under the Project No. AIC10-A-000441