Design of a Digital Controller for ALPI 80 MHz Resonators

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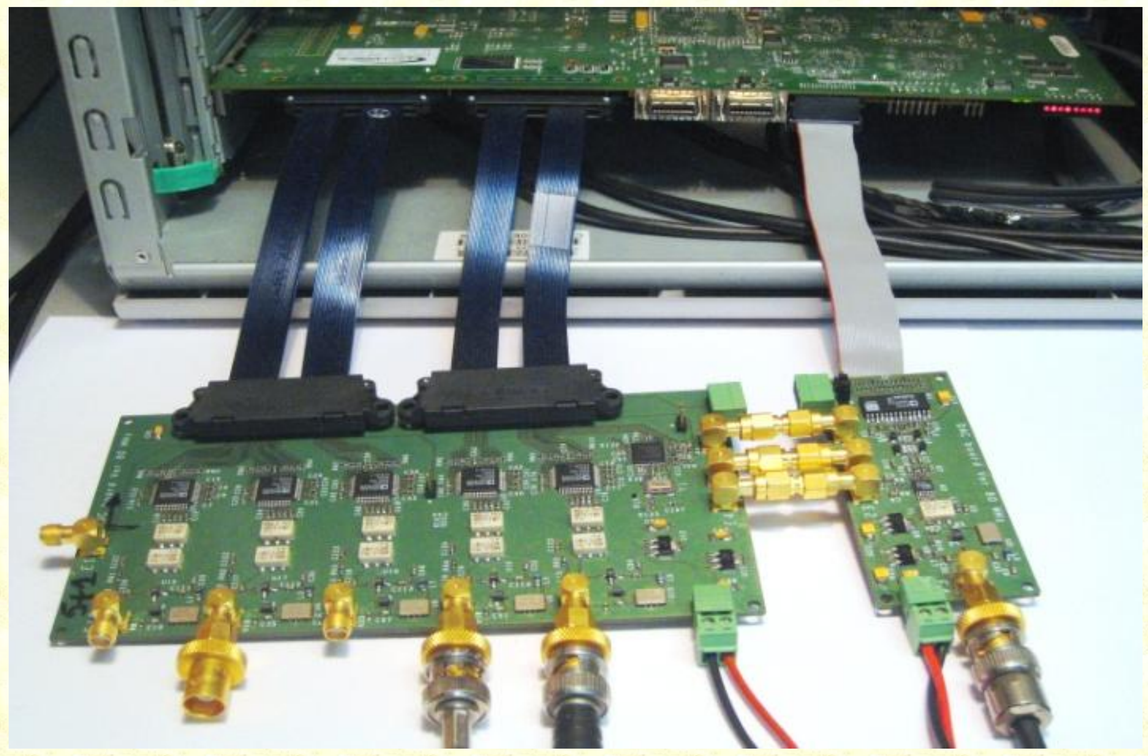
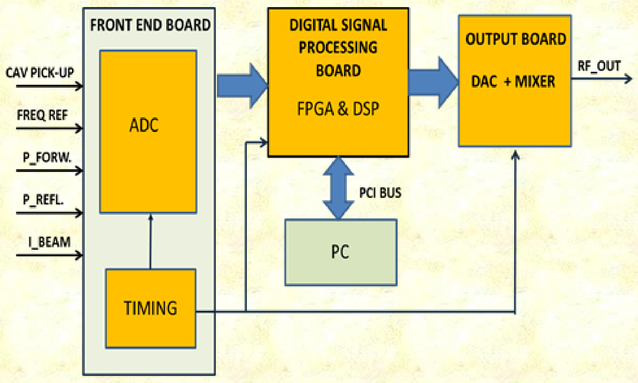
Abstract

We discuss the design of a resonator controller based mainly on digital technology. The signal frequency is 80 MHz but can be easily increased up to 350MHz; the controller can work in either “Generator Driven” (GDR) or “Self-Excited Loop” (SEL) mode. The signal processing unit is a commercial board (Bittware T2-Pci) with Xilinx Virtex II-Pro FPGA and 4 TigerSharc DSPs. The front-end board includes a set of A/D channels which sample the RF signals coming from the cavity pickup and from the reference generator. We present the results of some preliminary tests carried out on 80 MHz quarter wave resonator installed in the ALPI Linac accelerator at INFN-LNL and discuss possible developments of this project.

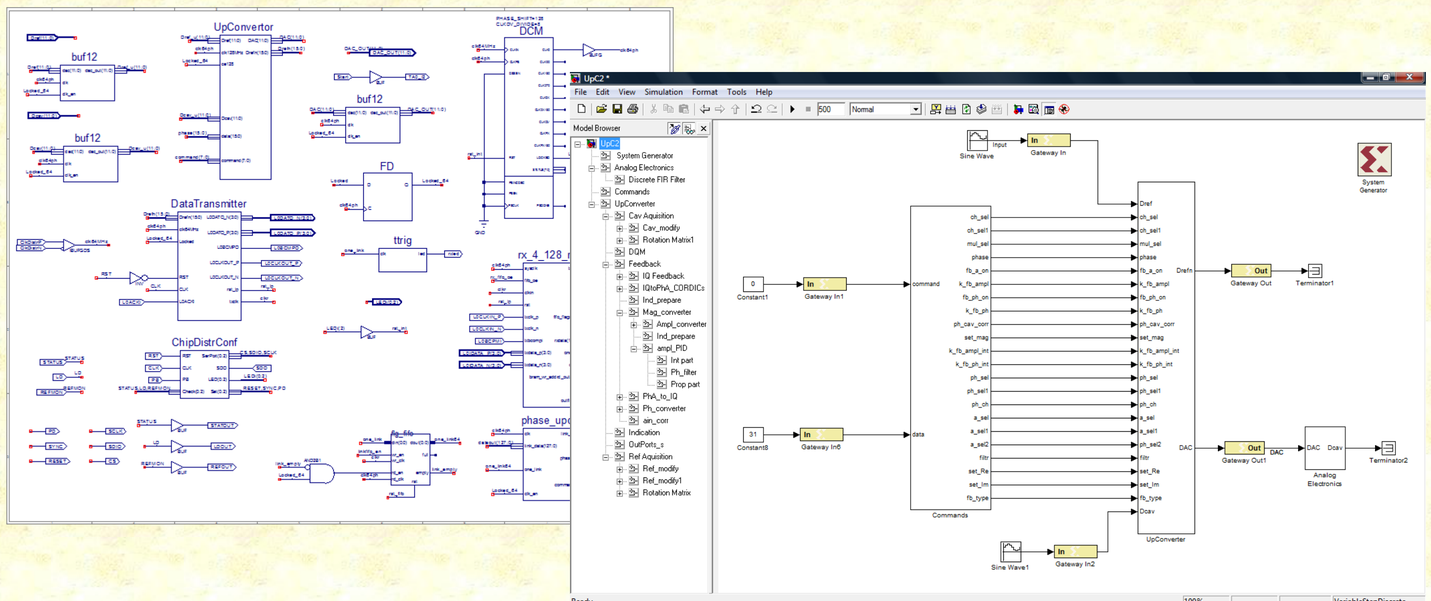


RF CONTROLLER DESCRIPTION

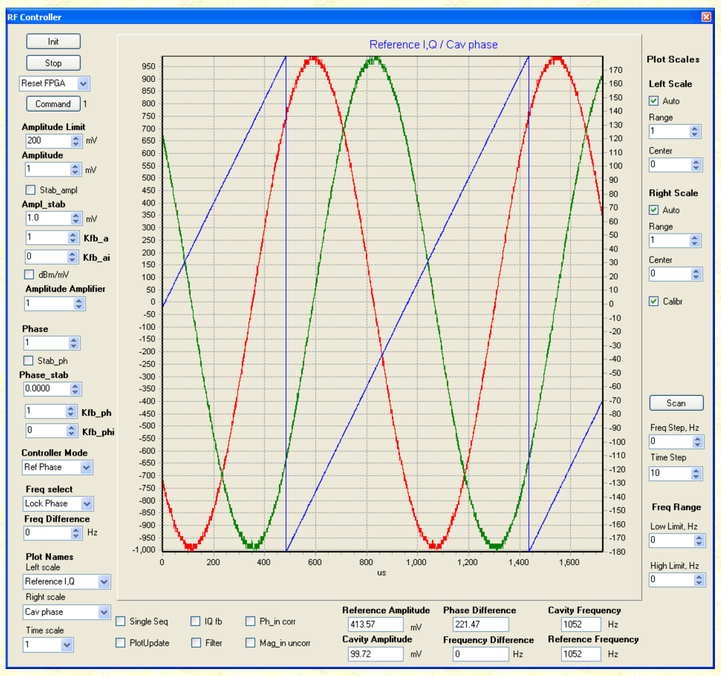


The controller is based on three boards: the analog front end for RF signal acquisition, the Bittware T2-PCI board containing DSPs and FPGA and an output board to generate the signal driving the power amplifier. The analog front-end includes five A/D channels based on the AD9433 chip. Two ADCs sample RF signals coming from the cavity pickup and from the frequency reference generator. Additional ADC channels acquire information of amplifier’s direct and reflected power and beam current, in order to extend the controller capability to accelerators with high current and beam loading effects. For each channel, an Epcos B39805 bandpass filter followed by a Mini-Circuits ERA-3 amplifier and an ADT1–1WT transformer provide the required filtering and impedance adaption for the ADC input. The output signal driving the power amplifier is generated by a DAC (AD9752) at a frequency of 16MHz; after proper filtering this signal is then upconverted to 80 MHz by mixing it with the 64 MHz clock. Clock signals to 5 ADCs, DAC, mixer and FPGA are provided by the AD9516 programmable clock distributor, placed in ADC board and featuring a channel-to-channel skew lower than 10ps. The frequency of sampling clock is 64MHz. The ADC and DAC boards are connected to the T2-PCI card through dedicated high speed I/O channels, supporting parallel data transfer from all five 12-bit ADC and to 12-bit DAC at 64 MHz rate.

FPGA PROJECT



USER INTERFACE



User Interface main functions

Setting up desired output signal amplitude and phase;
Switching on/ off amplitude and phase feedback;
Selecting feedback type between I/Q and amplitude/phase;
Tuning of feedback parameters like proportional and integral coefficients;
Tune trade-off between loop delay and signal measurement noise – by tuning digital filters;
Switching between SEL and GDR modes;
Detection of the cavity’s resonance frequency during start-up – with SEL or amplitude-frequency plot.

Diagnostic possibilities

A plot window in program can simultaneously present two different graphs taken from different stages of signal flow. Time scale range can be changed from ~1.9 ms up to ~1.3 sec. Plot curves can be updated every 2 seconds, or after a selected event to view the step response. In addition, plot can show cavity’s frequency response. Presented picture show I and Q components of reference signal (left scale) and cavity phase (right scale, in degrees).
Text windows below the plot show several parameters such as reference and cavity field amplitudes and frequency, phase difference. These data are updated at approximately 8 Hz rate. Phase and frequency difference are sent through Ethernet to cavity tuner.

TEST RESULTS

Finding cavity’s resonance frequency

First picture shows cavity’s frequency response. As we can see, reference frequency of test cavity is 300 kHz away from 80 MHz centre frequency, or ~79.7 MHz, and half-width bandwidth is ~80 kHz. Frequency sweep is initiated by pressing “Scan” button after defining frequency range and sweep rate.

Feedback tests with cavity

Two pictures on bottom line (most left and adjacent) show the phase error under environmental disturbance conditions (mechanical vibrations) either without feedback (left) and with the cavity locked (centre) when the cavity works in generator-driven mode. As we can see, average phase difference between cavity and reference in feedback mode is about 0 degrees, and the feedback successfully eliminates mechanical disturbances. It was shown that frequency locking in SEL is possible. Phase error in SEL phase feedback mode was large, about 10 degrees, because of large bandwidth of warm cavity. It is expected that phase error for superconducting cavity should be much lower. After switching to GDR mode (typical working mode), phase error reduced to 1%.

Digital filters addition

Four pictures on right side show influence of filter addition. Additional filtering is obtained by a sequence of two CIC decimation and interpolation filters with rate 256. Two upper plots show phase step responses before (green line) and after (blue) additional filters. Two down plots show phase differences between cavity and reference. Two centre pictures show plots without additional filters, two right pictures – with additional filters. As we can see, filter addition decreases phase error by about 4 times at a cost of loop delay increase: loop delay increases from ~5 to 60 us, and step response time up to 400 us. For superconducting cavities with typical filling times up to 1 second, this loop delay is more than acceptable.