A digital Base-band RF Control System*

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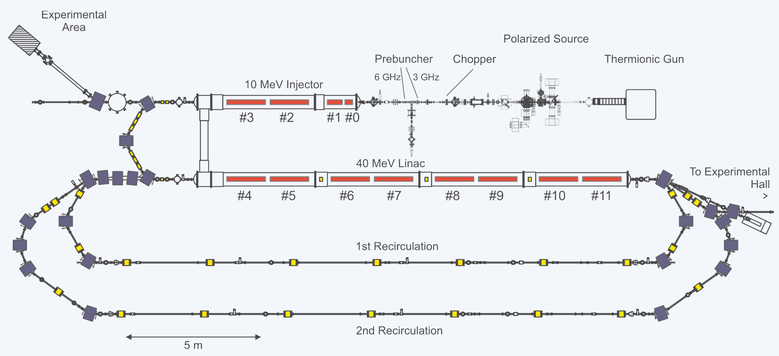
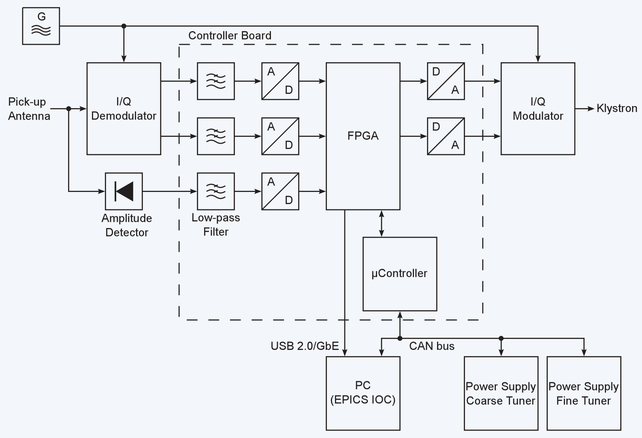


Design Energy:	130 MeV	Superconducting Cavities:	
Duty cycle:	CW	Frequency:	2.9975 GHz
Max. beam current:	60 μA	Q_L:	$3 \cdot 10^7$

Hardware

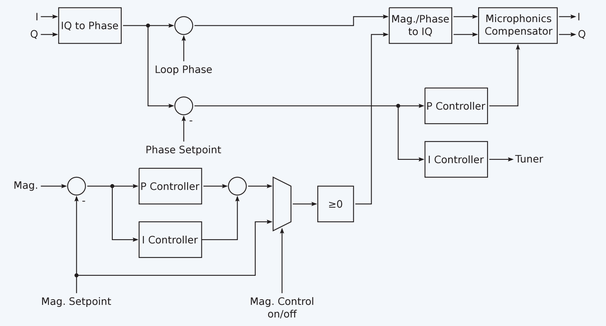
In-house developed RF and controller boards



Control Algorithm

Different control algorithms are neccessary

- Generator-Driven Resonator for normal-conducting cavities
- Self-Excited Loop for supercond. cavities (see figure)

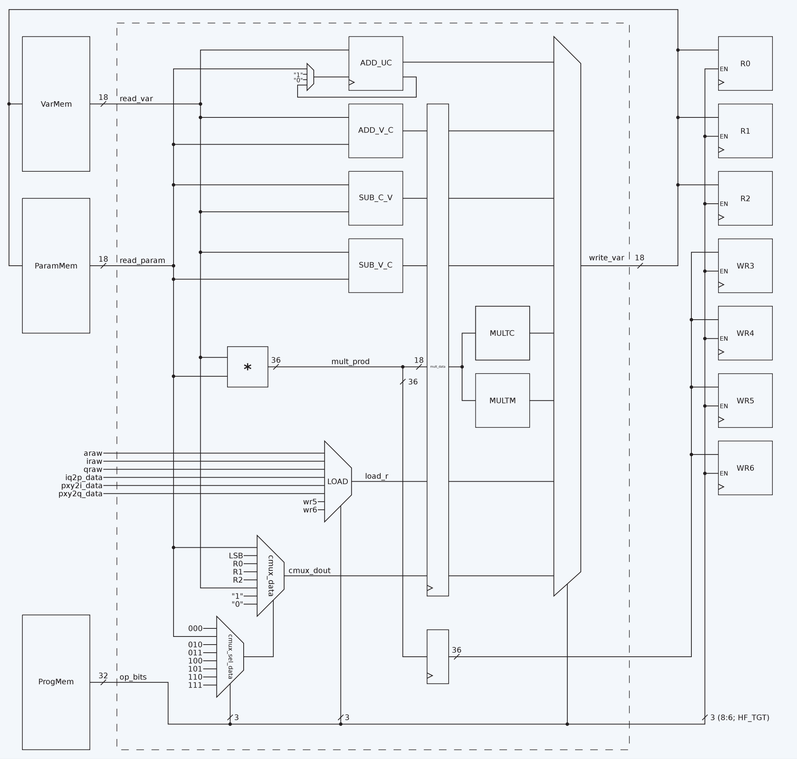


FPGA and Soft CPU

- Self-developed soft CPU implemented in the FPGA executes a program representing the control algorithm
- ALU uses 18 bit operands (full resolution of the ADCs)
- Two-staged pipeline
- CORDIC blocks transform from Cartesian coordinates to polar and back (pipelined as well)
- 36 bit accumulating registers for integral controllers
- CPU runs at 80 MHz, 1 μs latency caused by control algorithm
- Parameters are read-only for the soft CPU but read/write for the micro-controller
- Variables (intermediary results) are read/write for the soft CPU but read-only for the micro-controller

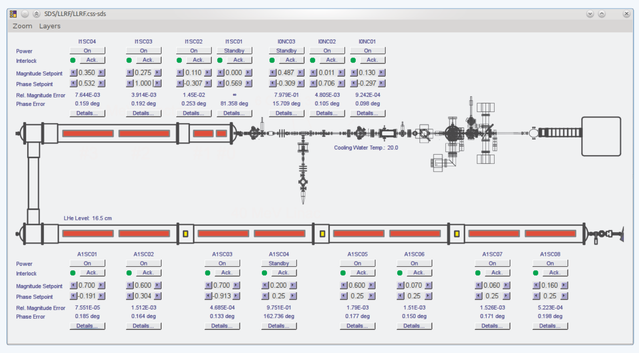
Advantages:

- All variables are stored in fixed registers (simplifies diagnostics)
- No synthesis of the Verilog code necessary after the control algorithm has been changed
- Control algorithm can be changed during operation

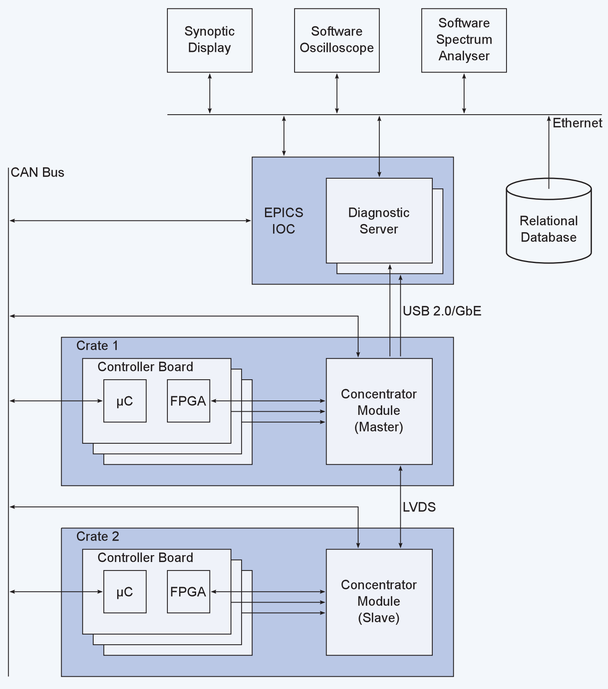


Slow Control

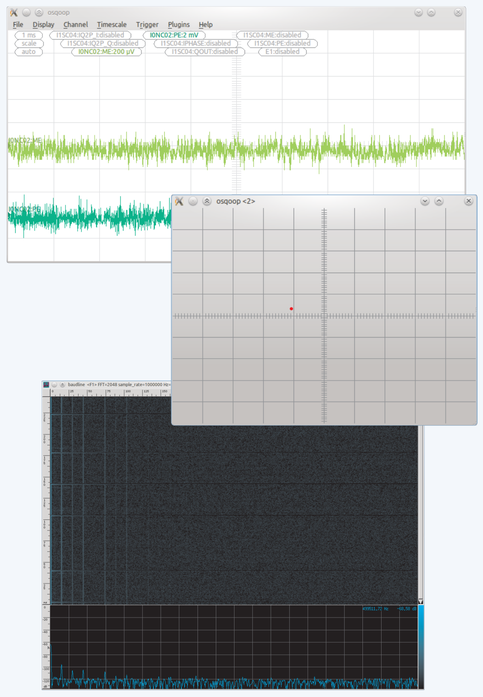
- Micro-controller runs Nut/OS
- Controller boards send commands directly to tuner power supplies
- EPICS IOC on standard PC
- Self-developed device support uses SocketCAN network stack
- Operator interface implemented with Control System Studio (Synoptic Display Studio)



Diagnostics



- Eight controller boards in one crate
- Concentrator card collects data from the controller boards and streams signals to the PC via USB 2.0
  - Eight signals with 16 bits at full sampling rate of 1 MS/s
  - Two LSBs of the full 18 bits are available as separate channels
  - All 64 signals of all 16 controller cards at a sampling rate of 2 kHz over separate USB interface
- Coupling of two crates possible for common read-out
- Data can be streamed to clients over the network
  - Software oscilloscope
  - Software spectrumanalyzer
- IOC provides mean values and online RMS errors of magnitude and phase



Deployment

- Use Debian Fully Automatic Installation to setup the PC (takes about 10 minutes)
- Update firmware and FPGA bitstream via CAN bus
- Bootloader allows firmware update even if firmware of device is broken
- FPGA multiboot functionality provides fall-back to “golden” image if primary bitstream is broken

Summary

- System has replaced old analog RF control sytem completely
- Accuracy achieved so far: mag. $7 \cdot 10^{-5}$ rms, 0.7° rms
- Soft CPU allows fast modification of the control algorithm as well as powerful diagnostics
- Highly automatized deployment allows continuous integration of improvements

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