THE MACHINE PROTECTION SYSTEM FOR THE R&D ENERGY RECOVERY LINAC*

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Abstract

The Machine Protection System (MPS) is a device-safety system that is designed to prevent damage to hardware by generating interlocks, based upon the state of input signals generated by selected sub-systems. It protects all the key machinery in the R&D Project called the Energy Recovery LINAC (ERL) against the high beam current. The MPS is capable of responding to a fault with an interlock signal within several microseconds. The ERL MPS is based on a National Instruments CompactRIO platform, and is programmed by utilizing National Instruments' development environment for a visual programming language. The system also transfers data (interlock status, time of fault, etc.) to the main server. Transferred data is integrated into the pre-existing software architecture which is accessible by the operators. This paper will provide an overview of the hardware used, its configuration and operation, as well as the software written both on the device and the server side.

INTRODUCTION

An ampere class 20 MeV superconducting Energy Recovery Linac (ERL) has been built to test concepts for high-energy electron cooling and electron-ion colliders. One of the goals is to demonstrate an electron beam with high charge per bunch (~5 nC) and extremely low normalized emittance (~5 mm-mrad) at an energy of 20 MeV. The ERL R&D program was started by the Collider Accelerator Department (C-AD) at BNL as an important stepping-stone toward a 10-fold increase of the luminosity of the Relativistic Heavy Ion Collider (RHIC). This program aims to demonstrate CW operation of an ERL with an average beam current in the range of 0.1-1 ampere, combined with very high efficiency of energy recovery [1].

The R&D ERL requires a protection system to prevent damage to hardware due to high beam current. The Machine Protection System (MPS) for the R&D ERL is designed as a device-safety system that generates interlocks based upon the state of input signals generated by select sub-systems. It exists to protect key machinery such as the 50 kW and 1 MW RF Systems. When a fault state occurs, the MPS is capable of responding with an interlock signal within several microseconds. The Machine Protection System inputs are designed to be fail-safe. In addition, all fault conditions are latched and time-stamped.

The ERL MPS is based on a National Instruments hardware platform, and is programmed by utilizing National Instruments' development environment for a visual programming language.

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HARDWARE

The MPS runs on a programmable automation controller called CompactRIO (Compact Reconfigurable Input Output). The National Instruments CompactRIO platform is an advanced embedded control and data acquisition system designed for applications that require high performance and reliability. This small sized, rugged system has an open, embedded architecture which allows developers to build custom embedded systems in a short time frame.

The National Instruments CompactRIO device that is used for the MPS is an NI cRIO 9074 (see Fig. 1). The cRIO 9074 is an 8-slot chassis with an integrated real-time processor and an FPGA. The embedded processor is a 400 MHz Freescale MPC5200 that runs the WindRiver VxWorks real-time operating system. The FPGA is a Xilinx Spartan 3 with 2 million gates (46,080 logic cells) and 720 KB embedded RAM. The cRIO 9074 also features a 256 MB nonvolatile memory. CompactRIO combines an embedded real-time processor, a high-performance FPGA and hot-swappable I/O modules to form a complete control system. Each module is connected directly to the FPGA and the FPGA is connected to the real-time processor via a high-speed PCI bus (see Fig. 2).

Figure 1: The National Instruments cRIO 9074 [2].

ERL critical sub-systems such as the RF system require the MPS to respond on a microsecond scale. High-speed I/O modules were chosen to meet the necessary timing requirements. The 24V capable module has sinking digital inputs with 7 µs response time, and the TTL module has digital inputs and outputs with 100 ns response time.

SOFTWARE

The MPS interface is written in LabVIEW (Laboratory Virtual Instrumentation Engineering Workbench).

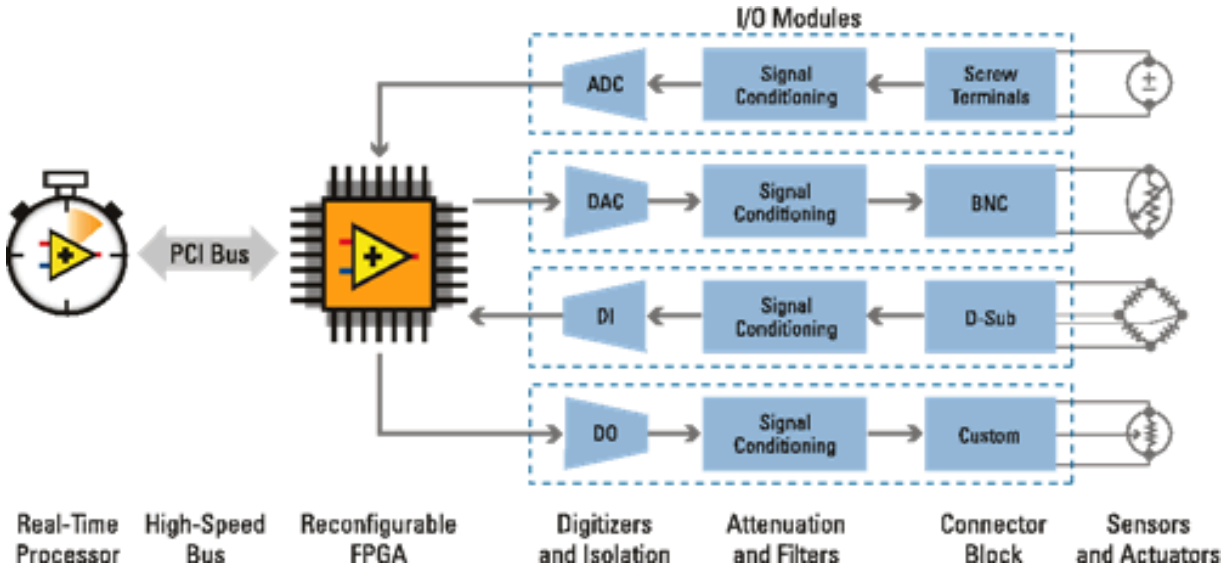

Figure 2: Block diagram showing a generic CompactRIO architecture [2].

LabVIEW is a graphical programming environment used to develop measurement, test, and control systems utilizing graphical icons and wires that resemble a flowchart. The National Instruments CompactRIO platform requires two different LabVIEW software modules corresponding to the System's interface, one for the Real-Time processor and one for the FPGA. These modules contain custom functions specific to the Real-Time processor or the FPGA in addition to all the functionalities of the standard LabVIEW module.

The code for both the Real-Time processor and the FPGA is developed on a host computer. The program for the FPGA is developed by using a standard LabVIEW software module. The LabVIEW FPGA code is then translated to VHDL code and compiled using the Xilinx tool chain. The program for the Real-Time processor is also developed by using a standard LabVIEW software module. When ready, the code for the Real-Time processor and the FPGA is downloaded to the CompactRIO device via Ethernet. Once the code is downloaded, the CompactRIO can run in a stand-alone mode, or communicate directly with a host via Ethernet.

Running directly on the CompactRIO platform, the MPS interface accepts the various input signals and generates any necessary interlocks. An interlock is generated when a logic high (fault) is seen at the input. If a cable is disconnected or broken, an internal pull-up ensures the system will generate an interlock. Exception is given to the RF sub-system which provides normally-high inputs due to equipment constraints. These inputs are inverted within the LabVIEW FPGA. If one of the continuously polled input levels change to high (indicating a fault), the fault is latched, and the time of the event is recorded using a 32-bit LabVIEW tick counter function. This provides a microsecond time stamp. The MPS interface also provides the capability to enable and disable inputs. Enabled and latched inputs are then combined and passed to other critical systems as interlocks. The input latches are cleared only after a software reset has been issued.

Operators communicate to the MPS interface using the main ERL server. Interaction with this Linux server is handled by a separate TCP server using the locally-constructed Simple Network Access Protocol (SNAP). SNAP provides remote access to the statuses of all MPS inputs and enable/disable controls for each. Additional handshake information between the server and the CompactRIO hardware across the network chain is used to monitor the overall status of the system. Commands can be sent and statuses read from the main ERL server process through a standard Collider Accelerator Department (C-AD) text-based parameter editing page that can be accessed from networked workstations or thin-clients. A web server capability is also provided by National Instruments to allow the developer to monitor and control the system remotely, avoiding interaction with the main ERL server.

EXISTING SYSTEM

The original ERL MPS was implemented and tested during the Cold Emission Test in 2009. In this configuration, the MPS had nine sub-system inputs and four outputs. As per the requirements, each sub-system provides either a TTL level or normally-open dry contact. All the inputs are latched when a fault occurs, and the fault time is recorded. This information is displayed by the MPS interface until the reset button is activated in an attempt to clear latched inputs. If the fault condition is still present, the appropriate latch maintains the interlock status. When the MPS turns on initially, the same reset button is used to establish a connection and inform the hardware that the sub-systems are ready to be monitored. This practice is utilized in order to prevent the MPS from starting prematurely in the case of a power-loss. The interface also has an indicator derived from the inputs, to

display the status of the critical sub-systems. The system response time is ~3-4 µs.

The MPS communicates with the ERL main server by sending data every 10 minutes, or every time a value changes.

PERFORMANCE

The MPS for the R&D ERL was recently used during the conditioning of the fundamental power couplers (FPC) [3]. The existing CompactRIO chassis is populated with 4 I/O modules: a 32-channel 24V capable input module, two 8-channel TTL input-output modules, and a 4-channel SPST relay output module. The layout is illustrated in Fig. 3. The inputs were expanded from nine to twenty-eight for this test. This did not require any additional I/O modules. The response time has increased to ~8 µs with the addition of the necessary logic and the defined I/O channels. This increase occurs because once more than 8 channels per module are utilized CompactRIO transitions to a byte-wide polling scheme. In other words, for up to 8 channels, the I/O is routed directly to the FPGA; when more than 8 channels are used, the I/O is transferred using a National Instruments proprietary Serial Peripheral Interface (SPI). The MPS hardware can be expanded by installing more I/O modules into the 4 remaining available slots in the CompactRIO chassis. The overall system size can also be expanded by daisy-chaining to another chassis via EtherCAT [4].

The Commercial of the Shelf (COTS) hardware-based MPS is extremely time and cost effective compared to a custom design. The initial configuration of the system took about three months and modifications for the FPC conditioning took about a week. This short development time compliments the system flexibility and expandibility, resulting in a very effective solution with minimal resource requirement. The whole system, including the software modules, cost about US ~$5,000.

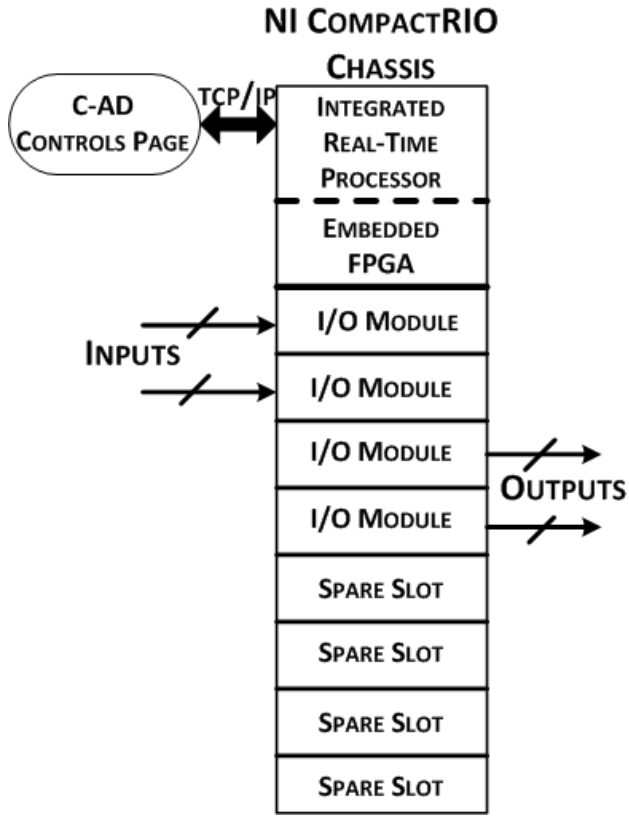

Figure 3: Block diagram for the current layout.

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[2] Image is courtesy of National Instruments.
[3] W. Xu et al., "FPC Conditioning Cart at BNL", PAC'11, New York, March 2011.
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