

AUTOMATIC ANALYSIS AT THE COMMISSIONING OF THE LHC SUPERCONDUCTING ELECTRICAL CIRCUITS

H. Reymond, O. O. Andreassen, C. Charrondiere, A. Rijllart, M. Zerlauth, CERN, Geneva, Switzerland

Abstract

Since the beginning of 2010 the LHC has been operating in a routinely manner, starting with a commissioning phase and then an operation for physics phase. The commissioning of the superconducting electrical circuits requires rigorous test procedures before entering into operation. To maximize the beam operation time of the LHC, these tests should be done as fast as procedures allow. A full commissioning need 12000 tests and is required after circuits have been warmed above liquid nitrogen temperature. Below this temperature, after an end of year break of two months, commissioning needs about 6000 tests. As the manual analysis of the tests takes a major part of the commissioning time, we automated existing analysis tools. We present here how these LabVIEW™ applications were automated, the evaluation of the gain in commissioning time and reduction of experts on night shift observed during the LHC hardware commissioning campaign of 2011 compared to 2010. We end with an outlook at what can be further optimized.

INTRODUCTION

The first LHC Hardware Commissioning Campaign (HCC) was started early 2008. The aim of this crucial phase, mandatory before to put the accelerator into operation, was to test in real conditions all the equipment and systems of the machine. It included protection systems and all the superconducting electrical circuits.

For this purpose, two types of tools were developed [1], one to manage the execution of the tests and a second to provide data analysis, to deal with the big amount data from the tests. The initial approach used when designing these analysis tools, was to help the users to perform manual analysis of the data with a tool that permitted to select a test result set, automatically load interesting signals and display them in a GUI that could easily be used by experts from several domains.

During the HCC, human and time resources have been optimized. Less people were available for the LHC start-up tests therefore to speed up the tests, the framework and the applications have been improved to permit execution of tests in parallel on several circuits. Furthermore, with the increased electrical circuit's knowledge, it has been possible to set limits to measured and calculated parameters, which led to automate part of the analysis.

SYSTEM OVERVIEW

The Electrical Circuit Commissioning (ECC) consisted of a series of tests to provoke a reaction of all interlock and protection systems. Different current cycles

(see Fig.1) were applied on these circuits to validate them, up to nominal current.

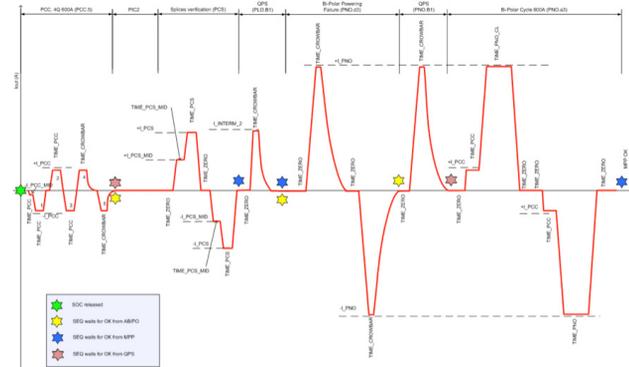


Figure 1: Current cycles for 600A circuit validation.

Each reaction of a protection system generated a so-called “Post Mortem” file, in which the most important parameters were stored in a circular buffer with time stamped data. These files were then collected and archived to be later analysed using the Post Mortem Analysis tools.

The Post Mortem Analysis System

The Post Mortem framework is made of three main systems [2]. The *Sequencer* application edits test cycles and sends commands to the power converters. The *Post Mortem Request Handler* (PMRH) collects the data files from the involved equipment and associates them to the test parameters sent by the *Sequencer*. The *Post Mortem Event Analyser* (PMEA) provides a GUI for experts to easily retrieve and analyse a test.

Several GUIs have been built to present data of specific tests. They display the executed current cycle, the values returned by the involved equipment and the calculated values (ramp, min-max, delays, resistances...).

Principle of Validation of an Electrical Circuit

The validation of an electrical circuit is performed as follows: From the sequencer, an operator selects the circuit to be tested and attributes a series of test steps to be performed, depending on the circuit type (nominal current and specific limits). Automated checks are made to verify that the circuit is available and not blocked by interlocks. When all conditions are met, the sequencer generates and sends commands to the power converter of the related circuit.

During the current cycle execution, the protection equipment reacts and generates post mortem files. These files are collected by the PMRH, from all systems in the

interlock and protection chain of the circuit. Their data are merged into one event. Then all available events are presented in the PMEA GUI. It gives an overview of the executed tests that are waiting for analysis, but also those already verified.

To validate a test step of a circuit, the event generated must be analysed and signed by experts of all involved domains (interlock system, powering, quench protection, cryo). When all the experts have signed and accepted the analysis results, this information is returned to the *Sequencer*. This allows the system to launch the next test step. In case of rejection of one analysis, the circuit powering is blocked.



Figure 2: High Voltage qualification in the LHC tunnel.

Then the problem must be investigated and solved before a new test sequence is launched. This could mean an intervention in the LHC tunnel (see Fig. 2) to make on site measurements to understand the facts, replacement of some parts in case of device failure or sometimes loading a new firmware release into an electronic system.

Each tunnel intervention must be scheduled and well organized to optimize the time and the work of the involved teams.

LHC Circuits Layout

The LHC circuits are divided into eight independent sectors. Each circuit can supply one or many magnets, depending of the circuit type. For example, one 13kA power converter drives 154 dipole magnets. There is a large range of different circuits, with currents of 60A, 80A, 120A, 600A, 6kA, 8kA and 13kA. These circuits power all the main dipoles and quadrupoles and their respective correctors, such as sextupoles, octupoles, decapoles and dodecapoles.

ELECTRICAL CIRCUIT COMMISSIONING EVOLUTION

Almost all of the test management and analysis tools used today have been developed for the first complete Hardware Commissioning of the machine in 2008. Many improvements were made during the next campaigns,

thanks to the experience gained. But also an effort to enhance the efficiency was conducted in order to minimize the testing phases, with the objective to increase the time dedicated to physics.

In the early age of the ECC, the sequencer could only manage one test at a time. It was then modified [3] so that it can run tests on various circuits in parallel. Introducing this feature in the test sequences was possible due to the sectorisation, but also by the large range of circuit types.

To meet this challenge we instantiated some parts of the PMRH code, used for collecting the PM files. As the PMRH, the PMEA and all analysis tools were developed with LabVIEW™; it was easy to introduce VI templates, and then call them as a clone when needed. From the analysis framework point of view, introducing parallelism in the tests was transparent.

Taking into account the Human Factor

At that stage the experts, started to be drowned in hundreds of events per day; to analyse and sign. In effect, without counting the selection tools for viewing the tests and those dedicated to the display of data as curves with pre-loaded signals, it took about 3 minutes to analyze a test. With an average of 300 tests per day to achieve the objectives, 15h in front of the screen were necessary, to check similar plot and table results. As the slightest variation could have an enormous importance in terms of reliability and safety of the machine.

As for any major achievements, taking or not into consideration the human factors that may be crucial for the success of the project. In the case of ECC, for many technical fields, the same experts who participated in the design and installation of the system then participated in validation tests, and sometimes also applying hardware corrections and compliance. It is not difficult to understand that whatever the motivation and professional commitment of the person who analyzes, his acuity and assessment will not be the same between the first and the 200th analysis. So, even by applying the same criterias, the first bad events will be surely rejected, but later could be accepted as near to the limits.

Introducing Automated Analysis

To overcome the problem of the number of tests to be signed by the experts, it was decided to automate some analysis. This was made possible from the ECC 2009, using the knowledge acquired from the previous campaign. Hence some acceptance ranges and even more restrictive criterias could be defined to specify automatic analysis algorithms for some particular circuits.

The first tool fitted with automated analysis was the Powering Interlock Controller (PIC) [4]. Originally it was dedicated to verify delays and status of digital signals, coming from the interlock system. The role of the expert being to check some patterns and signals synchronisation, according to various parameters, such as circuit type, test type and protection equipment present in the interlock loop.

Several Sources of Improvement

Since the 2010 ECC, new valuable features have been integrated in the PMA framework: automated analysis, accepted tests results directly sent to the MTF (Manufacturing and Test Folder repository of the related circuit). This gives a full traceability of circuit behaviour, without possible error due to human input. On the other side, for failed tests, a non-conformity report is generated and forwarded to the dedicated management tool. This gives to the expert in charge an overview of the encountered defects, but also a trace of what has to be fixed, reducing the risk of missing one issue.

The time saved thanks to the signature test automation, freed the experts for critical tasks such as monitoring the repair of problems. This also allowed reducing the number of persons involved in the test execution.

The change in the organization of the tests [5] has been an important contribution too. The availability of night shifts launching a large amount of sequences of tests during the night, on all sectors in parallel gives the field workers the opportunity to organize and fix problems on non-compliant systems the following day.

CONCLUSION AND PERSPECTIVES

The Electrical Circuit Commissioning of the LHC is now a well-defined and documented exercise fitted with powerful procedures and software.

The automated analysis and results signing have proven their utility and efficiency. Reducing the time devoted to this task, helped to reorganize the experts' responsibilities and to decrease the number of people implicated.

A big effort has been done to take into account the human factor, when developing the analysis framework. Some improvements have still to be done, for user training, as specification of the tools are not directly written by future users, lots of practical features and useful tips included in the tools are unknown to them.

Most of the electrical circuits have been qualified to 3.5 TeV operation. During the next 2013 long shutdown, their qualification to 7 TeV (i.e. nominal magnet current) will require extended sequences of tests. Here again, fully automated analysis tools will be a key point for an efficient ECC execution. The future LHC operation needs more powerful applications to study complex conditions and machine interaction. They will help operators to overcome difficult behaviour and to get a forecast about equipment and systems status.

REFERENCES

- [1] M. Zerlauth et al, "The LHC Post Mortem Analysis Framework", ICALEPCS 2009, Kobe, Japan.
- [2] O. O. Andreassen, "Post Mortem for the LHC", EN/ICE Workshop on Post Mortem, 2009, CERN, Switzerland.
- [3] B. Bellesia et al, "Optimisation of the Powering Tests of the LHC Superconducting Circuits", PAC09, Vancouver, Canada.
- [4] M. Zerlauth, R. Schmidt, J. Wenninger, "Commissioning and Operation of the LHC Machine Protection System", HB2010, Morschach, Switzerland.
- [5] M. Solfaroli, "Scope and Results of Hardware Commissioning to 3.5 TeV and Lessons Learnt", Chamonix 2010 Workshop, Chamonix, France.