ALBA TIMING SYSTEM - A KNOWN ARCHITECTURE WITH FAST INTERLOCK SYSTEM UPGRADE

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Abstract

Like most of the newest synchrotron facilities the ALBA Timing System works on event based architecture. Its main particularity is that integrated with the Timing system a Fast Interlock System has been implemented which allows for an automated and synchronous reaction time from any-to-any point of the machine faster than 5µs. The list of benefits of combining both systems is large: very high flexibility, reuse of the timing actuators, direct synchronous output in different points of the machine reacting to an interlock, implementation of the Fast Interlock with very low cost increase as the timing optic fiber network is reused or the possibility of combined diagnostic tools implementation for triggers and interlocks. To enhance this last point a global timestamp of 8ns accuracy that could be used both for triggers and interlocks has been implemented. The system has been designed, installed and extensively used during the Storage Ring commissioning with very good results.

INTRODUCTION

Alba [1] is a synchrotron light source under installation located nearby Barcelona. This 3 GeV third generation light source is planned to deliver the first X-rays beam to the users in 2012. The Linac has been commissioned in 2008, the booster in 2010 and the Storage Ring in 2011. The seven Beamlines included in the “Phase One” are being commissioned at the end of 2011.

The timing system is one of the critical systems in a synchrotron. Its main function is to synchronize the operation of the different parts of the accelerator. Including the injection procedure (Linac, Booster and Storage Ring) and the diagnostic devices.

When the Alba project started the initial triggering specifications were fixed by Accelerators Division. The main request was being able to generate triggers synchronously with the RF master frequency (499.654MHz in Alba case) in different points of the machine with a very low jitter (bellow 100ps), and to adjust the delay of some triggers in steps lower than 16ns.

Reviewing the state of the art of the timing systems developed in similar facilities it was found that two main approaches had been adopted historically: signal based model and event based model.

In the signal based architecture one reference frequency is downsampled to generate some trigger pulses that finally are distributed and delayed at each one of the destination points where it is needed to produce a trigger.

In the event based model the transmission is not of different pulses (or train of pulses) but of a code which is generated synchronously to a master frequency and transmitted following a typical start topology to all the points where the trigger output has to be produced. At each one of these points the continuous stream of these codes is decoded and a trigger pulse with an adjustable delay is generated if needed. One of the main difference between both approaches is that in the event based case all triggering information reach all the points of the facility. That involves full flexibility to change trigger parameters (as the decodification is remotely controlled) and a much easier maintenance. This is the main reason why all the newest synchrotrons have followed this architecture lately.

At some point other requirements were needed by Accelerators division about some trigger and fast interlock systems needs. The request could be divided to have two independent main characteristics: being able to produce synchronous outputs in different points of the machine and being able to react very fast to an interlock.

The idea of combining all those systems in a unique one which could give the maximum possible flexibility and performance came up. This paper explains how this system was defined as an upgrade of the Event based architecture and the process that was followed to implement and commission it.

STANDARD ARCHITECTURE

To establish a common framework a brief description of the different elements in the event based timing architecture will be done (please refer to Figure 1).

The first element is a device that generates the codified event stream (from now called EVG) synchronous to the RF frequency. In the case of Alba, it was also requested being able to generate events synchronous to a external 50Hz signal. The aim was being able to produce triggers synchronous to the AC 220V 50Hz power to minimize any possible effect in the ripple voltage of the power supplies for some specific triggers.

The event stream generated with the EVG is distributed following typical tree architecture to all the points where the trigger needs to be generated. To spread the signals there are some units called Fan Outs that produces multiple identical stream outputs from one event stream input.

Finally in the different destination points there are elements called Event Receivers (EVR from now) that decodes the stream. If some predefined event codes are received the trigger output with some preprogrammed characteristics (delay, pulse width, etc…) will be executed. The outputs will be synchronous to the event stream input and therefore to the master RF frequency in all the facility.

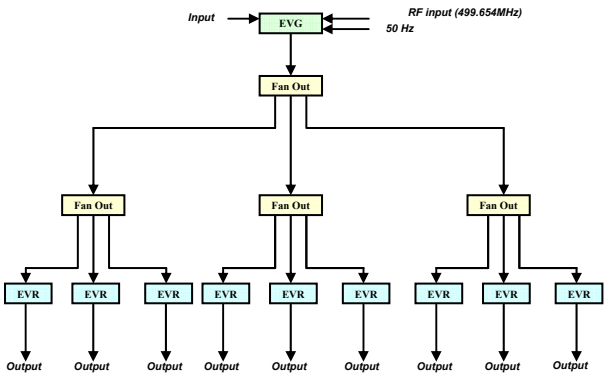

Figure 1:Event based timing architecture.

At Alba two different tenders were published: the first one included the electronics boards based in cPCI standard that were needed for each module (EVG, Fan Outs and EVRs). Among the bidders offers the contract was awarded to Micro-Research Finland Oy [2].

And in the second tender the optic fibers used for the timing network were included. More than 10Km of OM3 cable with 4 fibers were requested with a very low dispersion in the optic fibers length to avoid thermal effects in the delay change and also to minimize the delay adjustment procedure in the facility. The contract was awarded to Reichle & De-Massari (R&M)[3].

For very specific cases a delay adjustment within the bunch time was needed to be generated (in Alba case 2ns): Linac gun trigger, an streak camera used for diagnostic purposes and in the booster kickers magnets. For these cases a special product was requested to MRF which provided a special 6U cPCI card allowing delay adjustment of 10ps steps (EVRTG-300).

FAST INTERLOCK ARCHITECTURE

General Layout

When other triggering specification needs arose which could not be fulfilled with the Alba Equipment Protection System [4], as the capability to react synchronously to an interlock in different points in the machine or to react to an interlock in the sub miliseconds range, different approaches about how to fulfill such needs were considered.

The timing system already offered a platform to produce synchronous outputs and also the transmission of the triggers was fast enough. Moreover the timing network already covered more than 80 different points all over the accelerator. Therefore the idea of upgrading the timing system implementing a bidirectional communication link was considered as the best possible option.

Also there were different factors that reinforced following such direction: the first one was the high flexibility that this architecture would involve, the second was that the diagnostic tools of events timestamp that already were going to be implemented in the timing system could also be used for interlocks diagnostics. Doing in this way the timing diagnostic tools could become a very powerful tool to be used as it will be described later.

Finally from the cost point of view it appeared as a very good solution as the timing network was composed by four fiber cables (following a market "de facto" standard) which only one was used at that time.

Therefore the objective was being able to generate an independent event stream from the EVRs towards the EVG using the same timing protocol. That stream of events would be needed to be multiplexed in a new unit called “Fan Out Concentrator” which would become one of the main parts of this new architecture as it was needed to manage collision or saturation scenarios. Finally the interlock event stream would arrive to the EVG that would introduce the event in the normal timing event flow so the interlock could arrive to all the points of the machine following the same path as the rest of triggers generated by the EVG. Please refer to Figure 2 for a simplified architecture diagram.

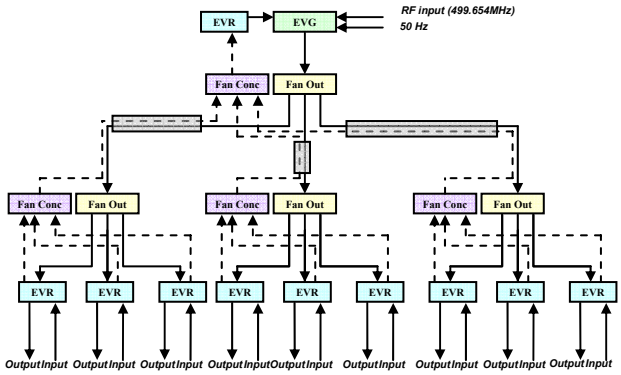

Figure 2: Fast Interlock System architecture.

To generate this system, MRF was contacted and a collaboration agreement was achieved that lead us to a new EVR firmware with all the capabilities implemented and with the development of a new unit by MRF: the Fan-Out Concentrator (cPCI-FCT-8).

Response Time

In a typical timing system the delay between the trigger generation at the EVG and its distribution to the EVR is not an important issue as far as all the triggers outputs are delivered synchronously. But if the timing system is required to react to interlocks it is needed to characterize the response time of the system.

In the hardware implementation we are using the codification/decodification process of the events uses 30 event clock cycles. In the case of Alba is 125MHz that is lead us a total is 240ns. So taking into account the number of stages present in Alba.

$$\text{time} \approx 240\ \text{ns} \times 7\ \text{stages} + 5\ {}^{\text{ns}}\!/_{\text{m}} \times 500\ \text{m} \sim 4.2\ \mu\text{s}$$

To understand the real magnitude of this number it has to be considered that the interlock propagation from any-to-any part to the machine and production of a reaction is a value closer to 4µs where 60% of the time is used just for signal propagation over the optic fiber. So no big margin for speed propagation improvement seems to exist for the future.

Timestamp

Each EVR has an internal time reference. In the case that a predefined event is received a timestamp log is possible to be acquired. This feature that is useful for triggering information it is still more interesting when interlock information can be acquired with common time reference being possible to match triggering effects and interlocks.

The same timing network is used to distribute the global clock reference to all EVRs. The system is based in a in a GPS receiver with a built in OCXO oscillator that provides PPS with an accuracy higher than ±100ns. Once this pulse is generated a reset for the seconds counter is sent via an event by the EVG. Everytime the reset is produced in a EVR an internal counter of 125MHz clock with accuracy higher than 40ppm is restarted.

For managing the PPS distribution and transmitting the UTC 32 bit seconds value an in-house electronic module was developed at Alba: the NTP Timestamp Server.

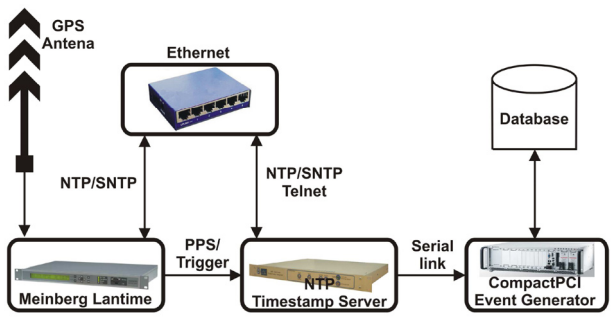

Figure 3: Global time reference distribution.

In the end at each EVR is available a timestamp of UTC time in seconds plus 8ns accuracy. So any event or interlock can be timestamped with 8ns accuracy.

APPLICATIONS

In this section a brief description of the practical applications where the Fast Interlock system has been used is presented.

RF Plants Fast Interlock

In total there are seven RF plants at Alba; six in the Storage Ring and one in the Booster. It has been developed in-house an electronic module that centralizes the safety conditions under which each one of the plants can operate (Figure 4). If those conditions are not fulfilled the plant is stopped locally and a different Fast Interlock event for each plant is generated. That event will execute in less than 5 µs all preprogrammed diagnostic and safety actions.

The unit can detect interlocks from three different RF detectors, 8 independent Arc detectors, one timing input (link to the Fast Interlock System) and a dry contact (normally used for slow signals as vacuum loss scenario detection). The reaction time is of 175ns with 5ns jitter and everything is fully programmable from its 10/100 Base-T Ethernet Port.

Internally an Alarm Log Engine has been implemented acquiring a maximum of 512 alarms sequences with 20ns timestamp that can be correlated with the global timestamp of the machine.

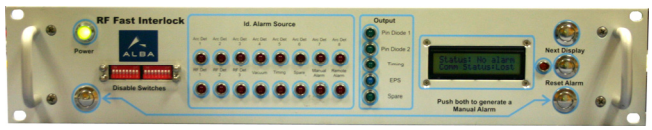

Figure 4: RF Fast Interlock Module.

BPM Fast Interlock

Alba has in total 176 BPM distributed around the 16 sectors of the Booster and the Storage Ring. Each one of the BPM is acquiring the X and Y orbit continuously. In case of an eventual distortion of the orbit outside certain predefined limits an interlock is generated.

In case that an BPM interlock is detected a Fast Interlock event is generated and will produce an immediate stop of the RF Plants and a distribution of a Post Mortem trigger to the rest of BPMs for acquiring a synchronous snapshot of the orbit. It has been defined 32 different fast interlock events: one for each one of the sectors of the SR and the booster. Doing in this way it can be easily identified the first sector where the orbit was disturbed which is a useful information for the Diagnostic group.

In the next figure a complete sequence of one BPM interlock timestamped with the Fast Interlock System is shown. A orbit interlock is detected in one BPM in SR in sector 13 and timestamped. The Fast Interlock system induces a shutdown of the six RF Plants 4µs later and that leads to a loss of the orbit in the rest of BPM sectors after 290µs.

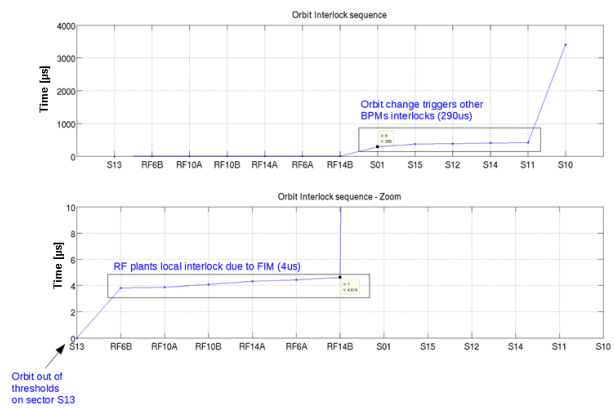

Figure 5: Orbit interlock sequence.

Front Ends

An independent Fast Interlock event has been defined for each Front End. In case of a vacuum loss scenario the RF plants will be automatically stopped to minimize the quantity of beam time that the vacuum gauges that closes had to absorb and to timestamp the beam loss.

CONCLUSION

In this paper a new architecture for the timing system has been proposed as an upgrade of the typical event based architecture that allows for fast interlock system implementation.

Several years have been needed since the initial idea came up until all the system has been developed, implemented, tested and commissioned. Currently the system has been working without problems for more than one year giving excellent service to Accelerator Division for the machine operation and completely integrated in the Control System (please refer to [5] for detailed information as it has been decided to detail the software implementation in an independent document).

Among the list of benefits one would highlight its very fast reaction time achieved that currently seems difficult to improve as 60% is spent in the transmission of the signal over optic fibers, the extremely high flexibility and reconfigurability, easy maintenance, its relatively low cost and the global combined timestamp tool that can be used both for triggers and interlocks using a common time reference.

CONTRIBUTION

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