NSLS-II BOOSTER POWER SUPPLIES CONTROL

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Abstract

A special set of devices was developed at BNL for the NSLS-II magnetic system Power Supplies (PSs) control [1]: Power Supply Controller (PSC) and Power Supply Interface (PSI). PSI is placed close to current regulators and is connected to the PSC via fiber-optic 50 Mbps data link. PSC communicates with EPICS IOC (Input/Output Controller) through a 100 Mbps Ethernet port. The main function of IOC includes ramp curve upload, ADC waveforms data download, and various process variables control. The 256 Mb DDR2 memory on PSC provides storage for up to 16 ramping tables for both DAC channels, and a 20-second waveform record for all ADC channels. The 100 Mbps Ethernet port enables real time display for 4 ADC waveforms.

The NSLS-II booster PSs are divided into two groups: ramping PSs, which provide passage of the beam during the beam ramp in the booster from 200 MeV up to 3 GeV in 300 ms time interval, and pulsed PSs, which provide beam injection from the linac and extraction to the Storage Ring.

This paper describes a project of the NSLS-II booster PSs control. Characteristic features for the ramping magnets control and pulsed magnets control in a double-injection mode of operation are considered in the paper.

INTRODUCTION

NSLS-II 3rd generation light source [2] is currently being constructed at Brookhaven National Laboratory, USA. It will be a storage ring operating at 3 GeV. To provide an effective continuous operation of the storage ring a full-energy booster [3] is proposed. The booster will accelerate electron beam from 200 MeV to the nominal energy with average beam current of 20 mA. The booster will be capable of multi-bunch and single bunch operation. Maximal number of bunches in one accelerated train is 150.

Two modes of the booster operation are planned: 1 Hz cycle with two beam injections with a 100-ms interval and 2 Hz cycle with one beam injection. The energy ramp period is 300 ms in both modes.

The required relative accuracy of the main PSs (dipoles, quadrupoles) control is 10^{-4} for the current plateaus (at beam injection and extraction) and 10^{-3} for the ramp.

Power supply control system will provide beam passing in the booster during acceleration. It will synchronously control all magnetic elements for this purpose. Also it will provide operations on orbit correction at any moment of injection, acceleration and extraction, tune and chromaticity adjustment at any moment of beam existence in the booster, response matrixes measurements, and power supplies and magnet parameters monitoring.

Power supply control should be synchronous with other accelerator subsystems to perform its functions. The synchronization is done through timing system [4]. The PS control equipment receives a trigger pulse from the timing system and uses 10 kHz signal from Event Receivers, which is synchronous to the main RF oscillator. This synchro signal allows providing the required relative accuracy of PSs at the ramp.

BOOSTER POWER SUPPLIES OPERATION

Two modes of operation are supposed for the booster: a one-second cycle with double injection with a 100-ms interval, and a 0.5-second cycle with single injection. Beam ramp time is the same for both cases: 300 milliseconds. Typical current diagrams for different PSs are provided in Fig.1.

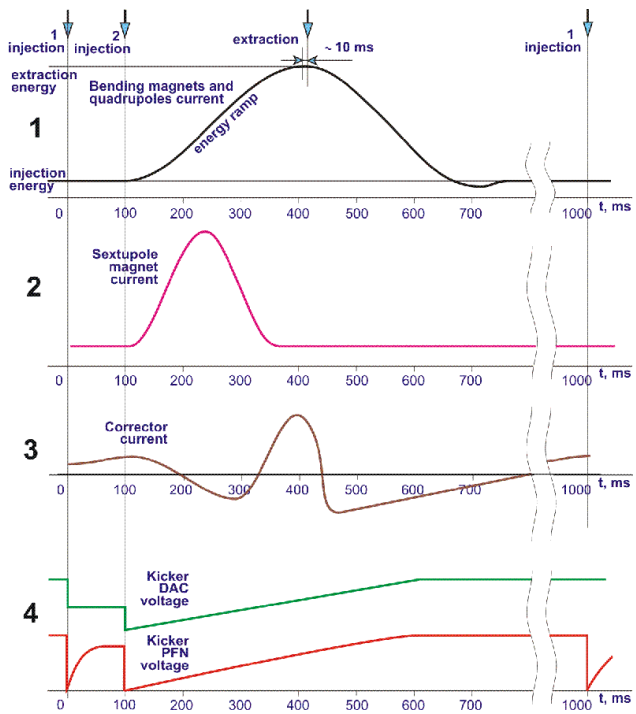

Figure 1: Booster elements current and voltage diagrams.

Diagram #1 shows change of bending magnet current in accordance with change of the beam energy. Depth on the plot in the region of 700 msec represents closure of magnetic loop for the dipole magnets.

Diagram #2 represents sextupole current compensating chromaticity deviation due to eddy current and magnet saturation effects.

Diagram #3 shows bipolar change of corrector current. The corrector ramp function should be changed in real

time at each booster cycle to provide an effective beam orbit correction.

Diagram #4 represents control and measuring signals for the injection kicker. Use of PSC allows change of DAC voltage during 100-ms interval synchronously with beam injections in hardware.

BOOSTER POWER SUPPLIES CONTROL STRUCTURE

There are 58 ramping PSs: 3 PSs for 3 groups of dipole magnets, 3 PSs for 3 groups of quadrupole magnets, 16 sextupole PSs, and 36 PSs for corrector magnets. Beam injection and extraction are provided by 9 pulsed PSs (injection and extraction septums, extraction bump magnets, 4 injection and 2 extraction kickers) and one DC extraction septum PS.

44 sets of PSC-PSI are proposed to be used for PSs control: 6 dual-channel sets for bending magnets and quadrupoles, 28 dual-channel sets for sextupoles and correctors, 10 single-channel sets for injection/extraction magnets. All devices will be placed in racks in the injection service area near the booster tunnel. A block-diagram of the booster power supply control is presented in Fig.2.

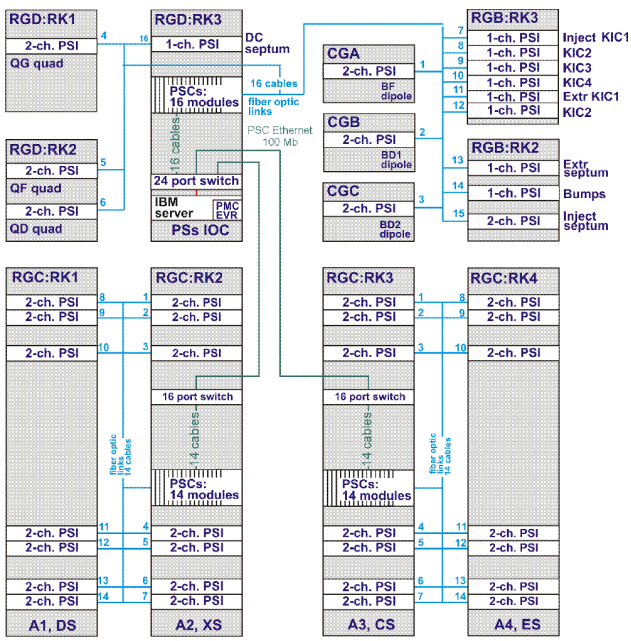

Figure 2: Block-diagram of the booster power supplies control. Distribution of the equipment among the racks.

It is supposed to use one IBM server (PSs IOC) to control all booster PSs. All PSCs will be distributed in three chassis and will be connected via switches in 1 Gbps network. .To maximize the communication speed, each PSC is directly connected to IOC via the Ethernet port. This will be the same for NSLS-II storage ring power supply control [1].

Ethernet interface of PSC is 100 Mbps, but it can only receive less than 13-14 kbyte ramping data per second due to the limit of FPGA softcore CPU, softcore MAC and a free light weight TCP/IP stack.

PSC-PSI DESCRIPTION

Main Parameters

PSI has one or two precision 20-bit DACs, three channels of precision 16-bit ADC for each DAC, six channels of 16-bit ADC for each DAC, sixteen digital inputs, 8 digital outputs. PSI is connected to PSC via fiber-optic 50 Mbps data link.

PSC is equipped with 256 Mb DDR2 memory, which provides sixteen 40 kb ramp tables for each ADC channel and a 20-second waveform record for all ADC channels. PSC has a 100 Mbps Ethernet port for connection with control system.

Operation Description

PSC version described in this paper is designed for the booster control. It has a short set of commands for interaction with high level applications:

- "Rst" resets all PCS registers to the initial state.
- "Enbl" is used for PSC disabling/enabling.
- "RampEnbl" is used for disabling/enabling of ramping mode.
- "BrkCmd#" breaks current ramp table processing and brings DAC# at "BrkRate#" (see below) rate to "BrkEnd#" state.

To provide a flexible operation PSC has the following set of setting parameters:

- "Mode" switches mode of PSC operation: Stop/Ramping Mode/Static Mode. Static mode is used for control of DC PS in the case when a transient process in PS due to a new DAC set is unimportant.
- "DoutMode" switches digital output mode: Static (level)/Pulse. Digital output pulse mode allows setting digital output to "High" level for specified time, then the level will be returned back to "Low" value.
- "DoutPlsWdt" - pulse width (ms) in digital pulse mode.
- "ClkSrc" - updates clock source: external (from backplane)/internal 10 kHz.
- "ClkDivd" - clock divider factor (0 - /1; 1 - /2; …. 254 - /255) for changing of the ramp time.
- "ActvTbl#" selects DAC# active ramping table (0-15 for DAC1, 16-31 for DAC2).
- "InActvTbl#" selects inactive ramping table for download.
- "BrkRate#" sets DAC# break rate.
- "BrkEnd#" sets DAC# break end setpoint.
- "AdcID#" selects ADC channel for #-waveform reading.

Also a set of indication parameters can be read from PSC:

- "PscLoadingRamp" - PSC ramping table download indication (Loading or Done).

- "PscFrountT" - PSC main board temperature.
- "PscRearT" - PSC rear board temperature.
- "PscIP" - last byte of PSC IP address (192.168.1.x).
- "PscDDR2Check" - DDR2 memory check during bootloading (Good/Failed).
- "PscFiberSd" - status of fiber link between PSC/PSI (Good/Failed).

PSC firmware provides reading/writing of the following values:

- Writing eight values of digital outputs and two DAC setpoints (DAC setpoints are used for static mode of operation).
- Uploading from IOC selected (determined by "InActvTbl#") ramping table of 40 kbyte data for ramping mode of operation.
- Reading sixteen digital inputs and eighteen ADC values.
- Downloading to IOC of two 10 kHz ADC waveforms selected from ADC1-ADC16 in real time.
- Downloading to IOC of two 1 kHz ADC waveforms for both DACs in real time. The order of ADC channels in the waveforms: ADC1,2,3,4,5,6,7,8,17 for DAC1 and ADC9,10,11,12,13,14,15,16,18 for DAC2. Each ADC has 1280 points in the waveform.

PSI is capable of detecting the status change sequence of digital inputs with a 10 ns resolution.

The ramping mode of operation will be used for all booster PSs: both for ramping PSs, and for pulsed/DC PSs. In the case of DC PS (for example, DC septum) the ramp table will be filled by one setting value.

In each cycle each PSC starts processing of ramping function downloaded from IOC by common trigger from the timing system. Also each PSC receives 10 kHz clocks from EVR in order to provide mutual synchronization.

SOFTWARE

Software interface for interaction with PSC (see Fig. 3) is based on EPICS.

Figure 3: EDM screen for testing of PSC/PSI.

At the moment an EPICS driver for PSC is developed and all process variables are implemented, EDM screen is prepared for testing of all PSC/PSI signals and commands.

It is supposed to use this screen for the first tests of the booster PSs at the test stand in BINP. Additional scripts for uploading of ramp tables from text or MATLAB files will be used.

A Ramp Manager (RM) application for operation with PSs during commissioning of the booster is being developed now. RM will provide edition of ramp function tables, synchronization of different PSs tables, generation of ramp function tables and uploading it to IOC, storing/restoring tables, visualization of ramp functions and measured waveforms. An example of RM python screen is presented in Fig.4.

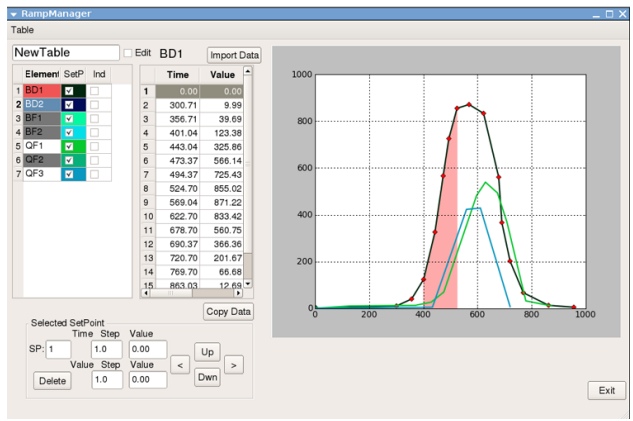

Figure 4: Ramp Manager screen.

SUMMARY

The detailed design of the NSLS-II booster PSs control is finished and all requirements are satisfied. Specifications for operation logic and parameters of Power Supply Controller and Power Supply Interfaces are worked out and are implemented in the firmware. Software is under development, its completion is planned before the start of the booster commissioning in October, 2012.

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