A NEW FAST TRIGGERLESS ACQUISITION SYSTEM FOR LARGE DETECTOR ARRAYS

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Abstract

Presently a common characteristic trend in low and medium energy nuclear physics is to develop complex detector systems to form multi-detector arrays. The main objective of such an elaborated set-up is to obtain comprehensive information about all reactions. State-of-art γ-ray spectroscopy requires nowadays the use of large arrays of high purity Ge detectors (HPGe) often coupled with anti-Compton active shielding to reduce the ambient background. In view of this complexity, the front-end electronics must provide precise information about amplitude, time, detection position and possibly pulse shape. The large multiplicity of the detection system requires the capability to process the multitude of signals from many detectors, fast processing and very high throughput of more than 10^6 data words/sec. The possibility of handling such a complex system using traditional analogue electronics has shown rapidly its limitation due, first of all, to the non negligible cost per channel and, moreover, to the signal degradation associated with complex analogue path.

Nowadays, digital pulse processing systems are available, with performances, in terms of timing and energy resolution, equal if not better than the corresponding analogue ones for a fraction of the cost per channel. The presented system uses a combination of a 15-bit 100 MS/s digitizer with a PowerPC-based VME single board computer. Real-time processing algorithms have been developed to handle total event rates of more than 1 MHz, providing on-line display for single and coincidence events.

INTRODUCTION

The principle functions of the front end electronics for nuclear physics applications are to acquire the electrical charge pulses generated by a radiation detector, to extract the quantities of interest and to convert them into a digital format. Usually these quantities of interest are the particle energy, the time of arrival and the shape information [1].

In an ideal acquisition system, the analog signal has to be converted into a digital data stream as earliest as possible and then transferred to preserve the information. Today with the modern digitizers the restrictions of the A/D conversion have been reduced because of the increment of the sampling frequency and the resolution in terms of the number of bits. Besides the loss of information due to the A/D conversion error, the major problem of the fully digital approach is the huge amount of data to handle. It is almost impossible to have a system in which the data throughput rate allows the acquisition of all the channels and makes the on-line analysis at the same time, the loss of data it will be dramatic.

In order to reduce the amount of data to be transferred, a Field Programmable Gate Array (FPGA) can be used to perform on-line digital pulse processing and consequently extract and save the relevant quantities [2].

The present paper will start with the description of the chosen digital approach solution to maximize the throughput of the acquisition system. The digital pulse processing algorithm section summarizes the applied techniques to reduce the amount of data and extract the quantities of interest. It will be followed by a description of the on-line acquisition engine implemented at the Institut Laue-Langevin to cover the experimental needs. The achieved performances in a series of real experiments will be discussed followed by the most important conclusions gathered in the development of the project.

DIGITAL APPROACH

In an ideal acquisition system, the analog signal is converted into a digital data stream as earliest as possible and then transferred, without any loss of information, to a computer that can make the analysis and extract the quantities of interest off-line. Thanks to a great variety of hardware available, the end user is able to best match the requirements of the specific experiment concerning the critical phase of the A/D conversion. Applications implementing very fast response detectors or requiring precise time determination will most profit from a reduced number of bits (typically 8 or 10 bit) and a high sample frequency (from 500 MS/s up to 5 GS/s). The opposite is true when high-energy resolution is required but the detector signals are relatively slow. In such a case 14/15 bit digitizers are better suited at a price of a lower sampling (typically 100 MS/s). Besides the loss of information due to the A/D conversion error, the major problem of the fully digital approach is the huge amount of data to readout. It is necessary to restrict the acquisition to some selected parts of the signals.

Like in a common oscilloscope, this happens firstly by means of the trigger defining a certain time window in which the signal has to be recorded (acquisition window). The difference between a common oscilloscope and a digitizer is that the latter has several memory buffers for the triggers and can save subsequent acquisition windows without any dead time between them. Therefore, the acquisition can take place without the loss of any event, no matter what is the frequency and the distribution of them, at least until the readout rate allows the empting of the memory buffers. For the present application we have chosen a CAEN digitizer (mod. V1724 – 8 channels 15

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bit 100 MS/s). Each channel of the digitizer is equipped with a dedicated FPGA that continuously writes the digital samples coming from the ADC into a circular memory buffer. When it receives the trigger, it keeps saving the post trigger samples, then freezes that buffer (which is made available for the readout) and continues to save the samples into a new buffer. The record length (number of samples in the acquisition window) and the size of the post trigger are both programmable.

The use of the trigger is the first step towards the reduction of the overall data throughput rate. However, in most cases, this is not sufficient because the number of channels, the event rate (i.e. pulses per second) and the event size (record length for each pulse) are such that the total throughput rate exceeds the capability of any type of readout bus. It is hence necessary to apply some data reduction technique.

The simplest approach is to discard the channels or some parts of the records that do not contain any significant information (zero suppression). The ideal would be to apply on-line digital algorithms able to extract from the signal only the quantities of interest (i.e. the time of arrival or the energy of the particle) and save and transfer to the computer only those numbers. Sometimes, the best compromise is to have an intermediate solution in which the digitizer saves part of the waveform together with the quantities calculated on-line.

DIGITAL PULSE PROCESSING ALGORITHM

The purpose of the Digital Pulse Processing (DPP) is to perform on-line signal processing able to transform the row sequence of samples into a compressed data packet that preserves the relevant information. For this purpose, a specific algorithm implemented in each channel's FPGA allows to extract the energy and/or the arrival time of the detected pulses. The pulse conversion starts as soon as a trigger is generated. In our case, this is via a voltage step overtaking a programmable digital threshold rather then comparing the absolute voltage level, as in the case of analog systems.

For an accurate time determination, the traditional approach would make use of a Constant Fraction Discriminator (CFD), where the zero crossing of the sum of the input and the delayed, attenuated and inverted input, delivers the wanted information independently of the amplitude of the pulse. In the digital CFD the FPGA calculate the second derivative of the input signal (the direct output of the detector preamplifier). The input signal can be represented as the sum of two exponential decays being the fast component determined by the time constant of the detector and the slow one by the RC of the preamplifier. A simple calculation demonstrates that the zero crossing of such a second derivate depends only on the two time constants while it does not depend on the pulse amplitude. The zero crossing of the second derivate of the input signal delivers, therefore, an accurate time determination with an uncertainty equivalent to one unit of the sampling time.

A trapezoidal filter is applied to the input signal to derive its amplitude, proportional to energy. This filter can be shortly described as an algorithm able to transform the typical exponential decay signal generated by a charge sensitive preamplifier into a trapezoid [3]. The height difference between the signal baseline and the flat top of the trapezoid is proportional to the amplitude of the initial pulse.

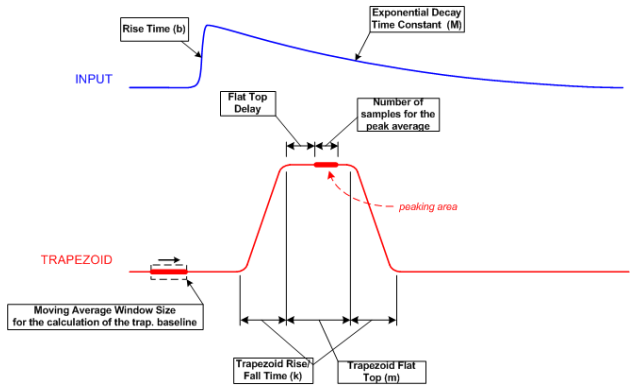

Figure 1: Trapezoidal filter with the relevant parameters.

Figure 1 describes all the relevant parameters necessary for a proper determination of the pulse height. This trapezoid plays more or less the same role of the shaping amplifier in a traditional analog acquisition system. We want to highlight the analogy between the two systems: both have a shaping time constant and must be calibrated for the pole-zero cancellation. For both, a long shaping time gives a better energy resolution but increases the probability of pile-up. Both are AC coupled with respect to the output of the preamplifier whose baseline is hence removed, but both have their own output DC offset, which constitutes another baseline for the peak detection. Setting the parameters of the trapezoidal filter is equivalent to change the shaping time in a classical spectroscopy amplifier.

ON-LINE ACQUISITION ENGINE

Our newly developed acquisition system consist of the following three main elements: a number of digitizers according to the required number of detectors, a processor card providing real-time algorithms and the instrument control software responsible for setting parameters, the real-time display and list-mode storage of data. Figure 2 represent schematically all the elements on the newly developed acquisition engine that will be discussed in further details in the following. The present system has been dimensioned according to the needs for the upcoming γ-spectroscopy campaign of measurements using the EXOGAM [4] high efficiency array of γ-ray detectors. Up to 10 segmented clover detectors will be used in the array. Segmentation is required to provide the optimum performance in terms of efficiency, energy resolution and minimization of multiple-hit events. These

Ge detectors will be surrounded by bismuth germanate BGO suppression shields and will also have passive heavy metal collimators for background reduction purposes.

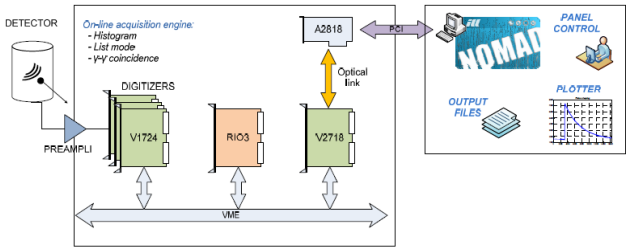

Figure 2: Schematic view of the acquisition engine.

Digitizers

The model used is the CAEN waveform digitizer board V1724. It is a 1-unit wide VME 6U module housing 8 channels 15 bit 100 MS/s flash ADC with threshold auto-trigger capabilities [5]. Trigger signals can be provided via the front panel input as well as via the VME bus, but they can also be generated internally, as soon as a programmable voltage threshold is reached. The individual auto-trigger of one channel can be propagated to the other channels and onto the front panel trigger output. The board features a front panel clock/reference I/O and a PLL circuit for clock synthesis from internal/external references. In this way, several boards can be phase synchronized to an external clock source or to a V1724 clock master board.

The digitizers consist of a common motherboard housing specific mezzanine cards for each channel. The motherboard houses the clock logic management and the readout control FPGA that provides the trigger management and acts as a bridge between the local bus and the different interfaces (VME 64X, Optical link, PCI express, USB 2.0). Mezzanine cards house the input front-ends and the channel FPGA that accounts for the analog-to-digital conversion, the digital pulse processing algorithm and the memory buffers. The readout control FPGA accesses the mezzanine cards through the local bus.

Processor Card

The real-time acquisition engine is implemented in a Power PC based VME board computer equipped with 256 MB of memory. This board does not contain any operating system to optimize real-time performances and prevent any dead time. A specific set of routines has been developed to account for the acquisition and all the functionalities necessary to access the digitizers [6]. We have developed real-time processing algorithms capable to handle total event rates of more than 1 MHz, providing on-line display for singles and coincidence events. The purposes of the processor card are:

- to create the data structures containing the variables and the parameters for the acquisition
- to initialize and program the digitizers
- to read the data from the digitizer, using BLT in the VME bus
- to analyze the acquired data extracting the wanted information and store them in the internal memory
- to generate the histograms for each input and for the coincidences.
- to create the list mode events
- to store list-mode data to the external mass storage.

Instrument Control Software

The instrument control software is acting as interface between the acquisition hardware and the user. It offers a full graphical interface to access all parameters related to the configuration of the digitizers as well as of the acquisition card. It allows real time visualization of all relevant spectra including double and triple coincidences.

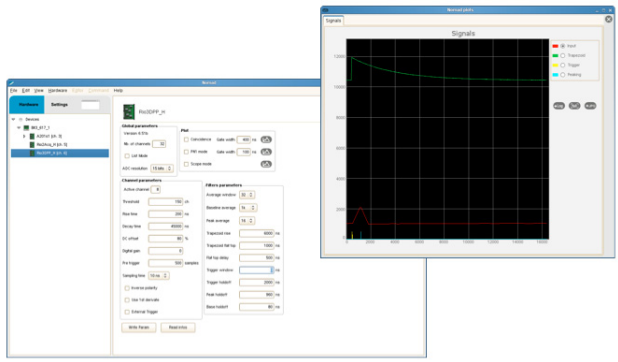

Figure 3: The digitizers setup screen and the oscilloscope live display.

Figure 3 depict the oscilloscope mode display used to tune the sampling parameters for each channel of the digitizer cards. This mode offers the unique advantage to visualize instantaneously the effects of any parameter modification with respect to all signals involved in the acquisition.

RESULTS

The new acquisition engine has been implemented with two different detector setups. The first test has been performed using an array of eight HPGe detectors for γ-spectroscopy studies from (n_{th}, γ) reaction. The goal of this experiment was, amongst others, to verify the beam quality, with respect to background and collimation, as well as the overall performance of the new acquisition in view of the upcoming EXOGAM campaign of measurements.

The detector setup of the second test was more complex, implementing a combination of HPGe and BGO detectors. The scientific goal of the experiment was to measure the e^+e^- pair-production cross-section close to the 1022 keV threshold [7]. We had the possibility to verify the accurate time synchronization amongst several digitizer cards as well as the capability of the system to handle detectors with completely different time response. Figure 4 shows the energy spectrum measured by the HPGe detector from ^{152}Eu radioactive source. We could

obtain an energy resolution of 2.45(5) keV at the 1408 keV γ-line. In the zoom area the doublet at 1085 and 1089 keV is clearly resolved.

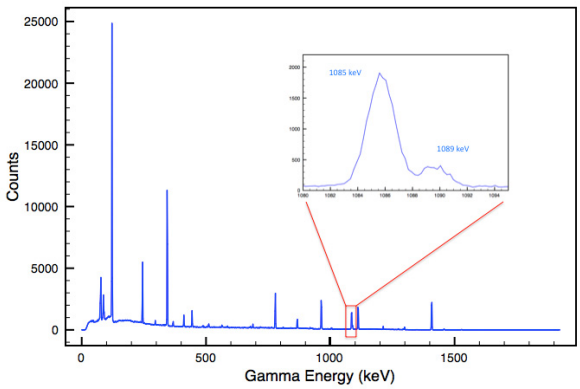

Figure 4: HPGe energy spectrum from the ^{152}Eu radioactive source.

From the analysis of the recorded list-mode data acquired using a ^{22}Na radioactive source in pair spectrometer mode, we could derive the timing properties of the new acquisition. The ^{22}Na source was selected because of the close vicinity of its 1274 keV γ-line with the energy range interesting for the experiment. Figure 5 reports the spectrum of the coincidence between BGOs and Ge detectors. The time difference between γ-detection in any of the BGO detectors and the corresponding detection in the Ge detector is plotted versus time. A single, very clean peak is visible at about 200 ns after the γ-detection in the BGOs.

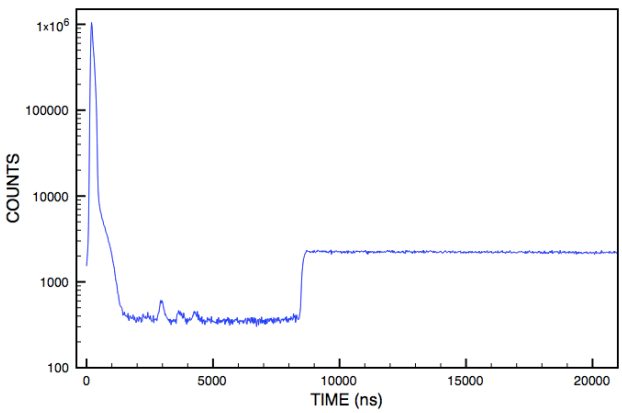

Figure 5: Time between BGO (start) and Ge (stop), measured for ^{22}Na source in pair spectrometer mode.

After about 8 μs the spectrum shows a rather low and extremely constant level of random coincidences. The absence of BGO-Ge coincidences below 8 μs could be explained by the conversion time of the system necessary to derive the energy and the time information. We do not have an evident explanation for the deformation of the main peak toward longer coincidence time. One possibility could be related to a slight misalignment in time on the signals from some of the BGOs.

CONCLUSIONS

The new acquisition system developed at the ILL implements a fully digital approach where the A/D conversion is performed directly on the preamplifier signal. With a reduced cost per channel, with respect to the analog approach, we are able to obtain information on energy, time and pulse shape. A direct comparison between the full digital system with an analog equivalent using the same detector did not show any significant loss in energy resolution.

All the relevant parameters are stored on EPROM for a maximum of flexibility and reproducibility. In the practical implementation using two different detector setups, the system has shown great modularity and the capability to be adapted to different types of signals from different detectors.

One major advantage is the possibility to acquire all signals independently from any trigger condition, reducing the chance of errors in the electronic setup and preserving a maximum of flexibility for the off-line analysis. Despite the large amount of data collected, the system never showed any significant dead time and our laboratory tests showed the possibility to achieve count rates higher that 1 MHz.

The combination of the new hardware and our control software offers the possibility to access a full set of graphical tools for configuration purposes as well as for on-line display of singles and coincidence spectra.

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