NSLS-II BEAM POSITION MONITOR EMBEDDED PROCESSOR AND CONTROL SYSTEM*

Kiman Ha#, J. De Long, Young Hu, Yuke Tian, Joe Mead, Kurt Vetter and L. R Dalesio BNL
Photon Sciences, Upton, NY 11973, U.S.A.

Abstract

The NSLS-II is a 3 Gev 3rd generation light source that is currently under construction. A sub-micron Digital Beam Position Monitor (DBPM) system consisting of hardware electronics, an embedded software processor and EPICS IOC has been successfully developed and tested in the ALS storage ring and BNL Lab.

INTRODUCTION

The BPM is a key component for the NSLS-II machine, it was designed and development based on digital down conversion and FPGA digital signal processing technology. Performance testing has already shown 200 nm stability under controlled thermal conditions [1]. The Digital Front End (DFE) board utilizes a Virtex-6 FPGA from Xilinx, it provides a Gigabit Ethernet TEMAC core and a Micro-Blaze 32-bit RISC soft core processor for system on a chip embedded applications. Digital signal processing components are designed and implemented using Xilinx System Generator and the Matlab/Simulink tools. The embedded processor was designed using Xilinx EDK for kernel based multi threaded applications. The DBPM uses an EPICS IOC for control and monitoring. The DBPM communicates with the IOC using a simple, robust Ethernet protocol to directly accesses a 1 GB DDR-3 memory space. An Industrial PC running the Linux Operating System (Debian 6) supports waveform monitoring including; ADC raw data waveforms (117 MHz), Turn by Turn (TBT, 378 kHz) waveforms, Fast waveforms (FA, 10 kHz) and slow data (SA, 10 Hz). ADC raw, TBT and FA data is triggered on demand and supports a large 1 million sample history buffer (~ 32 Mbytes) transmitted to host computers (EPICS IOC, Matlab stand alone client computer). The EPICS IOC application program is based on the EPICS Asyn driver for custom TCP/IP protocol communications. It provides very stable communication with the Microblaze core. This paper will describe the NSLS-II new advanced DBPM functionality, embedded software and EPICS for control systems.

HARDWARE

Figure 1 shows the NSLS-II DBPM design for the Injection system. It contains separated DFE and AFE boards. The DFE board includes a Virtex-6 FPGA and Gigabit ethernet PHY chip and 128 Mbyte x 16-bit Flash memory. The AFE board has four individual RF receiver channels and high speed digitizer a PLL, attenuators and a pilot tone RF frequency synthesizer.

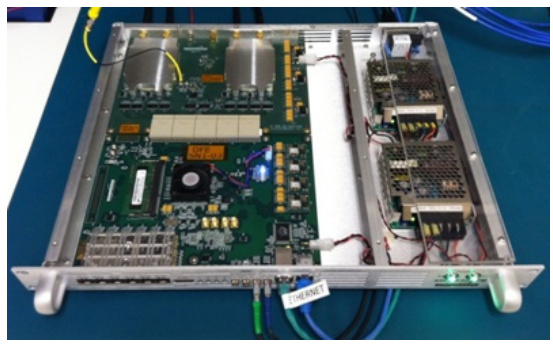

Figure 1: RF BPM for Injection System.

Embedded Event Receiver (EVR)

An embedded EVR with reduced functionality compared to the Micro Research Finland EVR board is implemented on the FPGA. The Embedded EVR synchronizes all of the BPM's data and generates synchronized clocks and trigger signals in addition to time stamps with 8 ns resolution.

Serial Data Interface (SDI)

A Fast Orbit Feedback System (FOFB) will be operational for the storage ring orbit stabilization. The NSLS-II requires a 10 kHz feedback rate. Vertical and horizontal Data is transferred to the cell controller every 100 uS using the Xilinx GTX transceivers at 5Gb/s. All data from all BPMs is collected at the cell controllers in approximately 20us.

RS232 Serial Interface

RS232 serial interface is used as a console port for the MicroBlaze processor. It is very helpful with system monitoring and diagnostics. The Microblaze initial boot information is displayed on the serial console. Boot manager, system reboot command and remote updating are operated using the serial console. This serial port connects with a terminal server (Ethernet to Serial converter box) for remote operation.

Tri-Mode Ethernet Interface

Virtex-6 Microblaze based TCP/IP socket communication performance is 4 Mbytes/sec, the RAW API mode is 3 times faster and the test results show a maximum of 12 MByte/sec. But the RAW API functions

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#*kha@bnl.gov

have some limitations in that buffer overflow occurs during the multiple frame transmits. The DFE board utilizes onboard Marvel Alaska PHY device (88E1111) for Ethernet communications it supports 10/100/1000 Mbps/sec. The DFE board supports only GMII interface from the FPGA to the PHY chipset. The PHY connection to the EPICS IOC is through an RJ-45 Ethernet connector with built-in magnetics. The FPGA clock generator provides a 25 MHz external clock to PHY clock input.

EMBEDDED SOFTWARE

Figure 2 shows the internal FPGA components of the embedded processor and HDL signal processor. Xilinx provides a flexible embedded software development environment. The DBPM target board embedded software uses Xilinx Kernel mode. The Microblaze has application threads for multiple socket ports communicating with client applications. Multi sockets provide optimized communication speeds for different data structures. For example large waveform array reading (~32 Mb) takes approximately 30 seconds, to allow higher priority data transfers the large waveform thread can be pre-empted. For the embedded firmware development Xilinx software tool versions: XPS/SDK 13.2, Microblaze 8.2a, XilKernel 5.0 and LWIP 3.0 a are used..

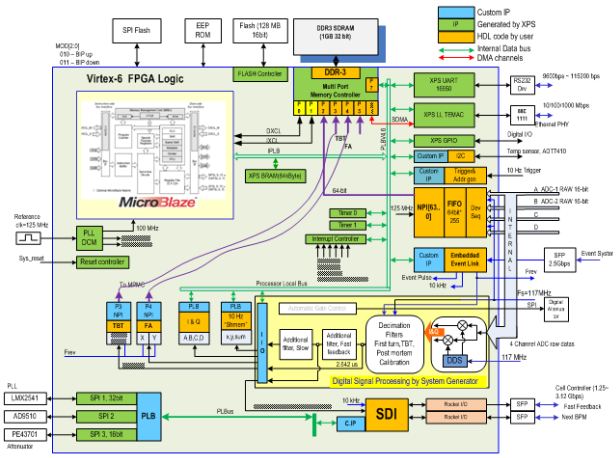

Figure 2: FPGA internal components for control and data processing.

MicroBlaze Soft Processor

The Microblaze core is a 32-bit RISC soft core processor using a Harvard architecture optimized for embedded applications. The Microblaze has a floating point unit, memory management unit, instruction and data caches and many other optimization functions. The EDK tool provides a simplified configuration wizard and it easily configures the BSP for FPGA embedded application. The Microblaze primary bus is the PLB, as master the MicroBlaze connects to slave PLB I/O peripherals. For the Virtex-6 DFE board the Microblaze and PLB are running at 100 MHz.

Lightweight IP (lwIP)

LwIP is an open source TCP/IP network stack for Microcontroller Ethernet applications. Xilinx EDK provides lwIP software customized to run on Xilinx Embedded systems. lwIP provides a TCP/IP socket layer API and raw API layer for applications. lwIP socket API is very similar to the Berkeley/BSD sockets therefore easily implements network programming . The lwIP v3.00.a version library is provided by Xilinx EDK 13.2.

MicroBlaze Processor Local Bus (PLB)

The Microblaze local bus interface is the 32-bit PLB and all I/O peripherals are PLB slaves. The Microblaze Data/Instruction cash bus interface to the multi-port memory controller which connects to the DDR-3 memory. Using external cash increases Microblaze and TCP/IP communication performance.

Multiport Memory Controller (MPMC)

Figure 3 and 4 show DDR write timing and the memory map. The MPMC is a key component for system performance tuning and real time operation. The MPMC physicaly interfaces to the DDR-3 memory and provides eight individual ports for the user bus interfaces. The DFE uses a SODIMM socket type 1GB DDR-3 memory and it is clocked at 400 MHz. It operates at double the rate of the clock and total the transfer rate is 32bits * 800 MHz. MPMC port 0 and port 1 is assigned for Microblaze Data/Instruction cash. Port 2 is a soft DMA port for the Gigabit Ethernet driver. Port 3 is connected to the ADC raw data path and operates at the ADC sampling frequency (117 MHz). Port 4 is assigned to the TBT data bus and Port 5 is assigned to 10 kHz FA data. One million points of ADC raw data and TBT and FA data can be copied to DDR-3 memory on demand or on a repetitive trigger.

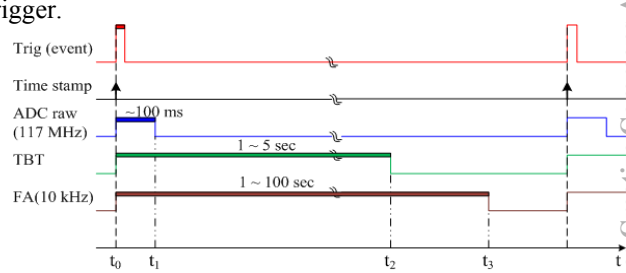

Figure 3: Timing of the waveform transmitter to DDR-3.

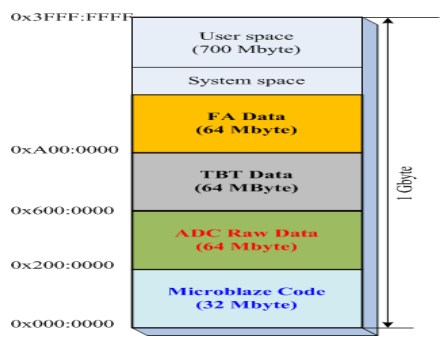

Figure 4: DDR-3 memory map (1 Gbyte).

BPM CONTROL AND IOC

Feedback control and event system links are separated from Ethernet because the global fast orbit feedback rate is 10 kHz and must provide global BPM data to the cell controllers deterministically. Similarly the event system runs at 125 MHz and requires determinism. Figure 5 shows a single cell BPM system configuration. The NSLS-II storage ring is divided into 30 such cells. Each cell has a VME EVR, a Linux IOC for communications and a cell controller for the fast orbit feedback system.

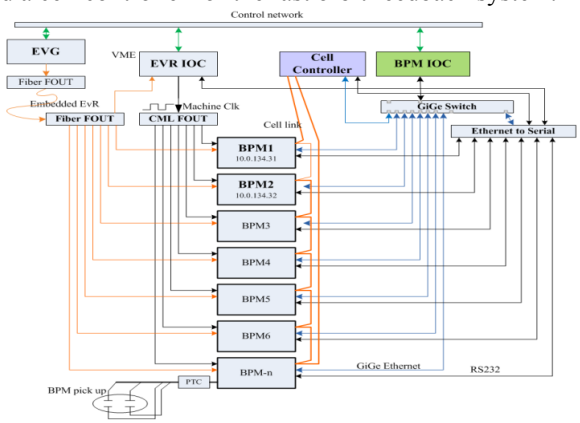

Figure 5: Layout of single cell.

Figure 6 shows embedded BPM software and EPICS IOC connect configurations. The Control System uses the Linux IOC for DBPM signal control and monitoring. IOC and BPM communication ports support Gb Ethernet. This communication uses a simple protocol based on register memory mapping. The DFE main device which is a Virtex-6 provides a hardware TEMAC Ethernet core and Microblaze soft processor that handle TCP/IP communication protocols. The EPICS IOC has three threads running for communication with the DBPM. The SA thread is designed for reading SA data (1024 bytes) and control register reads at the 10 Hz rate. The Microblaze SA server uses the RAW TCP/IP API functions for improved performance. The DDR waveform thread uses the socket TCP/IP API functions for stable communication because waveform data sets can be as long as 32 Mbytes. The DBPM EPICS IOC is an Industrial PC running the Linux Operating System, most communication is based on Ethernet ports.

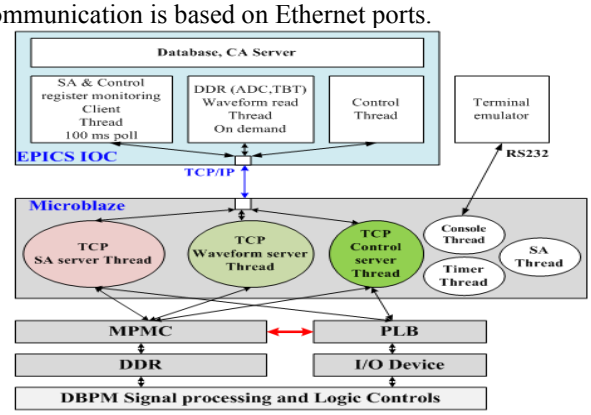

Figure 6: Control systems for BPM.

EPICS EXTENSIONS

Figure 7 shows EDM client examples for BPM controls and data measurements. ADC waveforms include 4 button signals: A, B, C, D and SUM data, the displayed waveform length is 4 k points and a slider PV can control the offset address within the 1Mpoint waveform. TBT waveforms include A, B, C, D, X and Y position, Sum and Q data. The TBT waveform length is 8000 points and a slider PV can control the turn offset within the 1 Million turn waveform. 10 kHz waveforms are the same as TBT waveforms. 10 Hz data is the 10 kHz data averaged over 1000 samples.

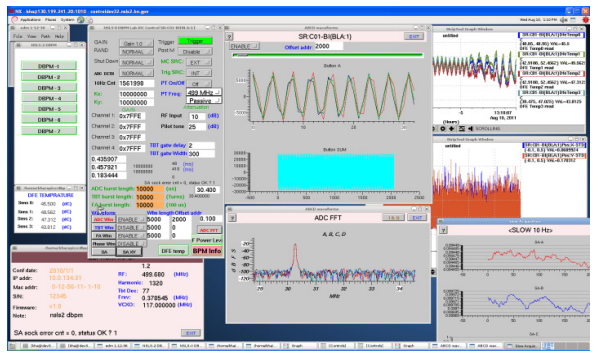

Figure 7: EPICS EDM screen for control and waveform monitoring.

SUMMARY

The development of sub-micron BPMs and their control system for the NSLS-II has been completed and successfully tested in the EPICS environment. FPGA based embedded software provides very reliable and stable operation. This year we will produce BPMs for the Linac and Injection systems, continue developing embedded firmware and EPICS software for the Booster and Storage ring BPMs.

ACKNOWEDGMENT

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REFERENCES

[1] K.Vetter et al., "NSLS-II RF Beam Position Monitor", BIW10, Santa Fe, NM, US.