EMBEDDED LLRF CONTROLLER WITH CHANNEL ACCESS ON MicroTCA BACKPLANE INTERCONNECT

K. Furukawa*, K. Akai, A. Akiyama, T. Kobayashi, S. Michizono, T. Miura, K. Nakanishi, J. Odagiri
High Energy Accelerator Research Organization (KEK), Tsukuba, Ibaraki, 305-0801, Japan
H. Deguchi, K. Hayashi, M. Ryoshi
Mitsubishi Electric Tokki Systems, Amagasaki, Hyogo, 661-0001, Japan

Abstract

A low-level RF controller has been developed for the accelerator controls for SuperKEKB, Super-conducting RF Test facility (STF) and Compact-ERL (cERL) at KEK. The feedback mechanism will be performed on Virtex-5 FPGA with 16-bit ADCs and DACs. The card was designed in the form-factor of an advanced mezzanine card (AMC) for a MicroTCA shelf. An embedded EPICS IOC on the PowerPC core in FPGA will provide the global controls through channel access (CA) protocol on the backplane interconnect of the shelf. No other mechanisms are required for the external linkages. CA is exclusively employed in order not only to make the AMC cards to communicate with each other, but also to communicate with central controls and with an embedded IOC on a Linux-based PLC for slow controls.

INTRODUCTION

The low level radio frequency (LLRF) is one of the crucial facilities to enable the high precision and high stability of the particle accelerator beams. There are several accelerator projects planned at KEK. New projects are always demanding to achieve higher experimental results, and the LLRF control should play an important role there. After the recent development at KEK the digital LLRF controls are well accepted, and three accelerator projects began to share the developments, namely Compact ERL (cERL) as a demonstration machine for the future energy recovery linac (ERL), SuperKEKB for B-physics study, and Superconducting RF Test facility (STF) for the international linear collider (ILC). They are sharing a single LLRF controller design.

In order to achieve a higher stability for better beam quality fast digital feedback or feed-forward mechanisms are utilized on those LLRF controllers. A field programmable gate array (FPGA) is employed to carry those tasks with high precision ADCs and DACs, and it would maintain the stability of RF cavities that are covered by the controller.

On the other hand, global controls are indispensable in order to achieve overall performance of those accelerators. Sensor signals from beam instrumentation are analyzed and applied to actuators along the accelerator to improve the beam quality. Among those actuators LLRF is the fastest and the most important. Thus, the LLRF controller needs to be designed with global control capability in mind from the beginning. Globals controls are provided by EPICS (experimental physics and industrial control system) in these accelerators [1].

We designed the LLRF controller for three accelerator systems with MicroTCA platform and embedded EPICS. Even a single LLRF controller card can perform the same EPICS control functions as other I/O controllers.

* < kazuro.furukawa @ kek.jp >

LLRF CONTROLLERS AT KEK

Digital LLRF controllers were developed at KEK since 2003, and it was applied for J-PARC linac at first [2]. It was based on CompactPCI platform, and has been performing well. Based on the experiences at the J-PARC linac, LLRF controller on an advanced telecommunication computing architecture (ATCA) platform was designed for STF, because ILC chose ATCA as a possible control platform [3]. Management facilities provided by ATCA were indispensable to achieve reliable controls even with large number of accelerator components. Actually, the large board area provided by ATCA standard was adequate to accommodate a number of analog control and monitor circuits which were required by the baseline clustered klystron scheme of ILC.

The ATCA standard includes the advanced mezzanine card (AMC), and for example LLRF controllers at DESY employed AMCs on ATCA carrier card, instead of a direct ATCA card. When the LLRF controller for cERL was designed, the standard of MicroTCA was just finalized, based on AMC. The size of the standard AMC card was just enough for the small number of analog circuits at cERL. Then, MicroTCA was chosen for cERL LLRF [4]. It aimed at the future stability of 0.01 % in amplitude and 0.01 degree in phase.

It turned out that the LLRF controller at SuperKEKB shared the same requirements as one at cERL, and it was decided at SuperKEKB to employ the same design of LLRF controller [5].

Later, a new RF system configuration of distributed RF system (DRFS) was adopted at STF in the framework of S1 Global. It does not require a large card size any more compared with the clustered klystron scheme. Thus, the same LLRF card will be utilized at STF as well [6]. The choice of the controller platform at three projects above followed the synergy of the previous developments, and MicroTCA was chosen.

Computing Platforms and MicroTCA

The ATCA standard was defined in 2003 for a new computing standard for telecommunication and industry as a descendant of CompactPCI standard which was used since 1993. ATCA employed a large card area for high-performance computing, many serial interconnects on the backplane, 2.5 Gbps each, for larger bandwidths and IPMI surveillance and remote management facility for higher reliability. Even though it was designed for telecommunication and industry, the design approach of ATCA was considered adequate for ILC controls.

AMC mezzanine card was included in the ATCA standard, and AMC itself inherited many of good part of ATCA. Later in 2008, MicroTCA was standardized with direct slot-in AMC cards. As embedded controllers became smaller with the evolution of FPGA technologies, MicroTCA is considered one of the proper embedded platforms.

Both of the ATCA and MicroTCA backplanes allow fast serial communication such as Gigabit Ethernet (GbE) and PCIe. If we choose GbE as a communication media, a switch module in the box can transfer packets directly to the external networks. In MicroTCA the switch is called MCH (MicroTCA Carrier Hub), and it connects the serial backplane interconnect to an external network through a layer-2 switch.

GLOBAL CONTROLS WITH EPICS

The accelerator control architecture in KEK evolved in several steps in the past. Some time ago several control systems were standardized with a combination of several fieldbuses, VME field computers, and Unix computers. In order to consolidate the efforts on the development and maintenance some of the fieldbuses were gradually removed and many controllers were directly attached on to IP networks [7].

At the same time EPICS (Experimental Physics and Industrial Control System) control software framework was employed at several control systems at KEK. Eventually, many controllers evolved to embed the same EPICS software as on VME field computers. The EPICS component on those field computers is called IOC (Input/Output Controller), and it communicates with others using a common protocol called Channel Access (CA). We call this embedded EPICS framework as "CA Everywhere", and it enabled the both rapid development and smooth maintenance.

Several different kinds of controllers have been developed in the framework of CA Everywhere, and they greatly reduced the control efforts and improved the reliability [8].

LLRF CONTROLLER WITH EPICS CA EVERYWHERE

As described above MicroTCA can accommodate GbE and TCP/IP on the backplane interconnect directly. In addition, many field controllers recently employ the idea of CA Everywhere to embed EPICS IOC software at KEK. Thus, it was rather natural to design the new LLRF controller with embedded EPICS IOC software, and make it connect with the global control network with EPICS channel access protocol directly through the backplane as in Fig. 1.

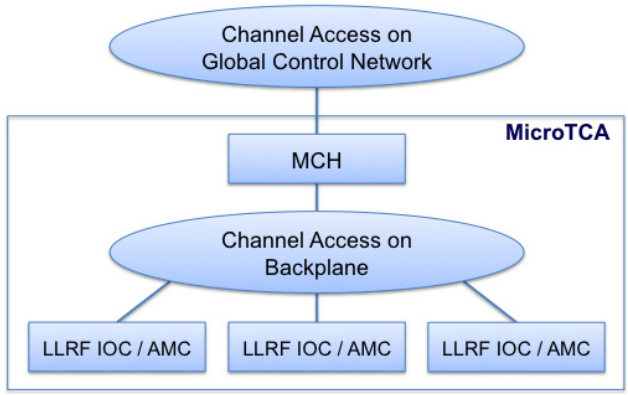

Figure 1: EPICS IOC software is embedded in controller cards and EPICS channel access protocol is used everywhere.

The PowerPC CPU in Virtex-5 FPGA on the LLRF controller runs Linux 2.6.21, and EPICS IOC 3.14.9 is embedded. The Linux kernel is booted from the on-board flash memory. On the other hand EPICS IOC software is loaded from a NFS file server, as the software can be improved frequently. Device support software to link between FPGA and IOC was developed using mmap() interface.

Hardware Features

The controller module was fabricated in a single-width full-height AMC module with two analog boards and a digital board, as shown in Fig. 2. The analog boards comprise four channels of 16-bit 130 Msps ADCs, four channels of 16-bit 500 Msps DACs. The digital board accommodates a Xilinx Virtex-5 FXT FPGA with PowerPC-440 hardcore CPU, 640MB RAM, 64MB flash memory, digital I/Os, IPMB, and GbE. IPMB (intelligent platform management bus) is used to manage the AMC in order to improve the reliability.

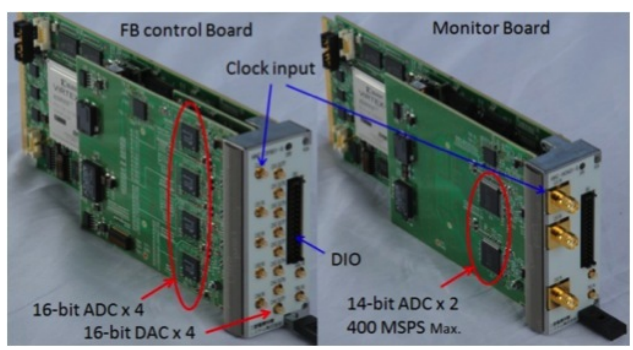

Figure 2: LLRF controller and monitor cards.

The digital part was designed based on the evaluation board of Xilinx ML507. The software for the controller was initially developed on ML507, and the main part of Linux implementation was provided by Wind River Linux 2.0.

Besides the feedback controller card, a LLRF monitor card was designed with the same digital board but with another analog board of two channels of 14-bit 400 Msps ADCs.

Other EPICS Embedded Controllers

Slow controls for cavity vacuum and so on are provided by a PLC system. It is equipped with Yokogawa's F3RP61 CPU with Linux 2.6.26, and EPICS IOC 3.14.11 is embedded on it.

The machine protection system at cERL employed a modular system which is served by a commercially available FPGA card. The card consists of Xilinx Virtex-4 with PowerPC and Linux 2.6, that embeds EPICS IOC 3.14. This card is used for other controllers as well.

The same protocol and the same software environment are shared between LLRF controllers and external servers and clients. That enables a reliable control system. The system structure is described in Fig. 3.

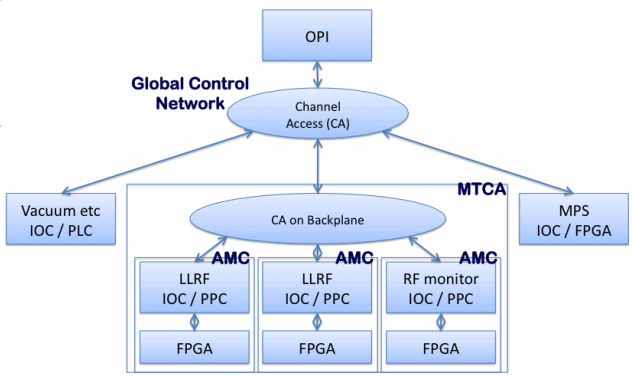

Figure 3: LLRF controller AMC cards can communicate locally on the MicroTCA backplane interconnect and globally through normal IP networks both using EPICS channel access protocol.

Enhancement Possibility

MicroTCA inherits several mechanisms from ATCA to enhance the availability, which can be utilized in order to improve the reliability of the LLRF system. Redundant power supplies, MCHs and CPUs are being evaluated as in Fig. 4. Presently, processes in LLRF system is carried on the IOCs on controllers. Additional CPU modules can be introduced into MicroTCA box to facilitate local processes among several controllers. We may run EPICS redundant IOCs on those redundant CPUs to enhance the reliability further [9].

After this controller was developed, the MicroTCA physics extension (MTCA.4) was defined. This platform may relieve the busy set of three circuit boards in the controller. We may utilize this new standard in the future.

Figure 4: Redundant CPUs, MCHs and power supplies are evaluated as a possible future extension.

The combination of fast ADCs, DACs and FPGA may serve as a general controller. As a connection to global EPICS controls was also provided, this controller can be applied for many different purposes in machine controls. Actually, the same controller card is evaluated for a specific beam monitor at SuperKEKB.

CONCLUSION

As a natural consequence of several developments at KEK, a LLRF controller in MicroTCA AMC with EPICS CA protocol on the backplane interconnect was developed. All controllers embed EPICS IOC to share the same software and protocol both locally and globally for rapid developments and smooth maintenance, including auxiliary controllers with PLCs and FPGA modules. This LLRF system is being applied to three accelerator projects of SuperKEKB, cERL and STF at KEK.

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