PROGRESS OF THE TPS CONTROL SYSTEM DEVELOPMENT

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Abstract

The Taiwan Photon Source (TPS) is a low-emittance 3-GeV synchrotron light source which being in construction at National Synchrotron Radiation Research Center (NSRRC) campus. Control system for the TPS is based on EPICS framework. Standard hardware and software components were defined. Prototypes of various subsystems are in implementation. Event based timing system was adopted. Power supply control interface accompany with orbit feedback support are also defined. Machine protection system is in design phase. Integration with the linear accelerator system which are installed and commissioned at the temporary site for acceptance test was already done. Interface to various system are still in negotiate stage. Development of the infrastructure of high level and low level software are on going. Progress will be summarized in the report.

INTRODUCTION

The TPS [1] is a latest generation of high brightness synchrotron light source which is being in construction at the National Synchrotron Radiation Research Center (NSRRC) in Taiwan. It consists of a 150 MeV electron linac, a booster synchrotron, a 3 GeV storage ring, and experimental beam lines. Civil construction has started from February 2010. The construction works are scheduled to finish in later 2102. Accelerator system installation and system integration will be proceeding in the year of 2013. Commissioning with beam is scheduled in the first quarter of 2014. Control environment should be ready in 2013 to support subsystem integration test and hardware commissioning without beam. Control system for the TPS is based on the EPICS framework [2]. The EPICS toolkit provides standard tools for display creation, archiving, alarm handling and etc. If users have found these tools inadequate, development of in-house alternatives is feasible and compatible. The big success of EPICS is based on the definition of a standard IOC structure together with an extensive library of driver software for a wide range of I/O cards. Many users of the system report a steep learning curve and the need for significant development resources, but this is balanced by the large installation base and proven ability of this approach. The EPICS toolkits which have various functionalities will be employed to monitor and to control accelerator system. The control system consists of more than a hundred of EPICS IOCs. The CompactPCI (cPCI) IOC will be equipped with input/output modules to control subsystems as standard IOC or the TPS control system. The power supply and fan module of the cPCI crate will be hot-swapped. Adopting cPCI platform for EPICS IOCs provides us a chance to take advantages of local IT industry products with better supports and low cost. The other kinds of IOCs are also supported by the TPS control system, such as BPM IOC, PLC IOC, various soft-IOC and etc. Consoles and servers are PCs or blades PC running Linux. To achieve high availability of the control system, emphasis has been put on software engineering and relational database for system configurations. Data channels in the order of 10^5 will be serviced by the control system. Accessibility of all machine parameters through control system in a consistent and easy manner contributes to the fast and successful commissioning of the machine. High reliability and availability of TPS control system with reasonable cost and performance are expected.

CURRENT STATUS

Major procurement is scheduled in 2011 to 2012. The design for the control system environment is already frozen in the hardware part. The software environment will be completed in 2012. Control related applications are started and expected to a preliminary form before subsystem ready in early 2013. Define TPS control system standard processed during the last couple of years. Efforts of the control system development status are summarized in following paragraphs. Progress on various issues is summarized in following paragraph.

Networking

Mixed of 1/10 Gbps switched Ethernet will be deployed for the TPS control system [3]. The Gigbit Ethernet connection will be delivered at edge switches installed at control and instruments area (CIA). One CIA corresponding to one cell of the storage ring, there are 24 CIAs total. The control network backbone will be 10 Gigabit link to the control system computer room and redundancy network installation site in the specific CIA #24. Private Ethernet is used for Ethernet based devices access which will support fast Ethernet and GbE. Adequate isolation and routing topology will balance between network security and needed flexibility. The file and database servers are connected to the control and intranet network, allowing the exchange of data among them. Availability, reliability and cyber security, and network management are focus in the design phase.

Equipment Interface Layer

There are several different kinds of IOC at equipment interface layer to satisfy various functionality requirements, convenient, and cost consideration. Most of the devices and equipments will connect to cPCI IOCs crates running EPICS directly. The 6U cPCI platform was chosen for the EPICS IOC platform. Local company manufactured crate and CPU module providing an economic solution is the major reason. To simplify various developments at construction phase, only 6U modules will be supported for the machine control system. The cPCI EPICS IOC equipped with the latest generation CPU board will be standardized as ADLINK cPCI-6510 CPU module [4]. The CPU module equipped with Intel Core i7 CPU running Linux delivery high performance to meet various applications. The latest releases version of Fedora core Linux distribution is adopted at IOC level. The cPCI-7452 128 bits DI/DO module will be used for BI, BO solution, this high density version in 6U form factor will save crate slots and satisfy most of applications. Industry pack (IP) carrier board in 6U cPCI form factor can equip up to 4 IP modules. Various IP modules are adopted for necessary applications. ADC and DAC modules in IP module form factor will be used for smaller channel count application, such as insertion devices control. Event system modules are in 6U cPCI form factor. Private Ethernet will be heavily used as field-bus to connect many devices. Power supplies of all magnets except for correctors are equipped with Ethernet to the EPICS IOC communication. Multi-axis motion controller with Ethernet interface will be the standard support for the control system.

Ethernet attached devices will connect to the EPICS IOC via private Ethernet. Some network attached devices might cannot work properly when the network traffic busy due to its simply TCP/IP stack implementation. Private network ensure lower traffic to ensure the reliability and performance of the links. Devices support VXI-11, LXI, Raw ASCII, Modbus/TCP protocol can connect to the EPICS IOC via TCP/IP interface directly. Devices of this category include power supply, temperature acquisition (RTD or thermocouple), digital multi-meters, oscilloscopes, signal generator, and other instruments.

High resolution ADC module embedded with EPICS IOC from D-tAcq [5] will be used for the analogue signal reading, it provides 10 Hz rate reading and has transient capture buffer up to 100 Ksample/sec sampling rate.

All corrector power supply will interface by the corrector power supply controller (CPSC) module. The CPSC equip with 20 bits DAC and 24 bits ADC. Corrector power supplies will be driven by the output of this module. Two SFP ports supported by the on board FPGA (Spatan 6), these SFP ports will receive correction setting (Autora and Gigabit Ethernet by using UDP/IP protocol) from fast orbit feedback FPGAs ot slow orbit feedback PC, feed-forward correction computer and IOC. Setting command received by these SFP ports will be added with the slow setting from EPICS CA setting.

Power Supply System Control

TPS power supplies control interface are divided into three categories rather than a unified solution [6]. All of the power supplies will be provided by three different vendors. The reason of this choice is to meet the practical situation from budget and available vendors and manpower.

The small power supply for corrector magnets, skew quadrupoles in the range of ±10 Amp categories. This category power supply will be in module form factor. Each power supply subrack can accommodate up to 8 power supply modules. A custom design CPSC module will be installed at control slot of the sub-rack. The CPSC will be embedded with EPICS IOC and provide fast setting SFP ports to support orbit feedback functionality. Power supply modules installed at the same sub-rack will interface to this CPSC module. The CPSC installed 20 bit DAC and 24 bit ADC to ensure necessary performance for the orbit control especially in vertical plane of the storage ring. To simplify the type of power supply, this category power supply will be used for the corrector of LTB/BTS/Booster Synchrotron, and storage ring as well as skew quadrupole magnet power supply. The CPSC modules support waveform capability which can support corrector ramping for the booster synchrotron if necessary.

The intermediate power supply with current rating 250 Amp will be equipped with Ethernet interface. Power-supplies are expected to have internal data buffer with post-mortem capability. Output current of the power supply will output at rear plane BNC connector, which can connect to the cPCI ADC module also. There are two versions of power supply in this category, sextupole power supply with 16 bits resolution and quadrupole power supply with 18 bits resolution DAC. Both kinds of power supply can meet the 50 ppm and 10 ppm performance specifications for long-term drift. Both kinds of power supply noise level are in the 10 ppm range of the full scale

The storage ring dipole DC power supply and power supplies for the dipole and quadrupole power supply of the booster synchrotron had already contracted to the IE Power (Acquired by Eaton in 2011). The control interface will be a serial interface. It is expected that a serial and Ethernet adapter enable directly Ethernet connection. Control resolution of these power supplies will be 18 effective number of bits, noise and drift will be better than 10 ppm of these power supplies. The dipole and quadrupole power supply of the booster synchrotron have built in waveform support with external trigger capability. This functionality is essential for energy ramping of the booster synchrotron. All of these power supplies will interface with the EPICS IOCs directly.

Timing System

The event system consists of event generator (EVG), event receivers (EVRs) and a timing distribution fiber network [7, 8]. EVG and EVRs can be installed with various universal I/O mezzanine modules to meet different input/output requirements. The mechanical form factor of EVG and EVRs is in 6U cPCI module. The 125 MHz event rate will deliver 8 nsec coarse timing resolution. Fine delay is also supported by UNIV Output module with fine delay and special EVR which can generate gun trigger signal. Its high resolution and low timing jitter allow accurate synchronization of hardware and software across the TPS control system. Its usage simplifies the operation of the machine and allows complex sequences of events to be carried out by changing very few parameters. Prototype system was delivered in March 2011 already and applied to the TPS linac system commissioning at the temporary site successful. Consideration for the injection sequence control is also in intensive study.

Insertion Devices Control Interface

Insertion devices (ID) control for the phase I project include one set of EPU46, two sets of EPU48 and seven sets of in-vacuum insertion devices (two sets of 2 meter long IU22, three set of 3 meter long IU22, and one set of 3 meter long IU 22 with taper functionality). The driven mechanism of EPU46 and EPU48 are drive by servo motors. All IU22 drive by stepping motors. The motion controller is Galil DMC-404x Etherent/Series Accelera motion controller. Preliminary version of EPICS devices supports for this motion controller is in use. Improve is under way. The cPCI EPICS IOC equips with AI/AO/BI/BO I/O modules will serve each ID. All IDs will equip with SSI optical encoder. All encoder are connected to the motion controller. All parameters of motion controller will map to EPICS PV. Update rate up to 200 Hz is feasible. This might useful for feed-forward compensation which need to know the encoder value as fast as possible.

Diagnostic System Interface

New generation digital BPM electronics [9] is equipped with Ethernet interface for configuration and served as EPICS CA server with 10 Hz data rate. Another multi-gigabit interface will deliver beam position for fast orbit feedback purpose at rate up to 10 kHz. The BPM electronics will also provide post-mortem buffer for orbit analysis during specific event happened like beam loss. Post-mortem analysis can help to find the weakest point and provide information to improve system reliability.

High precision beam current reading and lifetime calculation will be done at a dedicated IOC. This IOC will install EVR to received booster cycle timing signals and high resolution IP ADC modules to digitize the DCCT signal and perform beam lifetime calculation.

The GigE Vision digital cameras will capture images for diagnostic purposes and other applications.

Counting type and integrating type beam loss monitors will be connected to the control system by counter or ADC modules installed at IOCs.

Feedbacks and Feed-forward Plans

Since the TPS adopt aluminium chamber with 4 mm in thickness. Eddy current effects prevent the standard corrector from fast corrector. Four fast correctors will be installed at bellows site for each cell. So, the global orbit feedback system by using slow and fast correctors in the same feedback loop is the baseline design [9]. A counter rotate multi-gigabit links will circulate 10 kHz rate orbit data among all BPM platforms. The FPGA module embedded in the BPM platforms will be configured as distributed fast orbit feedback engines. All of these platforms will be installed with EPICS interface for various feedback supports such as PID parameters, and matrix download. The correction command from FPGAs will be sent to the CPSC module located at the power supply sub-rack via Aurora links. The data buffer in the FPGA module can be used to capture fast orbit data up to 100 sec at 10 kHz rate for feedback system diagnostic and performance study. The capture can be triggered either software or hardware with post-mortem capability.

The slow orbit feedback is planned to use one dedicated EPICS IOC for each plane (maybe one aTCA compute blade for each plane). The orbit data can be acquired by the EPICS CA access or from the BPM grouping data directly by UDP/IP link. The slow orbit feedback will used the slow transfer matrix to calculate the correction values. The slow feedback loop will read the DC value of the fast corrector regularly (1 ~ 10 times/sec), multiply the inverse of the fast response matrix to get the orbit distortion which cause due to the DC setting of fast correctors. The same orbit distortion will transfer to the setting value by the slow correctors. This scheme can ensure the setting of the fast corrector always around zero. This will keep the maximum dynamic range of the fast corrector to suppress fast perturbation. The corrector setting for the slow orbit feedback loop is via UDP/IP packet. All setting value of the correctors are packed in one UDP/IP package. Each CPSC module extract their setting form specific offset within the packet. One packet can serve for all slow corrector in one plane for the whole ring.

The bunch-by-bunch feedback system will adopt signal processor based on the latest generation FPGA processor with embedded EPICS IOC and build-in diagnostics.

Turnkey System Solution

Turnkey systems such as linear accelerator and RF transmitters were delivered by industry as turnkey contracts and EPICS control environment. Work on EPICS support for the turnkey system with proprietary control environment is also not a problem. It is expected

that the turnkey systems delivered no matter with or without EPICS control system can integrate with the TPS control system. The linac system delivered in June 2011 and done acceptance at accelerator test site. It will move to the TPS linac site in later 2012 after civil construction of the TPS building is completed. Two RF transmitters were received in 2010. EPICS ready interface of these delivered system proved that the integration is not a big problem.

PLC and Interlock Solution

Current TPS control system will support Siemens S7-300 or compatible model from VIPA PLC which are delivered from the turn-key vendors. Yokogawa FM3R PLC will be used for most of control system related interlock system. FM3R with embedded EPICS IOC will be used for some applications also. Each subsystem is responsible to build their own interlock and protection system based on their requirement and preference. The global machine interlock system will collect various interlock signals from local interlock subsystem of orbit, vacuums, front-ends, radiation dosage monitors and etc. The beam disable commands to trip beam or inhibit injection can be distributed to the specific devices or subsystem by the global machine interlock system or uplink functionality of the event system.

Operator Interface

The operator interface level consists of Linux PCs for consoles and servers for various purposes. Various EPICS OPI tools and Matlab will be adopted for OPI development [10, 11]. It is planned currently that most of the GUIs will be implemented by EDM and Matlab. Consoles in the control room have multiple LCD screens. The OPI computer will be installed at the equipment area of control room with optical PCIe extension to remote display unit at control room. This can provide better cooling for the computer, reduce loudness at control room and provide clean control consoles. Large screen format displays hang on the roof at control room will be available for display of important parameters likes beam current, lifetime, vacuum distribution, synchrotron radiation image and etc.

Control Applications

Generic applications provided by the EPICS toolkit will be used for all kinds of applications. Standard tools such as the archiver, alarm handler and save/restore tools are supported. Channel Access (CA) is used as an interface for machine process variables (PVs) access. Simple tasks such as monitoring, alarm handling, display and setting of PVs are performed using EDM panels and strip tools. Cold start, warm up and shutdown process will done by Matlab scripts.

Physics Applications Interface

The accelerator physics tools for TPS include extensively adopted Matlab Middle Layer (MML) and Accelerator Toolbox (AT) software packages. It enables various developed applications of different machines to be directly adopted for TPS applications. The MML has also provided a systematic way of managing machine data, and is easily extended to separate data from transfer lines, booster and storage ring. The Middle Layer communicates with the machine from within MATLAB using LabCA. To enable early testing of the physics tools through the control system, a virtual accelerator has been implemented to give simulation of the accelerators through the EPICS PV interface. It was developed by provided EPICS device support to interface the model using the AT and MML.

SUMMARY

Implementation of the TPS control system is in on going. Major procurement is in proceeding. Assembly and system integration is scheduled in 2012-2013. The TPS control system will take advantages of the latest hardware and software technology to deliver better performance and functionality, avoid quickly obsolesce and more economic. There are many issues required further efforts and focus including relational data base, system configuration and operational management, various application programs. Identify priority and find an adequate measure to deal with various issues is current efforts.

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