CSNS TIMING SYSTEM PROTOTYPE

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Abstract

Timing system is important part of CSNS. Timing system prototype developments are based on the Event System 230 series. We use two debug platforms, one is EPICS base 3.14.8. IOC uses the MVME5100, running vxworks5.5 version; the other is EPICS base 3.13, using vxworks5.4 version. Prototype work included driver debugging, EVG/EVR-230 experimental new features, such as CML output signals using high-frequency step size of the signal cycle delay, the use of interlocking modules, CML, and TTL's Output to achieve interconnection function, data transmission functions. Finally, we programed the database with the new features and in order to achieve OPI.

INTRODUCTION

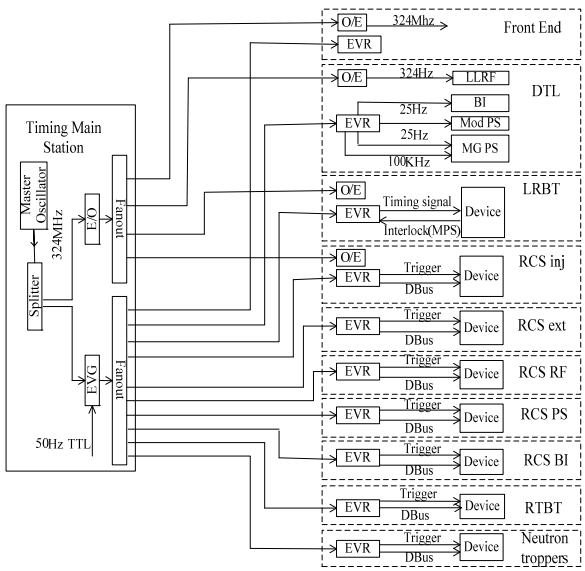

Figure 1: Timing System Outline.

The timing system using an Event system, that the event generator (EVG) and event receivers (EVR) as the main structures of a multi-level star structure(see Fig. 1), the core is EVG. The basic principle is, EVG distributed generation 8-bit parallel bus clock signal and 8-bit event codes, with 4 of 20 after a check code and / strings encoded as a stream of events, through the electro-optical conversion, optical fan-out module by and fiber (or cable) will be sent to a series of event streams EVR.EVR to receive the flow from the EVG's event to restore the 8-bit distributed bus clock signal and the 8-bit event code, and phase-locked clock generation and clock events EVG, EVR as a variety of operating reference clock. EVR can specify the port output clock signal; in the default event code EVR arrives, you can also specify the port in the pulse trigger signal output, and can produce a soft interrupt, the event code and time stamp stored in the FIFO memory with the memory can be read via the VME bus.

In BEPCII, event system has been successfully used to build a timing system, and long-term stable operation. CSNS timing system also intend to continue to use the event system[1]. Since 2004, the event system has also been upgrading , added a lot of features, the prototype of these new features was attempted. The CSNS timing system prototype provide the necessary basis for the construction of CSNS.

PLATFORMS AND DRIVER DEBUGGING

The software and hardware platforms of this experiment is as follows:

- Solaris2.8 of UNIX, mvme5100 CPU board, EPICS 3.13.8, Tornado2.1, VxWorks 5.4.2 .
- Red Hat Enterprise Linux 4, Kernel 2.6.9.Tornado 2.2.1, VxWorks 5.5.1, mvme5100 CPU board, EPICS BASE 3.14.8.2.

Modify some files of the driver，such as the routine ErCMLPat in the file drvMrfEr.c. Modify the souce code and the Db file.

HIGH-FREQUENCY STEP CYCLE DELAY

The control of the trigger delay is based on the RF cycle step (event clock = RF cycle * divide factor, of which divide factor can be 4, 5, 6, 8, 10, 12). As usual, the signal delay will be 12ns (see Fig. 2).This prototype utilize the CML output character of EVR230, of which up to 16 20-bit pattern configure register achieve the trigger delay control based on RF cycle step[2]. In fact, the maximum accuracy can be 1/(81MHz * 20)=617ps (see Fig. 3).

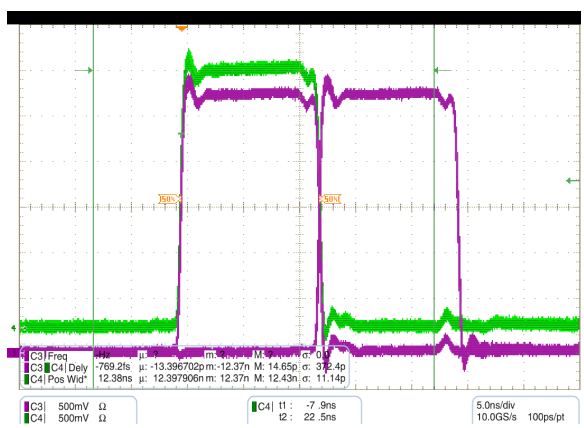

Figure 2: Delay is 12ns use common output.

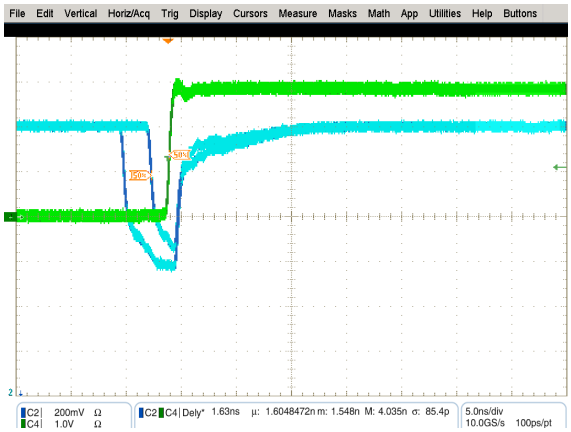

Figure 3: Delay is 600ps use CML output.

INTERLOCK FUNCTION

The event system of 230 series has interlock function. This function controls system can be used to participate and achieve with the machine protection system (MPS) of the interface. Using interface module UNIV-TTLIN, to receive electrical signals from the machine protection system, when the change occurs, the interlock signal level will become high level (see Fig. 5) from low level (see Fig. 4), the yellow signal will be closed .

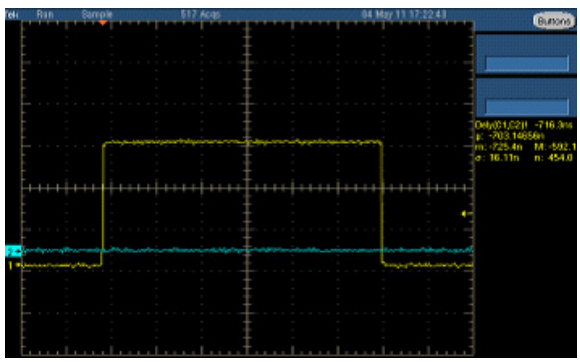

Figure 4: The blue signal is the input signal of interlock, its level is low when there are no interlocks. The yellow signal is the output of EVR.

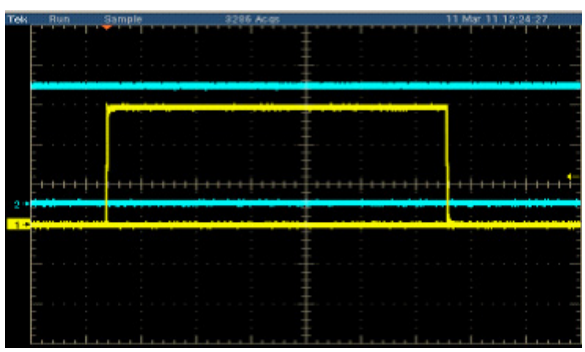

Figure 5: When the blue signal needs to realize the interlock function, it becomes high level, and the yellow signal is shutdown it just becomes low level.

DATA TRANSMISSION FUNCTIONS

The timing system prototype also considered the data transfer function, such as time-stamping, machine run mode data adn so on. EPICS-based control system can be used NTP (Network Time Protocol) to synchronize the time of each IOC. If the time granularity is the repetition period (such as J-PARC is 50Hz, U.S. SNS is 60Hz), then the timing system can be used to give each IOC to provide such high-precision time synchronization[3]. If the accelerator beam need to define some of the machine transfer mode and beam mode, in a different mode, some devices have different time charged action. We therefore need a model before the start of the model number will be sent to the running time of each site. Each time the site received mode information, to register the corresponding with different parameters, in order to achieve this mode of timing.

Data transfer operation mode is the accelerator data and time stamp and other information through the timing system to send and receive, this study we use the Swiss light source driver to Achieved. The driver contains four EPICS application: mrfApp, mrfDataBufferApp, regDevApp and generalTimeApp[4].

The four EPICS application to achieve three main functions: (1) mrfApp timing system to achieve the basic functions, which provides the trigger signal and clock signal; (2) mrfDataBufferApp and regDevApp accelerator operating mode to achieve data transmission;(3) generalTimeApp achieve timestamp (Timestamp) transmission.

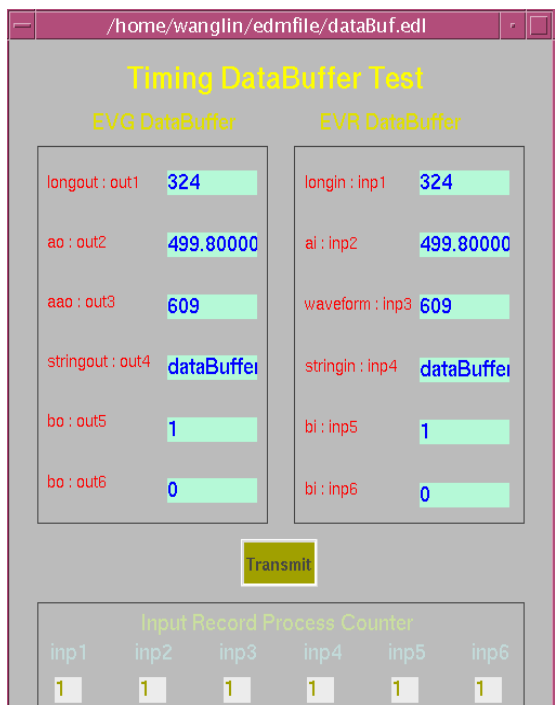

Figure 6: Data transfer test.

OPI

To facilitate the operation, in particular, produced a man-machine interface.The OPI has 4 part as shown in Figure 6 [5]. The first part is distribute bus&pulse output. The second part is CML output which showed in Figure 3. The 3rd is interlock function which showed in Figure 4. Last part is data transmission function. For the different mode, the right area will show different place which is correspond the left area.

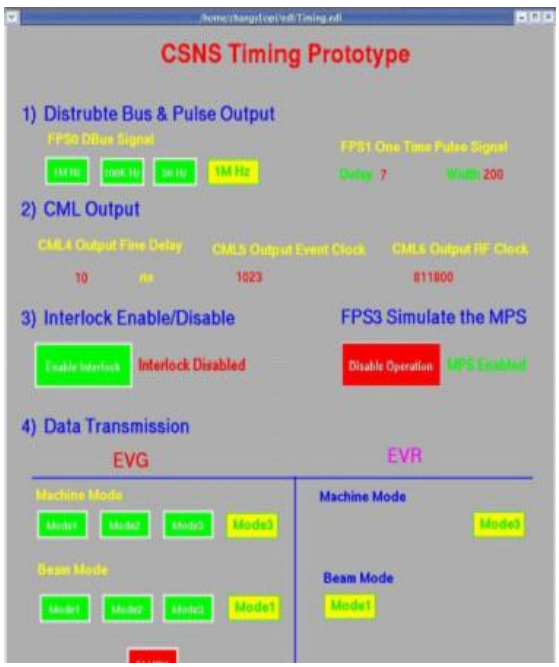

Figure 7: OPI of the prototype.

FOLLOW-UP

In CSNS,timing system is designed to provide triggers and clocks to the following systems,such as Front end, linac RF, injection, beam instrumentation, magnet power supply, RCS RF, extraction, spectrameter and target.Detailed discussions with the above systems have been done, while there are still some points need to be studied further.

REFERENCES

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