

NEW TIMING SYSTEM DEVELOPMENT AT SNS*

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Abstract

The timing system at the Spallation Neutron Source (SNS) has recently been updated to support the long range production and availability goals of the facility. A redesign of the hardware and software provided us with an opportunity to significantly reduce the complexity of the system as a whole and consolidate the functionality of multiple cards into single units eliminating almost half of our operating components in the field. It also presented a prime opportunity to integrate new system level diagnostics previously unavailable for experts and operations. These new tools provide us with a clear image of the health of our distribution links and enhance our ability to quickly identify and isolate errors.

INTRODUCTION

The Timing System at SNS is based on the dual timing system architecture used at the Relativistic Heavy Ion Collider (RHIC) at Brookhaven Nation Laboratory (BNL) [1]. The first system is a beam synchronous system that distributes and correlates specific tasks that are used in the production of the beam pulse. It produces a bi-phase mark encoded signal to embed the ring RF clock with the event scheduling data to provide remote platforms with a reference in which local PLLs can lock to and derive references that are synchronized to the ring frequency. This system was altered slightly to meet the specific requirements at SNS to synchronize the 60 Hz operation of the LINAC and neutron choppers to the accumulator ring [2]. The second system or Real Time Data Link (RTDL) serves as a general purpose information distribution network. It globally broadcasts information across a unidirectional link about each beam pulse. The delivery of this data only has to occur within a specified range of time and is not required to be correlated to the ring frequency and is therefore asynchronous to the ring RF source.

The hardware delivered by BNL can no longer be reproduced as many of the components have reached their end of life cycle. This makes it impossible to support the existing architecture for any extended period of time. A hardware redesign is required in order for us to effectively support the long term availability goals of the facility. This has provided us with an ideal opportunity to simplify our system architecture and focus on decreasing our maintenance overhead by integrating the functionality of multiple components into a single units and making system diagnostic capabilities available at each node.

TIMING MASTER HARDWARE

The Timing Master Hardware achieved the largest gains in reducing individual component design complexity by integrating both of the RHIC timing systems into a single VME card [3]. The previous platform requires multiple sets of hardware components that span across 2 VME crates using a VME bridge [4].

Event Timing

The RHIC beam synchronous system that generates the machine cycle sequence events across the Event Link (EL) requires 4 Trigger modules that produce reference pulses to 4 Event Input modules that are connected to a single Event Link Encoder module using a special adaptor cable that bridges the user defined pins of the P2 connector. The functionality of these 9 cards now resides within the SNS Timing Master Hardware.

The 4 Event Input modules produce all of the fixed or hard events that are used in the production of the beam pulse. The number of fixed events is limited to 64. This restriction is imposed by the Input modules which are only capable of generating 8 events per node. Special care must be taken when setting up this system to prevent Event Jostle. This occurs when 2 or more of these modules try to fire an event at the same time. The generation of soft or floating events must be held off by the IOC during the period of time when beam events are active to ensure they do not cause additional scheduling conflicts while the fixed events are in the process of being broadcast on the EL.

The SNS design utilizes a local memory to store the hard events. It has a depth of 16k address locations. There are only 255 usable events available in the SNS Timing System; therefore, the majority of the memory locations are unused. The Timing Master hardware maintains a counter that represents the current turn count within the machine cycle production period. A turn is defined as the amount of time it takes for the beam to travel around the SNS ring 1 time. There are approximately just over 17k turns in a given SNS machine cycle. This counter is used as an address pointer to the hard event memory. When a non-zero value is returned from a particular address location soft event requests are queued and held off until a conflict is no longer present. The machine specific event numbers are stored in memory locations that correspond to a given turn in the machine cycle when they are scheduled to be broadcast on the event link. Additional events are allowed to pass through the system at anytime there is not a machine specific event scheduled for production. The

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possibility of Event Jostle is completely eliminated in this architecture as there is only a single source of the hard events, and the processing of soft events are postponed and queued by the hardware when the address pointer returns a non-zero value. This also allows the IOC to schedule the soft events at anytime within the machine cycle as it is no longer restricted to non-beam production periods. Mapping the fixed events into memory also allows the new system to define any number of the 255 events as either hard or soft events. It is no longer restricted by the Event Input module limitations.

Data Link Timing

The RHIC RTDL hardware requires a single RTDL Encoder and multiple RTDL Input Modules. Each Input module is only capable of producing 8 frames. The encoder and input modules also require a special adaptor cable to bridge the user defined pins of the P2 connector. The protocol defined for the RTDL restricts the unique number of data packets it is capable of transmitting to 256 frames. The SNS system has been configured to broadcast 128 frames of data. This architecture would require a third VME crate if the SNS requirements were updated by adding additional frames above the current 128 that are presently defined and would require installing a 3rd VME crate as a total of 32 Input modules are needed to populate 256 frames.

The SNS Timing Master design eliminated the need for the encoder and input modules. This was handled in a similar fashion to the EL by mapping these frames into a separate local memory bank; however, unlike event driven timing system, this memory only needs to be large enough to contain all 256 frames. The IOC updates values in the RTDL between machine cycles. The RTDL section is processed by the hardware when it observes and RTDL valid event from the IOC. The hardware then processes the entire RTDL table and only queues the frames that have been updated by the IOC. After the table has been processed, the hardware clears the frame table to prevent stale data from being rebroadcast across the link.

TIMING RECEIVER HARDWARE

The most significant achievement in simplifying the overall system architecture was accomplished in the redesign of the Timing Receiver Hardware [5]. The RHIC Trigger Module [6] and the Utility Module [7] were integrated into a single VME card. This has the highest impact on reducing the total number of supported operating components in the field as a large portion of the subsystems utilize both sets of this hardware platforms.

Trigger Module

The primary function of the Trigger Module is to support the SNS subsystems that are responsible for the production of the beam pulse by producing machine cycle specific reference pulses that are synchronous to the ring RF clock. These cards contain local PLLs that derive

reference clocks from the bi-phase mark encoded event link generated by the Timing Master hardware at 32x the ring frequency.

These cards contain 8 front panel trigger reference outputs that can be configured independently to produce reference pulses to any of the 255 predefined SNS events. These pulses can be delayed from the start of an event using 1/64 increments of the ring RF frequency for systems that require alignment with the head or tail of the beam pulse within the accumulator ring.

Utility Module

The Utility Module provides the IOC with cycle to cycle information about each beam pulse that is extracted from the RTDL. The module will interrupt the IOC after receiving an RTDL valid event from the Timing Master on the EL. This notifies the processor that the table has been updated and is ready for any user applications that require this information. It also serves a platform for generating additional interrupts to the IOC when specific events have been observed on the EL or an error was observed on the event or real time data links.

System Diagnostics

One of the major challenges with the previous Timing System is determining the existence of and isolating transmission errors. The modules will notify the processor that an error exists; however, it provides very few details about the error. Additional information must be acquired by adding additional VME cards to the configuration.

The new Timing Receiver Hardware incorporates detailed diagnostics for both of the timing links within the hardware design. It utilizes 2 different memory banks that store the observed events from the EL and the frames from the RTDL for each machine cycle. The processor is interrupted only if this feature has been enabled in the hardware. This allows us to field diagnostic tools with every module without running additional application overhead if the diagnostic tool is not needed.

TIMING DISTRIBUTION NETWORK

The SNS Timing Distribution Network also suffers from component availability issues. This hardware redesign has also been modified from the original equipment that was delivered to SNS. This includes changes that actually complicated the design slightly; however, the functionality remains the same. Special care was taken to ensure the health monitoring equipment does not impact the operation of the distribution network should it experience a failure.

The overall distribution architecture was revisited. The previous distribution method performs multiple media conversions prior to reaching its final destination. This adds additional unnecessary jitter to the distributed signal that is received by the end components in the field making it difficult to perform high resolution beam reference measurements. The new design retains the

information on fiber links until it reaches the end point before converting it into an electrical signal.

The new hardware takes advantage of using hot swappable SFP modules and includes an additional new set of diagnostics that allows us to perform health checks of the links at the fan-out modules. This gives us an opportunity to perform preventative maintenance checks during scheduled maintenance periods.

CONCLUSION

By simplifying the system architecture, the SNS Timing System is easier to manage and has significantly fewer active components that are likely to fail. The addition of diagnostics at each node allows us to isolate and identify failures remotely and more rapidly than before. These changes also allow us to incorporate preventative maintenance routines into our scheduled maintenance periods and provide us with the opportunity to address failures before they impact accelerator operations.

Allowing the hardware to manage more of the overhead task allows a number of the IOC responsibilities to be reduced and simplifies the design of the software as well. A fair number of the tasks have been reduced to simply updating a handful of registers in the timing hardware.

The integration of our hardware components has allowed us to remove 8 different types of VME cards from our inventory and combine their functionality into just 2 cards. The Timing Master VME crate previously spanned across two 11U 21 slot VME crates. It now occupies a single 4U 9 slot crate. We have also managed to eliminate approximately 150 active VME cards from our operating environment.

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