BPM SYSTEM AND ORBIT FEEDBACK SYSTEM DESIGN FOR THE TAIWAN PHOTON SOURCE

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Abstract

Taiwan Photon Source (TPS) is a 3 GeV synchrotron light source which is being in construction at NSRRC. The BPM electronics with the latest generation FPGA and new mechanical form factor to enhance functionality of current generation products will be employed for the TPS. The prototype BPM electronics is testing. To achieve the stringent orbit stability goal of the TPS, orbit feedback system is designed to eliminate beam motions due to various perturbation sources. The design and implementation plan of the BPM system and the orbit feedback system are summarized in this report.

INTRODUCTION

The TPS [1] is a latest generation of high brightness synchrotron light source which has been under construction at the National Synchrotron Radiation Research Center (NSRRC) in Taiwan since 2010. It consists of a 150 MeV electron Linac, a 3 GeV booster synchrotron, and a 3 GeV storage ring. The design of the storage ring has 24 cells. There are 7 BPMs and 7 horizontal/vertical correctors are winding on the sexupoles in each cell. Current generation state of the art BPM electronics is designed and delivered more than 5 years ago. To avoid obsolesce of the components, to take advantages of advanced devices and enhance functionality, it was decided to adopt new design of BPM electronics. To satisfy stringent orbit stability requirement of the TPS, low noise corrector power supply system, and orbit feedback system are also designed.

STORAGE RING BPM AND CORRECTOR LAYOUT

The design of the storage ring has 24 cells, each cell equipped with 7 BPMs and 7 horizontal/vertical correctors are winding on the sexupoles in each cell. The lattice layout is as Fig.1. The locations of BPM and correctors are to satisfy DC orbit correction under the constraint of installation space. Since vertical beam size at centre of straight section for insertion devices is around 5 μm in sigma, better than 0.5 μm beam stability are required. To meet the tight orbit stability requirement, an orbit feedback system is indispensable. Standard correctors are side winding on the sextupole magnets. These kinds of correctors could provide about 500 μrad kick while their bandwidth could be limited only several tens of Hertz due to the eddy effect of the alumina vacuum chamber. The vacuum chamber is 4 mm thick elliptical chamber with 30 mm and 60 mm in minor axis and major axis respectively. Due to eddy current effect, the possible bandwidth in horizontal and vertical plan is around several tens Hertz. This bandwidth is not sufficient to eliminate perturbation below 100~200 Hz. Therefore, extra four horizontal/vertical correctors per cell will be installed on the bellows site as shown in Fig. 1 to obtain higher correction bandwidth. These correctors have fast response but smaller kick strength around 30 μrad. Thus the orbit feedback system plans to use two kinds of correctors simultaneously. The DC component of the fast correctors will transfer from fast to slow correctors smoothly and avoid saturation of the fast correctors as well as provide capability to suppress orbit drift.

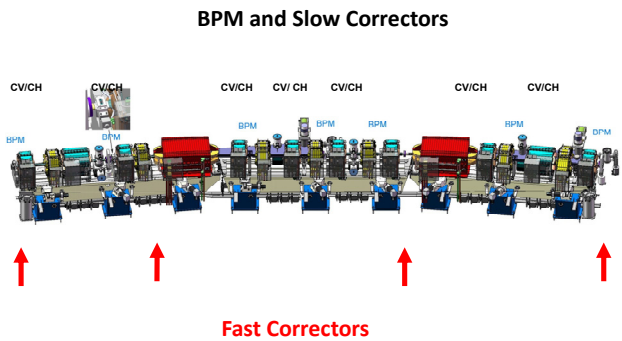

Figure 1: The slow (winding on sextupoles) and fast correctors layout in one cell of TPS storage ring.

BPM SYSTEM

BPM Electronics

The TPS BPM electronics was contracted to the Instrumentation Technologies in May 2011 for the Libera Brilliance+ as BPM electronics which is the latest member of the Libera family. The family covers the requirements of wide variety of the circular light source machines [1]. The BPM electronics delivers unprecedented possibilities for either building powerful single station solutions or architecting complex feedback systems. New electronics allows even more extensive machine physics studies to be conducted due to large data buffers and the new true turn-by-turn position calculation. There are 168 BPM units at the storage ring except some special BPM at straight sections. All 168 BPM electronic modules will installed at 48 BPM platforms. The first field tests of the new product had been performed on real beam at Taiwan Light Source (TLS) [2, 3] to test validation for the usage for the TPS. Figure 2 shows the tested installation.

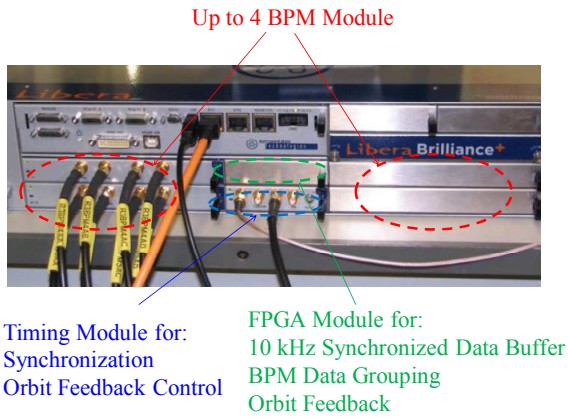

Figure 2: Libera Brilliance+ installation in the TLS.

Intensive test for performance and functionality were performed for the prototype to ensure that the new electronics satisfy the requirement of TPS. The test combined by using simulated signals from signal generator as well as real beam of the existed 1.5 GeV synchrotron light source. The long-term stability has been tested for bench measurement where input power level was set to several power level between -20 dBm to 0 dBm. Position stability is around 100 nm in rms for both planes for one day record. The temperature dependence has also been tested and almost could be ignored while ambient temperature was controlled within ± 0.1˚C. The resolution of FA data at 10 kHz meet specification where σ x and σ y is less than 150 nm. Besides, turn-by-turn data has been achieved 10 μm resolution for short bunch train.

The real beam tests at the TLS have also been performed. SA and FA reading had been acquired and analyzed for the stored beam. Current dependency affects position variation could be within 3 um from 30 mA to 360 mA. The instrument also possesses a useful feature which provides two approaches to process from ADC data to turn-by-turn data. One is classic DDC approach; another is time domain processing (TDP). This functionality is useful for peculiar filling pattern.

The preliminary testing ensures that the Libera Briliance+ BPM can meet the requirement of TPS storage ring. To simply the complexity, the same platform will adopt for the booster synchrotron also. There are 60 BPM units at the booster synchrotron. All 60 BPM electronic modules will be installed at 24 BPM platforms around the 24 CIAs.

BPM Data Access and Grouping

There are several data format flows are provided by the BPM platforms with EPICS interface, include of 10 Hz rate data for DC closed orbit correction, turn-by-turn data with software/hardware trigger and on demand access for accelerator physics study, streaming 10 kHz fast data for orbit feedback application. The fast data is also very useful for beam diagnostic.

The BPM platform is composed of a COM Express CPU module running Linux to control up to 4 BPM modules. Embedded EPICS server on this module could deliver 10 Hz rate access of BPM information, includes matrix elements of the orbit feedback system as well as handle the basic configuration.

A GDX FPGA module will be installed at the BPM platform to support 10 kHz synchronized data buffer for 4 BPM modules, and group with the other BPM platforms for the whole storage ring together. The fast orbit feedback control and fast corrector interface protocol are also processed in this module. There are four SFP ports on the front plane. There are several LVDS links in the BPM modules that can collect all ring BPM data with 10 kHz rate. The data is through the bi-directional multi-gigabit links to the adjacent nodes. Each FPGA module will serve as one node of the BPM grouping around the ring. We refer to this functionality as BPM grouping. The communication of the grouping is done by two SFP ports. The bitrate of the grouping can be up to 6.25 Gbit/sec. One of the remained SFP port will be used as fast corrector control interface with AURORA protocol. The last SFP port will provide functionality for grouping data output either use AURORA protocol or UDP/IP protocol, to support the slow corrector control or the diagnostic related application. The Ethernet packet supports jumbo frame to satisfy all BPM data grouping. Due to BPM data grouping and orbit feedback control use the same FPGA module, orbit feedback is also part of BPM platform.

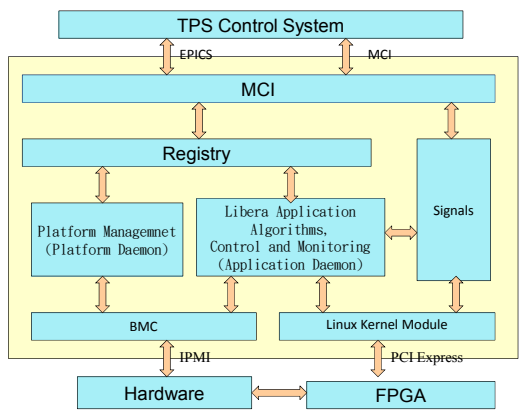

Figure 3: BPM platform software structure.

BPM Platform Software Structure

BPM platform software is organized in a few layers, see fig 3. In the bottom layer there are BMC library and Linux kernel module which communicate with FPGA and hardware through IPMI (Intelligent Platform Management Interface) and PCI Express respectively. On the top of that there is signal processing library and the application daemon for control and monitor algorithms processing. Beside application there is also platform management (Platform Daemon), which is responsible for monitoring health status of the hardware. The application and

platform daemon communicate with outer world through the MCI (measurement and control interface) which uses registry and signal library underneath for accessing application properties, signals, changing the application behavior, etc. On the top of MCI various adaptors to different control systems can be implemented [4].

ORBIT FEEDBACK SCHEME

The TPS aluminium vacuum chamber of storage ring is 4 mm thickness that prevents fast orbit correction by standard correctors in both planes which are back winding on 168 sextupole magnets. In order to satisfy fast orbit feedback request, 96 sets of fast corrector at bellows site are added. So, the TPS orbit feedback system is a global orbit feedback system combined fast and slow corrector in one system.

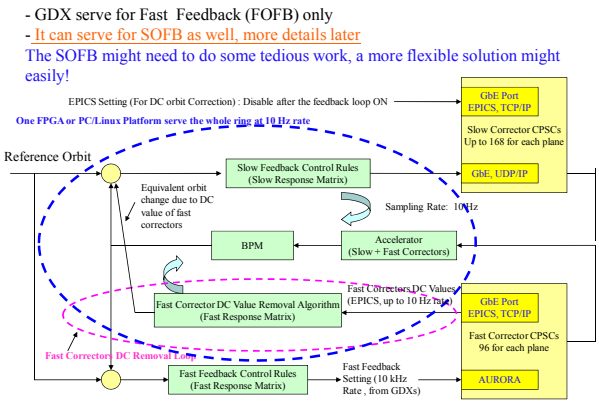

Figure 4: Control infrastructure in one cell of TPS storage ring power supplies.

Orbit Feedback Infrastructure

The infrastructure configuration of orbit feedback with fast and slow corrector is shown in Fig. 4. There are 24 cells in the TPS storage ring. Each cell will be equipped with two BPM platforms which can accommodate 7 BPM electronics at Phase I. Each BPM platforms has a slot which can allocate an FPGA module used for communication with the other module in other cells as a clockwise and counter-clockwise multi-gigabit redundancy link to group BPM data for the whole ring. Two FPGA modules of each cell will handle fast orbit feedback control algorithm and control 4 fast correctors in horizontal and vertical plane respectively. Correctors are controlled by a custom designed Corrector Power Supply Controller (CPSC) of each cell [5]. The CPSC module will be installed at slot of power supply crate to control up to 8 modules in the same chassis. At each cell, there are three CPSC modules installed at three power supply crates include of horizontal slow correctors (7 PS modules), vertical slow correctors (7 PS modules), and combined horizontal (4) and vertical (4) fast corrector. Fig. 4 shows

Besides fast correctors computation executed in FPGA modules, the slow corrector control will be handled by general purpose CPU. It would acquire the BPM grouping data through the rest SFP port of FPGA module configured as Gigabit Ethernet. The slow corrector will be controlled with 100 Hz update rate and be delivered at phase I to keep from fast corrector saturation. The slow corrector setting rate is expedited that is possible in the future. The possible candidate platform would be aTCA.

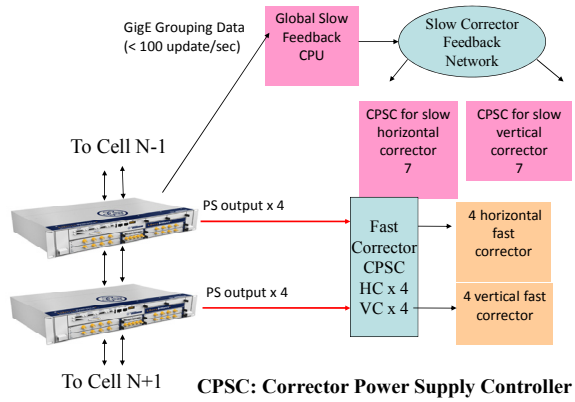

Figure 5: Configuration of global orbit feedback for corrector power supply.

Corrector Power Supply and its Control Interface

Fig. 5 shows the small power supplies applied for both slow and fast correctors and skew quadrupoles. There will be 8 power supply modules in one crate and the most left slot will be plugged in one CPSC. Besides general control, monitor and configuration, the fast correctors will be also applied for the fast orbit feedback. The CPSC with EPICS IOC is therefore dedicatedly designed and the embedded FPGA will handle fast update application. Built-in waveform and synchronization mechanism are also supported.

The power supply for both fast and slow corrector magnets in the range of ±10 Amp will be controlled by analogue interface directly. The CPSC is dedicated to be designed for both EPICS control system and fast orbit feedback application which is based on AURORA of Xilinx to support high speed communication and control. Fig. 6 shows the corrector power supply crate which includes 8 power supply modules and one CPSC at the most left slot. The CPSC with EPICS IOC is dedicatedly designed and the embedded FPGA will handle fast update application. Synchronization mechanism and built-in waveform are also supported. The setting reference of the corrector power supply is generated by 20 bits DAC and readback is from 24 bits ADC. This controller is also a embedded EPICS IOC for slow control. Fast setting ports are to receive fast data from orbit feedback module (GDX).

Control Rules Scheme

The response matrix R_s and R_f, which relates the orbit shifts to the slow and fast correctors respectively could be decomposed by singular value decomposition (SVD) as Eq. 1 and Eq. 2.

$$R_s^{+} = V_s \Sigma_s^{+} U_s^{T} \quad (1)$$

$$R_f^{+} = V_f \Sigma_f^{+} U_f^{T} \quad (2)$$

where R_s is 168×168 matrix; R_f is 168×96 matrix. These two loops of correction are operated at different platform but shared the same BPM data streaming. As well as the other light sources, to avoid saturation of fast correctors and counteraction of fast and slow loop, the different controllers would be applied for two loops respectively to separate the working frequency domain.

Figure 6: Corrector power supply crate. There are 8 power supply regulation modules in one crate and the most left slot will be plugged in one CPSC.

Fast Orbit Feedback Loop

The fast orbit feedback loop will be performed in the GDX FPGA modules in the distributed manner; each FPGA module control four fast correctors. The matrix elements download and feedback parameters will be done by the EPICS IOC located at the platform of the GDX FPGA module. All feedback loop of platform will be synchronous by grouping and external signal, such as feedback on/off.

Slow Orbit Feedback Loop

The slow orbit feedback loop processing will use PC running Linux. The individual BPM and fast corrector setting value in each cell will be combined in the local net, and transfer to a waveform type of EPICS interface to satisfy software real-time access request for slow orbit feedback control. The CPSC is also EPICS IOC that will receive slow setting value from typical EPICS interface or UDP packet port. Each CPSC module would extract their setting data by specific address within the packet.

Communication between Fast and Slow Orbit Feedback Loop

The plan FOFB system will working down to DC. A slow system will have to read the DC part of the current in the fast corrector from the CPSC module and transfer it on the slow correctors by multiply inverse of the slow transfer matrix. The two systems would not be independent; a reliable communication needs to be implemented between them. The main advantage of this solution is to reduce beam movements in the whole frequency range. This scheme were high successful in ALS and Synchrotron Soleil [6, 7].

SUMMARY

The design of the BPM system and corrector power supply system were performed for the TPS storage ring. The BPM electronics contract to the vendor in June 2011. All BPM electronics will be delivered in late 2012. Orbit feedback FPGA module is in call for tender process. Corrector power supplies will be delivered in later 2012 also. System integration is scheduled in 2013. Full scale test of the system will be possible in late 2013. Test with beam will be possible in 2014. Preliminary test for the system will be possible in 2013. All necessary hardware and software are in preparation.

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