# COMPACTPCI EXPRESS FOR CONTROL APPLICATIONS

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*Abstract*

CompactPCI (CPCI) is well established in control applications as a standard for industrial PCs and as a standard for front-end instrumentation, e.g. by means of the transparent optical PCI/CPCI Bridge MXI-4 from National Instruments. In both application areas increasing performance requirements ask for a replacement of the parallel CPCI bus by a backplane based on high speed serial links, similar to the replacement of PCI by PCIe in the desktop environment. CompactPCI Express and its derivative PXI Express both provide a smooth and cost-efficient transition path from CPCI to high speed serial links on the backplane.

Forschungszentrum Jülich has developed a CompactPCI Express carrier board for CMC daughter modules that is compatible to the SIS1100-CMC/cCMC boards from company Struck Innovative Systeme. The CompactPCI Express carrierboard is based on a single lane PCIe implementation with the PEX8311 bridge ASIC from PLX. A development environment has been setup, that consists of crates from Schroff, CPUs from MEN and the transparent electrical PXI Express to PCIe bridge MXI-Express from National Instruments. The design and application of the new board as well first experiences with the new technology are presented.

## INTRODUCTION

Originally driven by the Telecom industry, the PICMG standard CompactPCI (PICMG 2.0) [1] is now well established in many areas, e.g. military, industrial automation or medicine. Main reason for this success is the combination of the popular Eurocard format with the standard PC bus PCI. The use of PCI guarantees software compatibility with commodity PCs and a low effort is required to redesign standard PCI boards as CompactPCI boards. CompactPCI is also very popular in research. Since many years Forschungszentrum Jülich is using CompactPCI for control systems of large experiments, as pointed out in the next section.

The increasing need for bandwidth is leading to a replacement of classical parallel bus systems by high speed switch serial switch fabrics like PCI Express (PCIe), InfiniBand, RapidIO or Gigabit-Ethernet. PCIe now is the de facto replacement of PCI in the commodity PC market. For modular board systems several standards employing the above switch fabrics have been defined:

The VME International Trade Association VITA [2] developed the standards VXS (VITA 41) and VPX (VITA 46). VXS is downward compatible to VME. VPX is a more cost efficient approach completely incompatible to VME.

The PCIMG standardized ATCA (PICMG 3.x) and MicroTCA (PICMG MTCA.0) . ATCA was mainly driven by the Telecom industry. MicroTCA is a more cost efficient spin off from ATCA based on AMC, the ATCA mezzanine card standard. With company National Instruments as the main driving force, PICMG also defined CompactPCI Express (PICMG EXP.0) as a downward compatible extension of CompactPCI. On the initiative of several vendors of CompactPCI CPUs, PICMG has started a new not yet finished standardization activity for the CompactPCI Plus standards PICMG 2.30 PlusIO and CPLUS.0. CompactPCI Plus also aims at a follow up system to CompactPCI, which is downward compatible. As a consequence, CompactPCI Plus is a direct competitor of CompactPCI. CompactPCI Plus defines also USB, SATA and Gigabit Ethernet links on the backplane, The system and peripheral slots are incompatible to Compact PCIexpress, but hybrid peripheral slots are foreseen that also support CompactPCI Express Type 2 Peripheral boards. The version CompactPCI PlusIO defines a system slot that is compatible to CompactPCI.

Taking into account that each of the above standards defines several board form-factors and backplane communications protocols, now a multitude of competing solutions are existing leading to a severe segmentation of a small market. It can be anticipated that only a few options will survive, so for the user it is a major risk to invest into one of these technologies.

## COMPACTPCI IN CONTROL APPLICATIONS AT FORSCHUNGSZENTRUM JÜLICH

CompactPCI is being used at Forschungszentrum Jülich since 1996 in several research areas. Reasons are compact, robust and ruggedized mechanics, good cooling, easy replacement of modules plus external cabling and the long lifecycle of components while maintaining software and silicon compatibility with the commodity PC market at the same time. Another reason is the good support by vendor National Instruments (NI), which defined PXI (PCI eXtensions for Instrumentation) as an extension of CompactPCI for measurement applications by providing additional signals for timing, clocks and triggering. Very popular in Jülich is the NI product MXI-4 which allows PC control of remote CompactPCI crates – e.g. with detector electronics - via an optical serial link.

Typical examples for the application of CompatPCI are the control and data acquisition systems for Neutron scattering instruments. All the Neutron instruments developed in Jülich are based on the TACO control system and the TACO device servers typically run on CPCI-based server systems, to which all peripheral systems are connected, as shown in Fig. 1 [3].

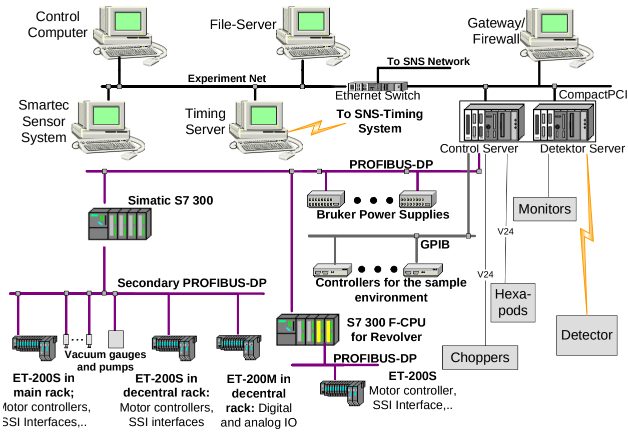


Figure 1: Control- and DAQ-System of the Neutron Spin Echo Spectrometer at the SNS.

In many cases also the detector electronics is contained in a remote CPCI system as shown in Fig. 2.

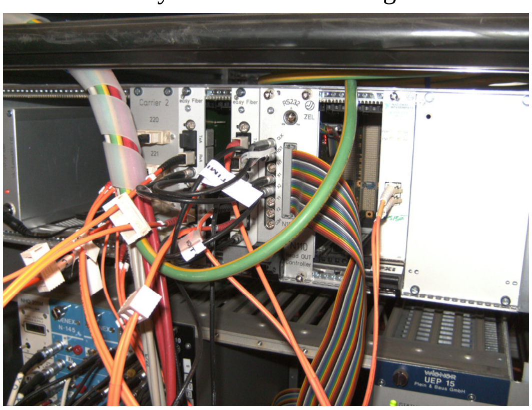

Figure 2: Detector electronics CompactPCI system of the Neutron Spin Echo Spectrometer at the SNS.

In order to fulfil a variety of different instrument requirements, a modular system of carrier boards and mezzanines has been developed in cooperation between the company Struck Innovative Systeme (SIS) and ZEL, the central electronics lab of Forschungszentrum Jülich.

Carrier boards exist for CompactPCI, PCI and PCIe and are commercially available from SIS as SIS1100-cCMC, SIS1100-CMC and SIS1100-eCMC.

All carrier boards have the same basic architecture. They are equipped with a Xilinx FPGA (Spartan or Virtex series) which are programmed for the dedicated application function. Most IO-pins of the FPGA are connected to a CMC connector which holds an application-specific mezzanine card. The connection to PCI or PCIe is implemented with a bridge ASIC from PLX (PEX8311 or PCI9054) providing a 32bit parallel bus connected to the FPGA. For special memory intensive applications also specific CompactPCI carrier boards with additional static RAM have been developed.

Application specific mezzanines are available for Counter/Timer functionality, readout of multiwire proportional chambers, time-to-digital converters, Hotlink, a optical serial link to VME (SIS1100-OPT), etc.

## OVERVIEW OF COMPACTPCI EXPRESS

CompactPCI Express combines the Eurocard format with PCIe, the standard serial interconnect fabric for PCs. It defines point-to-point full duplex links on the backplane with up to 16 lanes. Each lane has a nominal bandwidth of 2Gbit/s in each direction. As a consequence CompactPCI Express achieves a major increase of backplane bandwidth as well as software and silicon compatiblity with recent developments in the consumer PC market.

An additional goal of the standard is backward compatibility and smooth transition to CompactPCI [4], [5]. Software compatibility to CompactPCI is a direct consequence of using PCIe. Additionally, legacy CompactPCI modules can be plugged into CompactPCI Express systems, as shown in the next paragraphs.

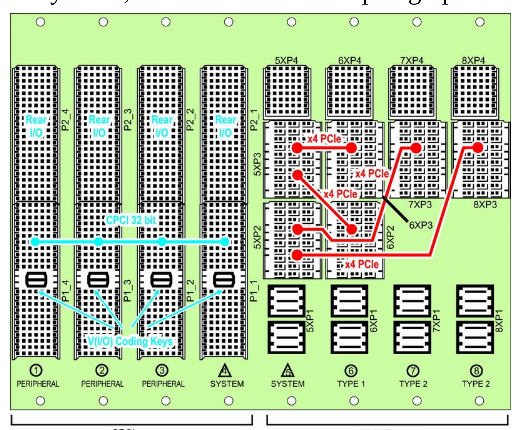


Figure 3: Combined CompactPCI / CompactPCI Express backplane from Schroff.

CompactPCI Express defines a tree topology on the backplane with optional PCIe switches. There may be subordinate PCI buses on the backplane supporting legacy CompactPCI modules. The connection to these PCI buses is done via bridges on the backplane, by bridge modules in Hybrid Peripheral Slots or by rear IO bridge module. Another possibility is the use of CompactPCI CPUs with a CompactPCIe side board, e.g. available from companies MEN or EKF. As shown in Fig. 3, company Schroff provides such a backplane, which is used also in our test installation at Forschungszentrum Jülich. Six types of backplane slots are defined:

- The **System slot** should contain the PCIe root complex and may have four PCIe links with up to 4 lanes or two PCIe links, one with up to 8 lanes and one with up to 16 lanes. Typically the system slot is the root of the tree structure on the backplane. It is intended for CPUs.

- The **Type 1 Peripheral Slot** supports two PCIe links, one with up to 8 lanes and one with up to 16 lanes.
- The **Type 2 Peripheral Slot** supports only one PCIe link with up to 4 lanes.
- There may be an optional **Switch Slot**, in order to achieve even higher bandwidth. In this case the switch slot is the root of the tree structure on the backplane.
- In a **Hybrid Peripheral Slot** legacy CompactPCI modules or Type 2 Peripheral modules can be plugged.
- **Legacy Peripheral Slots** are intended for legacy CompactPCI modules.

For measurement applications the PXI Systems Alliance developed the PXI Express standard by extending CompactPCI Express with the definition of additional signals for timing, clocks and triggering, similar to PXI.

Today a variety of CPUs, crates, interconnects to PCs and peripheral modules are available from companies like National Instruments, Schroff, Elma, MEN, EKF, One Stop Systems, EMtrust, etc.

## COMPACTPCI EXPRESS DEVELOPMENTS AT FORSCHUNGSZENTRUM JÜLICH

Readout of detectors via electronics in front-end CompactPCI crates is limited in bandwidth by the PCI bus on the backplane and the serial optical uplink MXI-4. CompactPCI Express is an attractive system to overcome these limitations, since it provides a major increase in bandwidth and allows a smooth transition from CompactPCI. Also development effort and system costs are much lower than with other technologies, e.g. MicroTCA. CompactPCI Express CPUs and crates are available for about the same price as comparable CompactPCI components.

So we decided to invest into CompactPCI Express. We did not take CompactPCI Plus into account, since the standard is not yet finished and the product situation is still unsatisfactory. A further argument for CompactPCI Express is the existing broad range of peripheral boards from National Instruments and the serial electrical connection MXI-Express to commodity PCs which can achieve a bandwidth of up to 832 Mbytes/s.

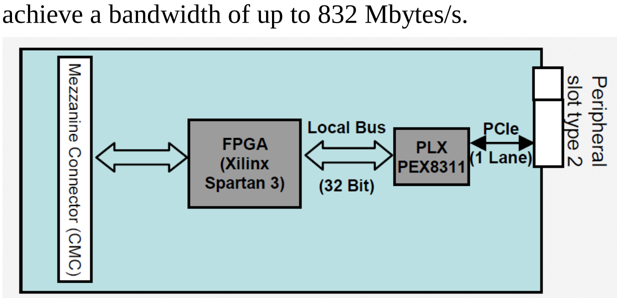


Figure 4: Blockdigram of the new carrier board.

As a natural first step into the CompactPCI Express technology we extended our above-mentioned family of carrier boards by developing a corresponding Type 2 Peripheral carrier board. Fig. 4 and Fig. 5 show block diagram and photo of this new module. The PCIe link with 1 lane is implemented by the PLX PEX8311 bridge ASIC, that maps PCIe to a 32bit parallel host bus connected to the FPGA.

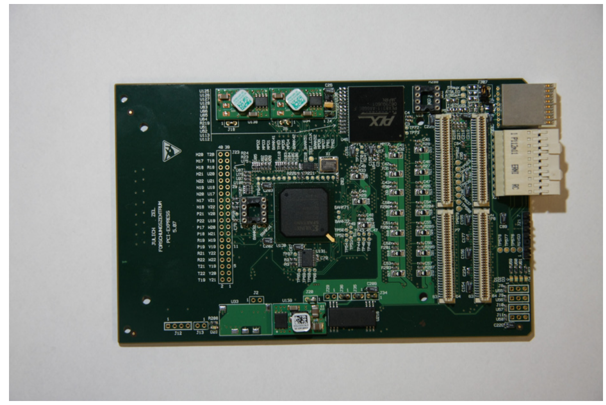

Figure 5: Photo of the new carrier board.

As development platforms we bought two Crates from Schroff with the backplane shown in Fig. 3. One of the crates is equipped with a MEN F17 CPU and the F602 CPCIe sidecard. The other crate is equipped with a MXI-Express uplink to a commodity PC. As reference module we use the digital and analog IO module PXIe-6251 from National Instruments, which is a Type 2 Peripheral board.

We successfully tested our new carrier board together with the MEN CPU. Unfortunately the board does not get recognized by the MXI-Express link. We are still investigating this problem and suppose some incompatibilities to PXI Express. After solving this problem we will do performance measurements.

## REFERENCES

[1] PCI Industrial Computer Manufacturers Group PICMG, www.picmg.org.

[2] VME International Trade Association VITA, www.vita.com.

[3] H. Kleines et al., “Implementation of the Control and Data Acquisition Systems for Neutron Scattering Experiments at the New “Jülich Center for Neutron Science” According to the “Jülich-Munich Standard”, Proceedings of the ICALEPCS 2005, Geneva, 2005.

[4] V.Andrew, “CompactPCI/PICMG standards on the Move: A look at CPCI Express”, RTC Magazine, January 2007; pp. 22.

[5] Steve Cooper,”High performance view: CompactPCI Express”,CompactPCI and ATCA systems magazine, August 2006, http://www.compactpci-systems.com/articles/id/?1846.