

MAGNET POWER SUPPLY CONTROL SYSTEM USING “I-DIO” FPGA PROGRAM IN A VME FIELD BUS CARD

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Abstract

A VME optical link remote IO module system (i-DIO card) has been developed and tested for a two channel enclosed magnet power supply of the XFEL/SPring-8. An FPGA in the i-DIO card is used for current deviation monitoring and local control. In this paper, the magnet power supply control system of the XFEL/SPring-8 project is summarized.

INTRODUCTION

The XFEL/SPring-8 project has been started since 2006 and the building was already completed in March 2009 [1, 2]. The installation of accelerator and undulator components will be finished by the summer of 2010. The first production of magnet power supplies (PSs) was already delivered to the SPring-8 site and the performance and control system are now being tested.

MAGNET POWER SUPPLY

The XFEL/SPring-8 uses 13 groups of magnet PSs depending on output type, current and voltage (Table 1). Transistor dropper control is employed for the small PSs and FET or IGBT PWM control is used for the large PSs. There are three types of current regulation, that are unipolar, bipolar, and four-quadrant.

One PS control interface module (i-DIO) has 64bit DO and 64bit DI, and it can control two PSs. Therefore most of the small PSs are enclosed by two sets in one chassis, which are used for horizontal and vertical steering magnets and quadrupole magnets. In order to decrease noise, the i-DIO card is installed in the PS chassis (Figure 1). The card can be easily inserted and removed for maintenance.



Figure 1: Front and top view of 2-channel type magnet power supply. The “i-DIO” is inserted from the rear panel.

Power Supply Specification

Table 1 shows the PS groups together with output current and voltage. The initial letters U, B and AUX

correspond to unipolar, bipolar and four-quadrant output types. LINAC and MS-Und indicate the installed locations in the facility, corresponding to the 8 GeV accelerator and the undulator respectively.

Table 1: Group, Specification and Amount of PSs

PS GROUP	Current and Voltage	LINAC	MS-Und.	Total
U1	3A, 4V	12	0	12
U2	5A, 5V	16	0	16
U3	11A, 7V	17	60	77
U5	20A, 17V	13	0	13
U6	20A, 42V	2	0	2
U7	300A, 42V	0	2	2
U8	600A, 58V	0	2	2
U9	130A, 30V	0	1	1
B1	$\pm 3A, \pm 4V$	56	76	132
B2	$\pm 3A, \pm 8V$	39	48	87
B3	$\pm 10A, \pm 6V$	2	0	2
AUX1	$\pm 1A, \pm 10V$	17	4	21
AUX2	$\pm 12A, \pm 10V$	0	5	5
Total		174	198	372

The four-quadrant PSs are used for the field adjustment and residual field cancellation of the bending magnets. As shown in Figure 2, the bending magnets of a bunch compressor are connected in series to the main PS, and the four-quadrant PSs adjust the magnetic field of each magnet.

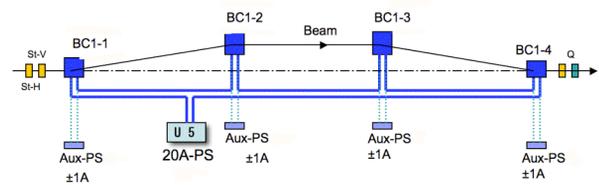


Figure 2: Connection of the first bunch compressor magnets to the power supplies (U5 and AUX).

Power Supply Stability and Interlock

The current stability of the magnet PSs, particularly for the bending magnets, is important for orbit stability of the electron beam. The specified current stability and ripple are less than $10E-5$ for some PSs (U7) and $10E-4$ for others.

A current comparing circuit of the PS gives an alarm signal when output current deviation exceeds $\pm 5\%$ of a setting value. In order to avoid the electron beam hitting to a vacuum chamber wall, some critical PSs are equipped with a further alarm system, in which current monitoring ADC data are compared to DAC data by an i-DIO FPGA program with an accuracy of $\pm 1\%$ or $\pm 0.1\%$ (Figure 3). The alarm signals are sent to device and safety interlock systems to stop the electron beam within 16 ms.

CONTROL SYSTEM

The Opt-VME/DIO system has been used in the SCSS test accelerator, 1 GeV SPring-8 injector linac, and SSBT of SPring-8 [3]. The XFEL magnet power supply control system employs the same VME field bus system, but the i-DIO is modified from the OPT-VME/DIO. The PS control application program is run on the VME and workstation system (MADOCA) [4, 5].

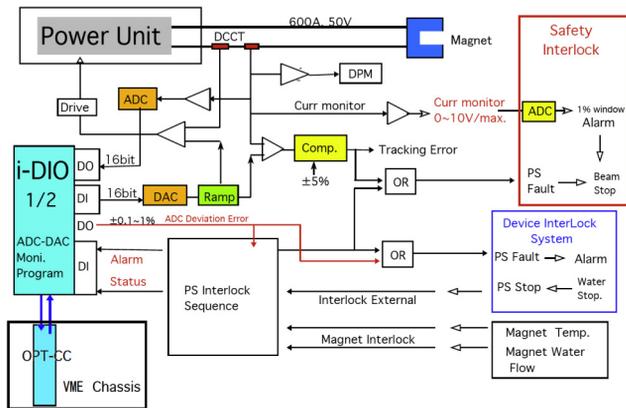


Figure 3: Block diagram of the power supply control and interlock systems.

OPT-CC

OPT-VME was first developed as a master module of the VME field bus in 2001. Then it is modified to OPT-CC, which has 12 optical ports in order to increase the number of slave cards. Also it has a relay mode to realize a star connection. The card size is 6U in the VME chassis as shown in Figure 4.

i-DIO

OPT-VME's Remote IO card (OPT-DIO) contains an FPGA for communication with the VME master module. This Remote IO card is modified to "i-DIO" in order to manage high level application programs, for example,

ADC averaging, current deviation monitoring and local control sequences (Figure 5).

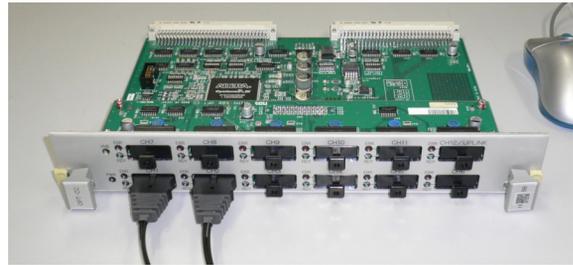


Figure 4: OPT-CC: VME field bus master module.

Basic specifications are as follows.

- 32bit DI x2port, 32bit DO x2port. Each port is isolated by photo couplers.
- Built-in to the PS chassis.
- 3 rows 64pin DIN connector x2, Euro card size 6U.
- CRC error check, overtime monitoring.

The FPGA device of the i-DIO is changed to Cyclone III (EP3C25) with 25 μ s clock. The interface between the i-DIO and power supply and the circuit block diagram are shown in Figure 6 and 7.



Figure 5: i-DIO (6U Euro size).

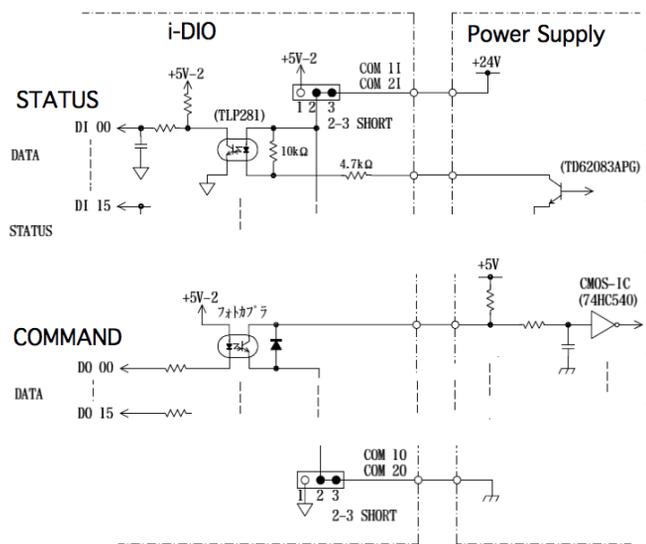


Figure 6: Interface of the i-DIO and power supply.

ADC Monitor Application

The i-DIO receives the ADC data in every 1 ms. Then the i-DIO takes a moving average of the period between 1ms and 1016ms. For the current deviation alarm, the i-DIO can compare the ADC and DAC data with a threshold level between 0.1% and 12.7%. These parameters are set by the EM program of the VME.

Local Control System

For the local control of the PSs, the i-DIO changes the DAC data according to a command from current up/down buttons on the local control panel (figure 8). The command is sent through the DI status signal and processed by the i-DIO program. On/off and reset sequences are also achieved in the same way.

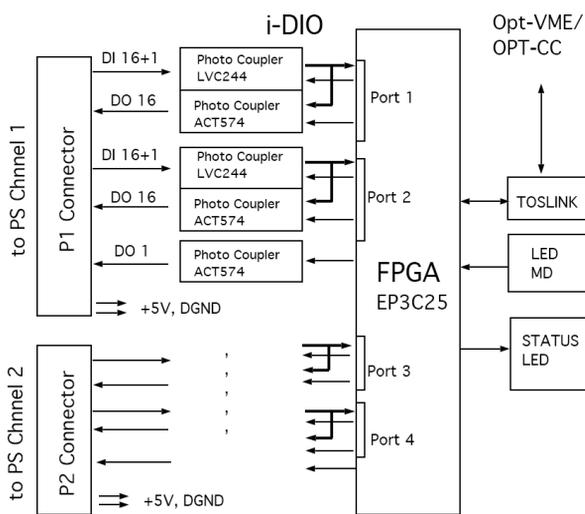


Figure 7: Block diagram of the i-DIO.

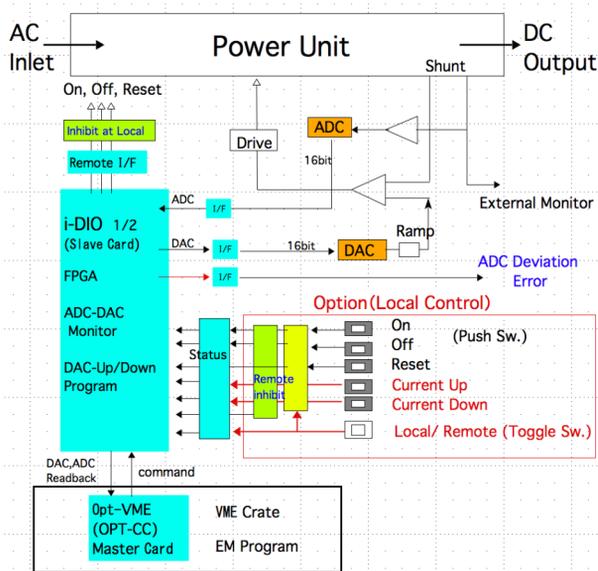


Figure 8: PS local control system using the i-DIO.

CONCLUSION

The i-DIO was tested for the first production of the PS (B1) in September 2009. Various functions of the i-DIO, such as PS-on/off, reset, current set, ADC monitor and status monitor, are successfully operating. The current monitoring alarm system works without any problem under various noise circumstances even for the finest threshold level of 0.1 %. Figure 9 shows the current stability of the PS measured by the ADC with the averaging time of 1 ms, 3 ms, 12 ms, and 50 ms. Accuracy of the ADC current monitoring data is within 3×10^{-5} for the case of 12 ms averaging.

The 64bit DI and 64bit DO interface of the i-DIO card enables to control two PSs leading to a better cost performance. Installation of the PSs to the LINAC klystron gallery and undulator gallery will start in November 2009.

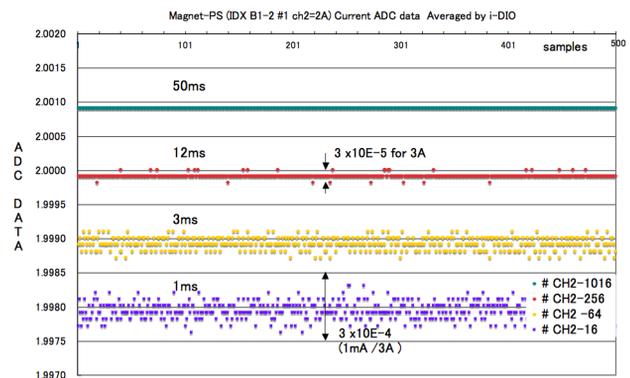


Figure 9: Current stability measured by ADC with a different averaging time.

AKNOWLEDGEMENT

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REFERENCES

- [1] <http://www.riken.jp/XFEL/eng/index.html>
- [2] T.Shintake, et al., "Status of X-ray FEL/SPring-8 Machine Construction", Proc. of EPAC08, Genova, Italy, 2008.
- [3] T. Masuda et al., "Upgrade of the SPring-8 Linac Control by Re-engineering the VME Systems for Maximizing Availability", Proc. of ICALEPCS' 03, Gyeongju, Korea, 2003.
- [4] T.Fukui, et al., "Applications of Reconfigurable Logic Devices for Accelerator Control", Proc. of ICALEPCS' 03, Gyeongju, Korea, 2003.
- [5] R. Tanaka et al., "The first operation of control system at the SPring-8 storage ring", Proc. of ICALEPCS'97, Beijing, China, 1997, p1.