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Very Fast Feedback Control of Coil-Current in JT-60 Tokamak

T. Aoyagi, T.Terakado, M.Takahashi, H.Nobusaka, J.Yagyu and Y.Matsuzaki
Japan Atomic Energy Research Institute, Naka Fusion Research Establishment,
Naka-machi, Ibaraki-ken, 311-01, Japan

Abstract

A direct digital control (DDC) system is adopted for controlling thyristor converters of power supplies in the JT-60 tokamak built in 1984. Microcomputers of the DDC were 5 MHz i8086 microprocessor and programs were written by assembler language and the processing time was under 1ms. They were, however, too old in hardware and too complicated in software. New DDC system has been made in the JT-60 Upgrade (JT-60U) to control the power supplies more quickly under 0.25 and 0.5 ms of the processing time and also to write the programs used by high-level language. The new system consists of a host computer and five microcomputers with microprocessor on VMEbus system. The host computer AS3260 performs on-line processing such as setting the DDC under the discharge conditions and so on. Functions of the microcomputers with a 32-bit, 20 MHz microprocessor MC 68030, whose OS are VxWorks and programs are written by C language, are real-time processing such as taking in instructions from a ZENKEI computer and in feedback control of currents and voltages of coils every 0.25 and 0.5 ms. The system is now operating very smoothly.

I. INTRODUCTION

Control of a current, positions and configurations of plasmas in a tokamak is done by poloidal magnetic fields, and power supplies of the poloidal field coils have to be controlled very fast to suppress intrinsic instabilities of plasmas. A schematic diagram of the feedback control system is shown in Fig.1. Magnetic probes measure magnetic fluxes of plasma and a ZENKEI real-time control computer[1] performs as follows: calculating the positions of plasmas and the derivations of the reference positions, multiplying PID gains to the derivations and outputing the command of the coil-currents. Direct digital control (DDC) of JT-60 poloidal field power supply (PFPS)[2] carries out that taking in commands of the ZENKEI (I_F^{ref} in Fig.1) and giving out the delay angle cosine (Ec) to phase controllers (PHC) of thyristors. Thyristor banks have two sets of the converters which deliver the plus and minus direction currents (I_1 and I_2), respectively, and during low-current under 20% of the rating coil-current two converters supply circulating currents (I_c) to operate the thyristors smoothly.

II. DDC SYSTEM

A. Functions

The DDC performs two functions in details such as on-line processing during no-discharge and real-time processing during discharge. Functions of on-line processing are as follows: (1) setting the DDC system under conditions of the discharge instructed by the ZENKEI, which are in detail instructions and checks on the discharge mode of CAMAC modules and of PHC and are diagnosis of them before the

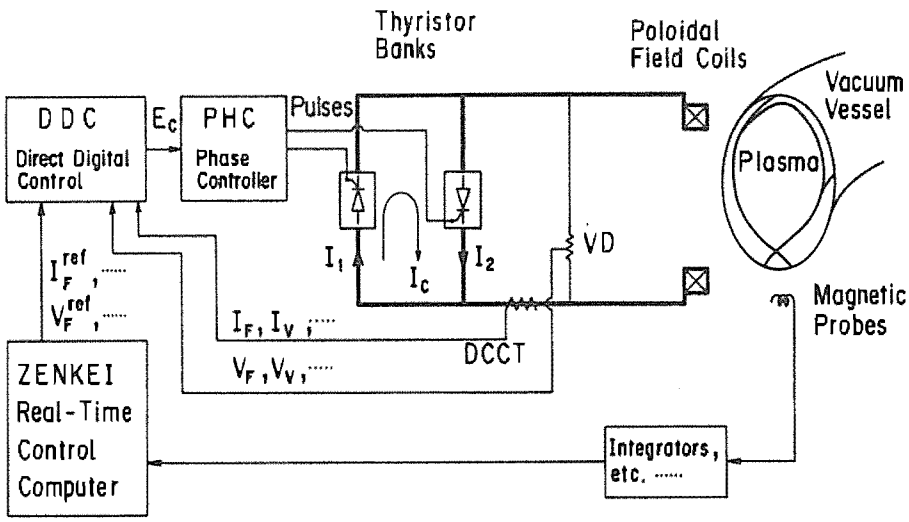

Figure 1. Schematic diagram of feedback control system of plasma position

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discharge, (2) managing the time-sequence and (3) collecting and transferring data of coils' currents and voltages to the ZENKEI after the discharge. Functions of real-time processing are taking in instructions of a feedback control computer IIb of the ZENKEI and in currents and voltages of coils which are measured by direct current current transformers (DCCT) and voltage dividers (VD), calculating minimum time response control and non-interactive control algorithms and giving out the Ec value to the PHC every 0.25, 0.5 and 1 ms as shown in Fig.1.

B. Original and old DDC system

The original DDC system consists of five CAMAC crates correspond to five converters of PFPS and one crate for collecting data. Each crate has many modules as shown in Fig. 2. Functions of the modules are as follows. An ACM module with a 5 MHz i8086 microprocessor is most important module and performs almost all control of the DDC. An ACB module is communication crate between the ZENKEI and the DDC CAMAC by branch highway (BH). An INTR module is taking in the timing clock and the interacting events. Many AI modules are taking in coil-currents and voltages, DO modules are giving the instructions of start/stop of operation, on/off of bypass pair(BPP) operation[2] and Ec values calculated to PHC.

Purposes of adopting the DDC in PFPS are not only fast processing, but also having the flexibility in the control. However, the programmings written by assembler language were very complicated and were very hard to change. Because the 16-bit microprocessor was very primitive in 1984 and it had to execute many processing during 1ms. In order to solve the problems, a developing a new system was tryed. In the system a mini-computer ECLIPSE-MV was used instead of the ACM and Ada was used as the language. The system could operate preliminarily, but it was special and expensive.

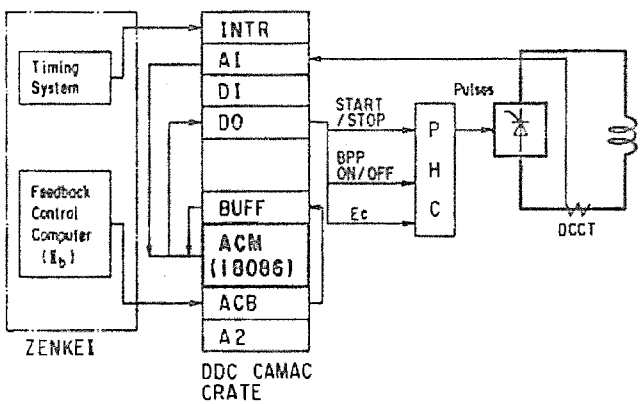

Figure 2. Schematic diagram of original CAMAC carte of DDC system in PFPS

III. NEW DDC SYSTEM

A. Objectives and configurations of new system

In JT-60U, plasma current increases to 6 MA and plasmas have large volume of 100 m^3 with vertically elongation[3]. In order to suppress intrinsic vertical instabilities of elongated plasmas, there needs faster processing and more flexible control in DDC to change the control algorithms easily and to protect over-currents of coil-power-supply systems[4]. The target of processing time is under 0.5 ms and is hopeful under 0.25 ms[5]. The flexibility of the control is as follows; (1) switching operation modes from circulating current mode to non circulating current mode, (2) changing control method from coils' current feedback control (ACR) to coils' voltage control (VR), (3) starting and stopping thyristor converters with many patterns such as gate-shifting, BPP and so on. For these purposes old DDC microcomputers and their softwares were too old in hardware and too complicated in software.

In order to fulfill above-mentioned requirements, a new DDC system had to be made, and the configurations of the system are as follows. First, it has been adopted to a newest and fastest microcomputer to write programs used by high-level language C and to execute the floating calculation, because the programmings and maintenance of the system will be easy. Second, the system has been made under the environment of UNIX, because the UNIX has been ready for debugging, editing, using many application programs and so on very strongly. Third, the network had to be adopted to the standard communication software, because there need no programs of communication. Finally, we divided the functions possessed original microcomputer i8086 in the on-line processing and the real-time processing. Because we want to program under the environment of useful and strong operational system(OS) which is equipped with a work station(WS). The WS, however, is very hard to process the real-time processing very fast, so this processing is executed by the microcomputer under an adequate OS.

B. Hardwares

An architecture of DDC system developed and made for the JT-60U is shown in Fig. 3. The main components of the system are a host computer AS3260 (Toshiba Corp.) , five microcomputers MVME 147 (Motorola Inc.) and five CAMAC crates correspond to five converters of the PFPS. The AS3260 which is the same specifications of WS Sun 3/60 is connected with a ethernet cable of the ZENKEI by a 8-channel transceiver and a bridge, and also connected with a ethernet cable of MVE crates by two 8-channel transceivers, two optical remote repeaters and two splice boxes through a optical fiber. The microcomputers which consist of a 32-bit, 20 MHz microprocessor MC 68030 and a floating point coprocessor MC 68882 on the MVEbus are mounted on chassis possessed VME backplans and power supply. The chassis encloses a CAMAC branch drivers CBD 8210

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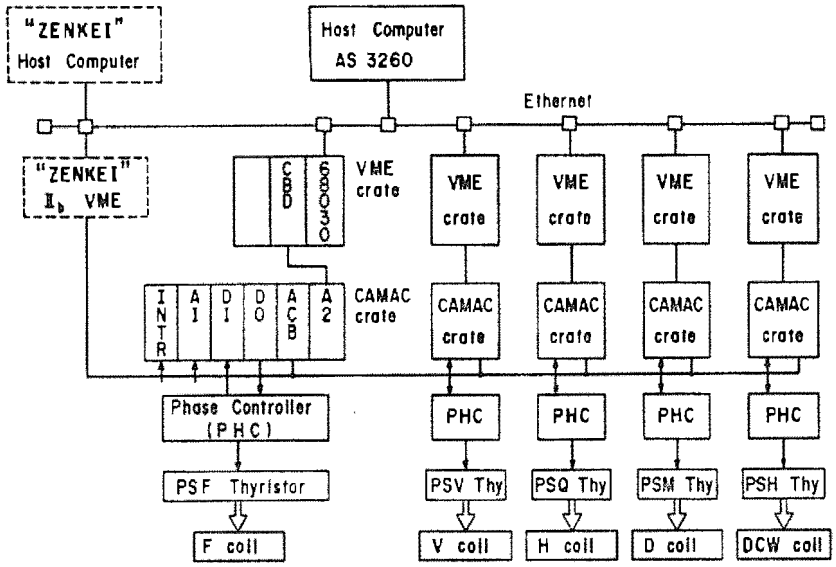

Figure 3. Architecture of new DDC system of poloidal field coil power supply

(Creative Electronic Systems) which connects the VME crate and a A2 module of the CAMAC crate by the branch highway and a I/O transition module MVME 712M. Except the ACM module, the CAMAC crate is quite same as the original architecture explained as the former section, namely it consists of a ACB module which is connected the ZENKEI IIb by BH and DO, DI, AI and INTR modules which are connected a PHC, DCCTs and so on. The system has still another hardwares such a VME crate for collecting data and a WS AS3160 and a CAMAC crate for testing the system

C. *Softwares*

An organization of the DDC software is shown in Fig.4. The host computer whose OS is UNIX performs on-line processing described in section II.A. The main programs are an on-line processing task, a ZENKEI communication task and a microcomputer communication task. The configuration of the ZENKEI communication task are as follows: (1) the processing execute each power supply separately, (2) the communication protocol is TCP/IP, (3) the connection between the ZENKEI and the AS3260 is set by actively and (4) the client is the ZENKEI IIb and the server is the AS3260. Second, the configuration of the microcomputer communication task are nearly the same as that of the ZENKEI communication task only except that the client is AS3260 and the server is each microcomputer. Finally, the on-line processing task performs as follows: (1) setting the DDC system under conditions of the discharge such as reasonable check of the power supply circuit and of constants values of many control tables and diagnosis of the crates and PHC before the discharge instructed by the ZENKEI and then answering back, (2) collecting and trans-ferring data of coils' currents and voltages to the ZENKEI.

Microcomputers whose OS are VxWorks (Wind River Systems, Inc.) carry out real-time processing. The main programs written by C language are a real-time processing task, an interrupt processing task and a communication task. The communication task performs watching and executing of the command to the CAMAC and the referencing/changing memories of CPU instructed from the host computer by TCP/IP protocol. The real-time processing task is set by the main task of the CPU, and then it begin to execute the real-time processing at the time of LAM (look at me) interrupting signal from CBD. The sequence of the real-time processing is as follows: it catches the LAM signal from the ADC of the CAMAC, then it takes in currents and voltages of coils,

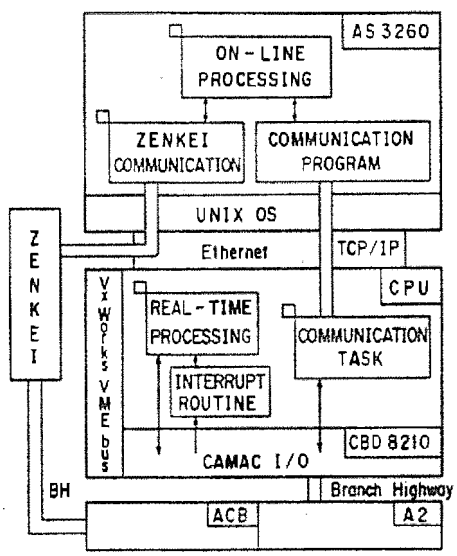

Figure 4. Organization of new DDC software

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calculates the control-algorithms and gives out the Ec value to the PHC every 0.25, 0.5 and 1 ms. Finally, the interrupt routine works from the interrupting signal of the CBD. The routine performs resets of the PHC by the BPP-command and of the Ec values of the PHC at the repair of thyristors, and it do also start-processing of the real-time processing.

IV. TESTS AND RESULTS

New DDC system has been made and tested. A processing time which is measured from input of data to output of Ec calculated is shown in Table 1.

	PSF	PSV	PSH	PSQ	PSM
ACR MODE					
With C.C	328	350	278	299	-----
Without C.C	258	264	230	235	185
VR MODE					
With C.C	304	335	261	294	----
Without C.C	267	267	237	238	190

ACR: Auto Current Regulation
VR : Voltage Regulation
C.C : Circulating Current

Table 1. Processing time of each power supply (μs)

Results are satisfied by achieving the target that the processing time is under 0.5 ms. Moreover, we achieved the processing time of 216 μs in PSQ with C.C mode by changing the clock time of the microcomputer MC 68030 from 20 MHz to 32 MHz [5].

Figure 5 shows waveforms of currents on working of PSH power supply. An upper waveform is a current of plus direction, a middle one is a minus one and a lower one is a coil current summed plus and minus currents. At a start phase, PSH1 and PSH2 power supply which deliver plus and minus current, respectively work together. At the current of 11 kA which is a half of the rating current, PSH1 stops and only PSH2 works. The constant current of 12 kA is continued during 1.5 second, and then it decreases. At a point of 4.4 kA which is 20% of the rating current, PSH1 works again, and then the coil current switches from minus to plus. At the end of the operation, PSH1 and PSH2 are to terminate in gate-shifting operation[2], namely in inverter operation for reducing the coil current quickly, and the results are very satisfactory. In order to achieve this operation, some new algorithms and computer simulations were performed.

The new DDC system has been made, tested and operated on five coil-currents' power supplies, and the results showed that the system operated very smoothly about the very sophisticated control such as switching operation modes, changing control method from ACR to VR and starting and stopping of BPP of thyristor converters during the real-time control. Moreover, the new system was applied to controlling the vertical instability of plasmas, and the results showed that the oscillation amplitude of the vertical instabilities decrease from 4.5 cm to 3.2 cm as changing the clock time from 1 ms to 0.25 ms, respectively [5].

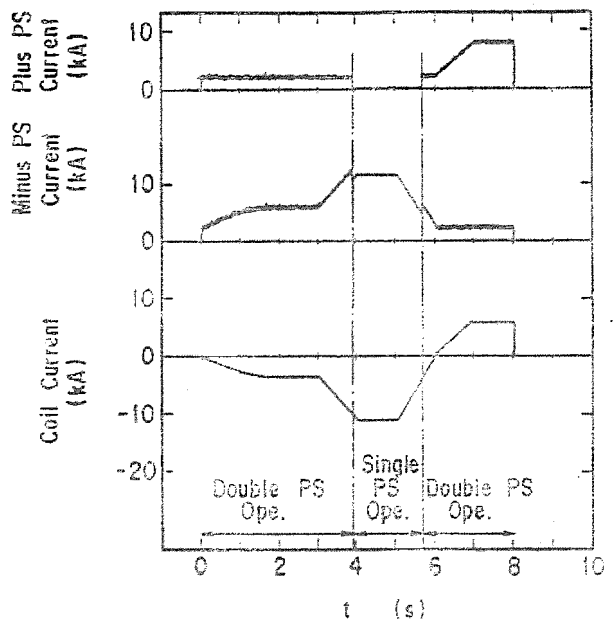

Figure 5.
Waveforms of currents controlled by new DDC system

V. CONCLUSIONS

We have modified direct digital control (DDC) system of thyristors converters in JT-60 poloidal power supplies to process quickly and to have the flexibility in the control. Results of operations showed that these modifications have been performed very good.

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REFERENCES

1. I. Kondo et al., Fusion Engineering and design 5 (1987) 69
2. R.Shimada et al., ibid. 47
3. H.Ninomiya et al., Plasma Devices and Operations, 1(1990) 43
4. Y. Matsuzaki et al., Proc. of 16th SOFT (1990) 1482
5. M.Takahashi et al., this conference