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RF Control System of the HIMAC Synchrotron

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Abstract

An RF control system of the HIMAC synchrotron has been constructed. In this control system we have adopted a digital feed back system with a digital synthesizer (DS). Combining a high power system, performance of the control system have been tested in a factory (Toshiba) with a simulator circuit of the synchrotron oscillation. Following this test, we had beam acceleration test with this control system at TARN-II in INS (institute for Nuclear Study, University of Tokyo). This paper describes the RF control system and its tested results.

Introduction

HIMAC is a heavy ion accelerator facility dedicated to the medical use, especially for the clinical treatment of tumors. The ion species required for the clinical treatment range from ^{4}He to ^{40}Ar. The required beam energy is from 100MeV/u to 800 MeV/u. This maximum energy is determined so that the silicon ions can penetrate into a human body with a depth of about 30cm. A maximum beam intensity is determined to finish one irradiation within a short time, which is 10^{11}ppp for helium beam. There is also a requirement of low intensity beam of 10^{7}ppp from counter experiment. The HIMAC synchrotron has been designed to satisfy these requirements. In table 1 major parameters of this synchrotron are listed. The characteristic requirements for the RF acceleration system of this synchrotron are followings.

1) Wide RF range (from 1MHz to 8MHz).
2) Wide beam intensity range between 10^{7}ppp and 10^{11}ppp in the synchrotron.

To control wide acceleration frequency stably with low FM noise, a digital control system with a digital synthesizer (Stanford Telecommunication, STEL-1375a) has been adopted for the HIMAC RF control system (See Fig.1). Beam monitors of position (ΔR) and phase ($\Delta\phi$), which can be used with wide beam intensity range, have been developed also. This $\Delta\phi$ monitor must have fast response to use for $\Delta\phi$ feedback loop which damp the synchrotron oscillation. We have checked the $\Delta\phi$ feedback loop with the developed simulator circuit in a factory. In the test with the simulator, we found that the $\Delta\phi$ feedback loop could damp the simulated synchrotron oscillation of frequency up to 6kHz. This result is good enough, because the maximum frequency is 4kHz in the HIMAC synchrotron. As a next step of the test, we have tried to accelerate the beam by use of the developed RF control system.

Table 1
Parameters of the HIMAC synchrotron

Beam species	He^{2+} to Ar^{18+}
Injection energy	6 MeV/u
Momentum spread of the injected beam	$<\pm 0.3\%$
B (injection/maximum)	.1/1.5 T
Field ramp	2 T/sec
Repetition rate	0.5 - 1.5 Hz
Maximum beam energy	800MeV/u
Beam intensity range	10^{7} ppp -10^{11} ppp
Circumference	129.6 m
Transition γ	3.67
Harmonic number	4
Frequency range	1 - 8 MHz
Filling factor	0.8
Peak voltage	<11 kV (at 1MHz)
Synchrotron frequency	1 - 4 kHz

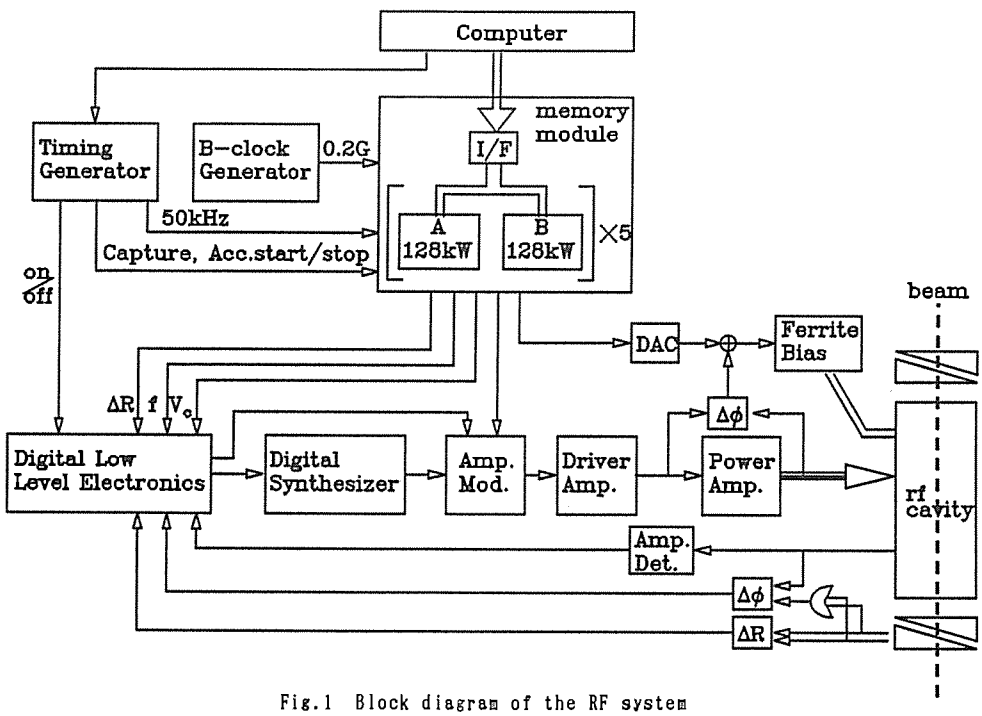

Fig.1 Block diagram of the RF system

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Pattern generation

The pattern memory devices are designed to generate the patterns of an accelerating frequency, an accelerating voltage, a ferrite bias current, a bias of beam position, and an accelerating voltage correction. In the computer of man-machine interface, data points of the patterns are given by the formula firstly and can be corrected after by the operator. These pattern data are sent to the computer (RF computer) which control acceleration system directly. The data size of one pattern must be less than 128k words. For each kind of pattern there are two memory units. One memory unit is used to control each device, and the another memory unit is used to change the pattern data in it. With these two memories the pattern data can be changed without stop of the system. This make system tuning easy.

To output the pattern data from the memory to the control devices, two kinds of pulses are used to change the pointer address. One is clock pulse of 50 kHz (T-clock) and the another is the pulse of increment (or decrement) of the dipole magnetic field (B-clock). One pulse of the B^{+}-clock (B^{-}-clock) corresponds to 0.2 Gauss increment (decrement). To generate the pattern data with these clocks, pattern memories are divided into following three regions.

1) region-1
   T-clock is used to generate the pattern data, which determine the pattern in the flat base.
2) region-2
   B-clock is used to generate the pattern of the accelerating period.
3) region-3
   T-clock is used again to generate the pattern in the flat top.

An event pulse of the beam capture starts to advance the pattern memory address of region-1 with T-clock. To start the beam acceleration, an event pulse changes the T-clock to B-clock and jump to the memory address in region-2 where the output frequency data is same as the last data in the memory region-1. To stop the beam acceleration in the flat top, an event pulse of the flat top changes the memory address to the first address of the region-3. If there is difference between the last output data and the data of the head address in region-3, the output value is moved to the data of the head address with one bit step. This function make the change of the output value smooth and is important not to loss the beam.

Beam monitors

The electrostatic pick-up beam monitors of position (ΔR) and phase ($\Delta\phi$) have been developed, which are described in the other paper[1]. In the following only specific features are listed:

1) The developed monitors can be used at the lowest beam intensity of the HIMAC synchrotron (10^{7}ppp), and the output errors of the $\Delta\phi$ and ΔR monitors are ± 3 deg. and ± 3mm with the lowest beam intensity, respectively. The monitor gains can be selected from 0dB to 100dB with 10dB step.
2) Response of the both monitors are fast enough to use for the feed back loops. The delay times of $\Delta\phi$ and ΔR monitors for step function are $7\mu s$ and $20\mu s$, respectively.

Digital control circuit

To control the wide range accelerating frequency stably, we have adopted the digital control circuit which is shown in Fig.2. The ΔR and $\Delta\phi$ analog signals are converted to digital data every $2\mu s$ with eleven bits (+ sign bit) ADCs which are located near the rf cavity together with the beam monitor electronics. One bit corresponds to 2.4mV (0.052mm in the ΔR monitor and 0.087° in the $\Delta\phi$ monitor). In the control module, the ΔR digital data is biased firstly to control the beam center at optimum position. Then the start-stop function of the feed back with time constant of about $100\mu s$ are followed. The ΔR and the $\Delta\phi$ data are added after adjustments of a proportional loop gain in the $\Delta\phi$ feed back, and proportional and integral loop gains in the ΔR feed back. This sum data is further added to the frequency pattern data from the memory module. The data of twenty bits is used to drive the DS, and one bit corresponds to 10Hz. Clock frequency of 10MHz is used for the digital processing, and time delay between digitizing the analog data (ΔR and $\Delta\phi$) and driving the DS with new data is $2\mu s$.

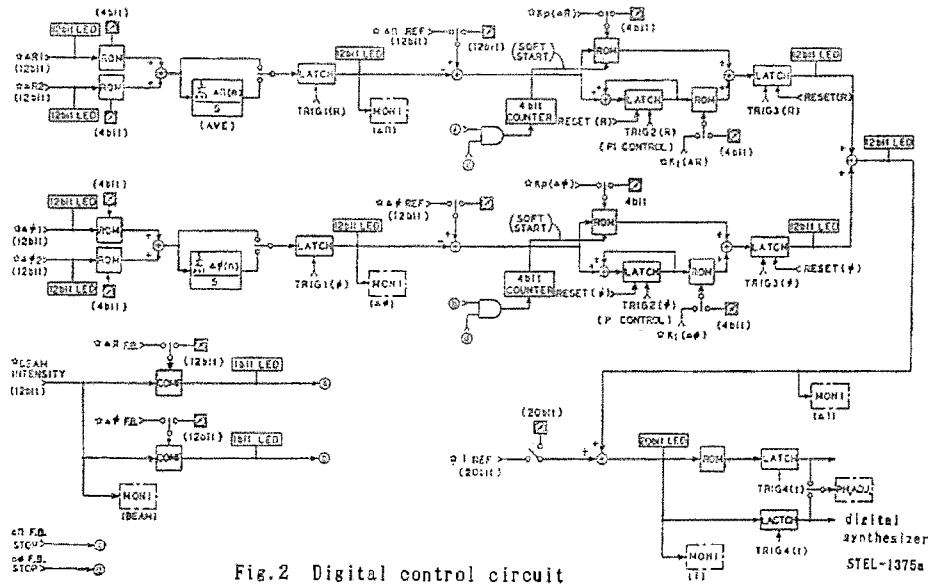

Fig.2 Digital control circuit

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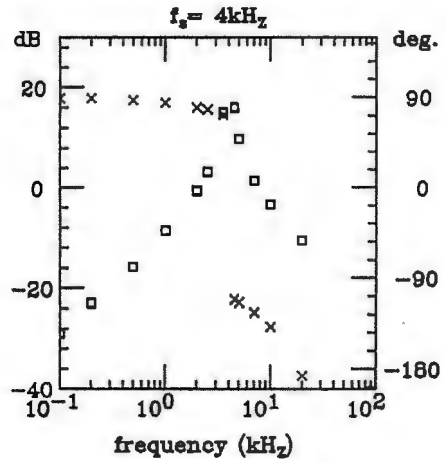

Fig.3 Calculated open loop transfer function of $\Delta\phi$ feed back loop. □;gain, ×;phase.

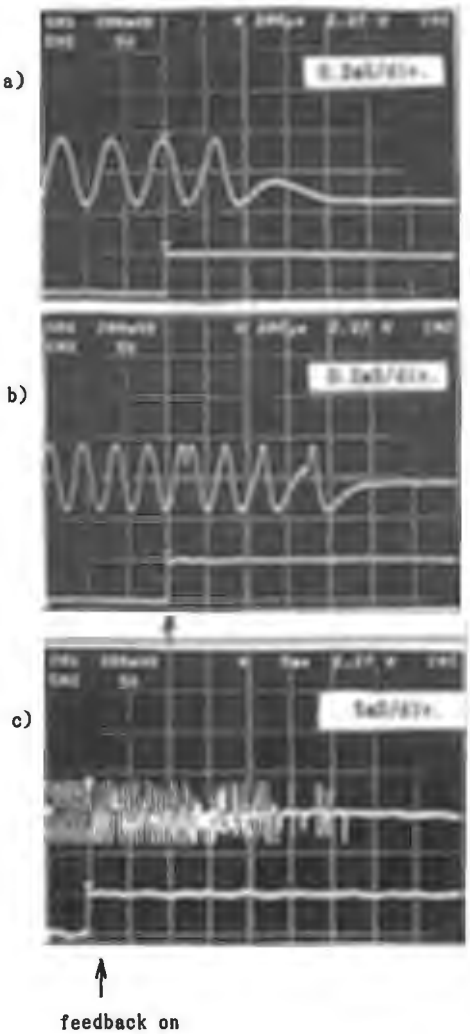

Fig.4 Damping test of the synchrotron oscillation with $\Delta\phi$ feed back with the simulator circuit. The test were performed with synchrotron oscillation frequencies of a) 4kHz, b) 6kHz, and c) 7kHz. The input signal voltage at a first FET ampilfier is 4mV(p-p) and f_{rf}=1MHz.

Test of the feed back loop with the simulator circuit

To check the effectiveness of the $\Delta\phi$ feed back loop, an open loop transfer function has been calculated. In this calculation response delays of the following parts have been considered.

1) 7μs in the $\Delta\phi$ beam monitor.
2) 1μs and 2μs for the digitizing the analog data and the digital processing, respectively.
3) 1.5μs in the DS.
4) 1.5μs in the RF cavity.

The calculated result with the critical damping condition is shown in Fig.3. From this result the response of the $\Delta\phi$ feed back is fast enough to damp the synchrotron oscillation of 4kHz, which is maximum frequency in HIMAC synchrotron.

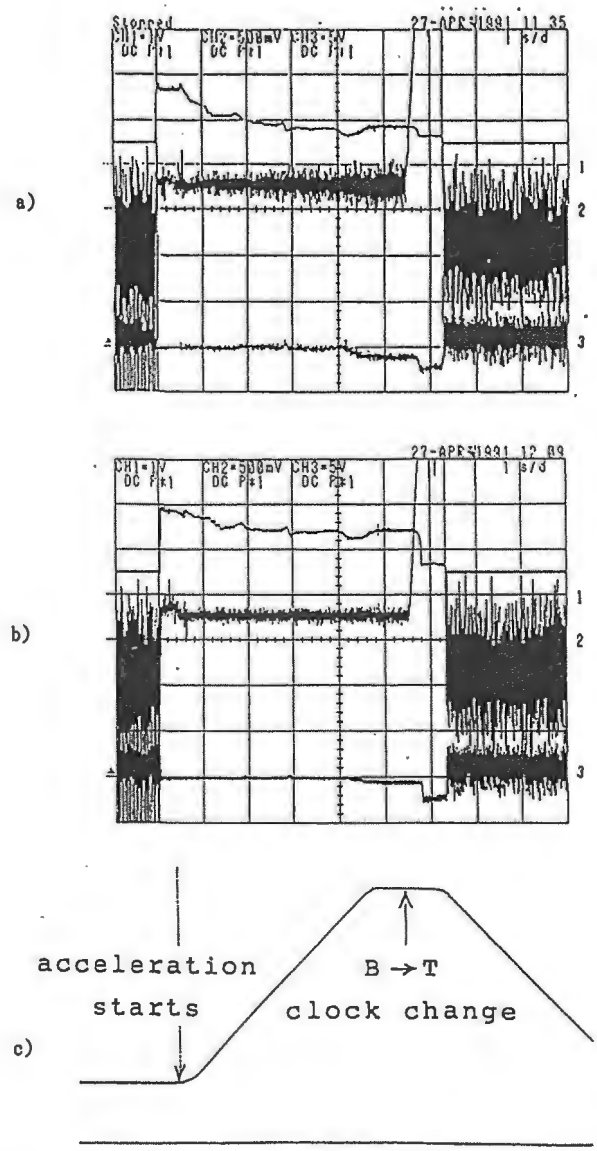

Fig.5. Outputs of the beam monitors. Upper trace is the beam intensity, middle trace is ΔR, and lower trace is $\Delta\phi$ in each picture. Strength of the $\Delta\phi$ feed back loop is a) critical damping b) five times of a). Fig.5-c) shows a corresponding field pattern of the dipole magnet. The acceleration period was 4.46 sec.

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To test the $\Delta\phi$ feed back loop further, we have used a newly developed simulator which is a circuit to generated the synchrotron like oscillation. It has the similar transfer function as the synchrotron oscillation. The test was performed with the condition that f_{rf}=1 MHz and f_s (frequency of the synchrotron oscillation) = 4, 6, and 7kHz. As shown in Fig.4, the feed back loop could damp the oscillation of 6kHz quickly. From these results, it is clear that the $\Delta\phi$ feed back loop has fast response which is good enough for our purpose, because the maximum frequency of the synchrotron oscillation is 4 kHz.

Test of beam acceleration

If there is a large phase jump when the accelerating frequency is swept, the accelerated beam will be lost. To make sure that there is no large phase jump in our DS, we have performed the beam test. To do the beam test at TARN-II, we have joined our RF control system (computer, timing generater, memory module, digital low level electronics, digital synthesizer, beam monitor electronics) with the RF system of TARN-II[2),3)]. In this beam test, we could not prepare our B-clock generator of 0.2 Gauss clock. Though the B clock of TARN-II is generated every 1 Gauss increment of the dipole magnetic field, this B-clock was used in the beam test. To see the effect of the corresponding frequency step in the beam acceleration, we have tried to accelerate the beam without the filter which smoothes the step function in the analog RF control system of TARN-II. Though there existed a clear effect of the step function, the beam could be accelerated. We have decided to use the 1 Gauss clock for our digital control system, which has no element to smooth the frequency step in this digital system.

Firstly in the beam test, we have adjusted the position bias in the ΔR feedback loop. If the adjustment was not correct, the beam was lost when the ΔR feedback loop was turned on. The next step was to adjust the strength of the feedback loop on ΔR and $\Delta\phi$. As the beam intensity was low, the low pass filter of 1kHz was inserted in the ΔR position monitor. From this fact the strength of the ΔR feedback loop has been set at weak value. About the $\Delta\phi$ feedback, the strength of the critical damping condition was not enough. As shown in Fig.5, the best strength of the $\Delta\phi$ feedback loop was about five times stronger than the strength of the critical damping condition at the flat base.

Conclusion

We have constructed the RF control system with the digital synthesizer. The $\Delta\phi$ feed back loop has been checked successfully with the simulator circuit in the factory. In the beam test, we could accelerate the He^{2+} beam from 10MeV/u to 160MeV/u. These energies correspond to the acceleration frequencies of 1.1 MHz and 4.0 MHz, respectively. The tuning of the control system was very simple and easy to succeed in the beam acceleration. This is the characteristic feature of the digital control system and important in the medical accelerator. The acceleration efficiency was about 55%. The possible reasons of the beam loss are;

1) The low beam intensity which makes large noise in the beam monitors, which is due to white noise in the FET of the first amplifier.
2) The RF noise whose effect was enlarged with the low beam intensity.
3) The B-clock step of 1 Gauss which makes the longitudinal beam emittance growth. (In the analog system, we can use the filter to smooth this B-clock step.)

Improving these things with the longer beam monitor electrode and the B-clock step of 0.2 Gauss in the HIMAC RF system, it will be possible to accelerate the beam without large beam loss.

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